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XRT73LC00A

E3/DS3/STS-1 LINE INTERFACE UNIT

MAY 2011 *REV. 1.0.2*

GENERAL DESCRIPTION

The XRT73LC00A DS3/E3/STS-1 Line Interface Unit is a low power CMOS version of the XRT73L00A and consists of a line transmitter and receiver integrated on a single chip and is designed for DS3, E3 or SONET STS-1 applications.

XRT73LC00A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates.

In the transmit direction, the XRT73LC00A encodes input data to either B3ZS (for DS3/STS-1 applications) or HDB3 (for E3 applications) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction the XRT73LC00A performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of line code violations.

The XRT73LC00A also contains a 4-Wire Microprocessor Serial Interface for accessing the on-chip Command registers.

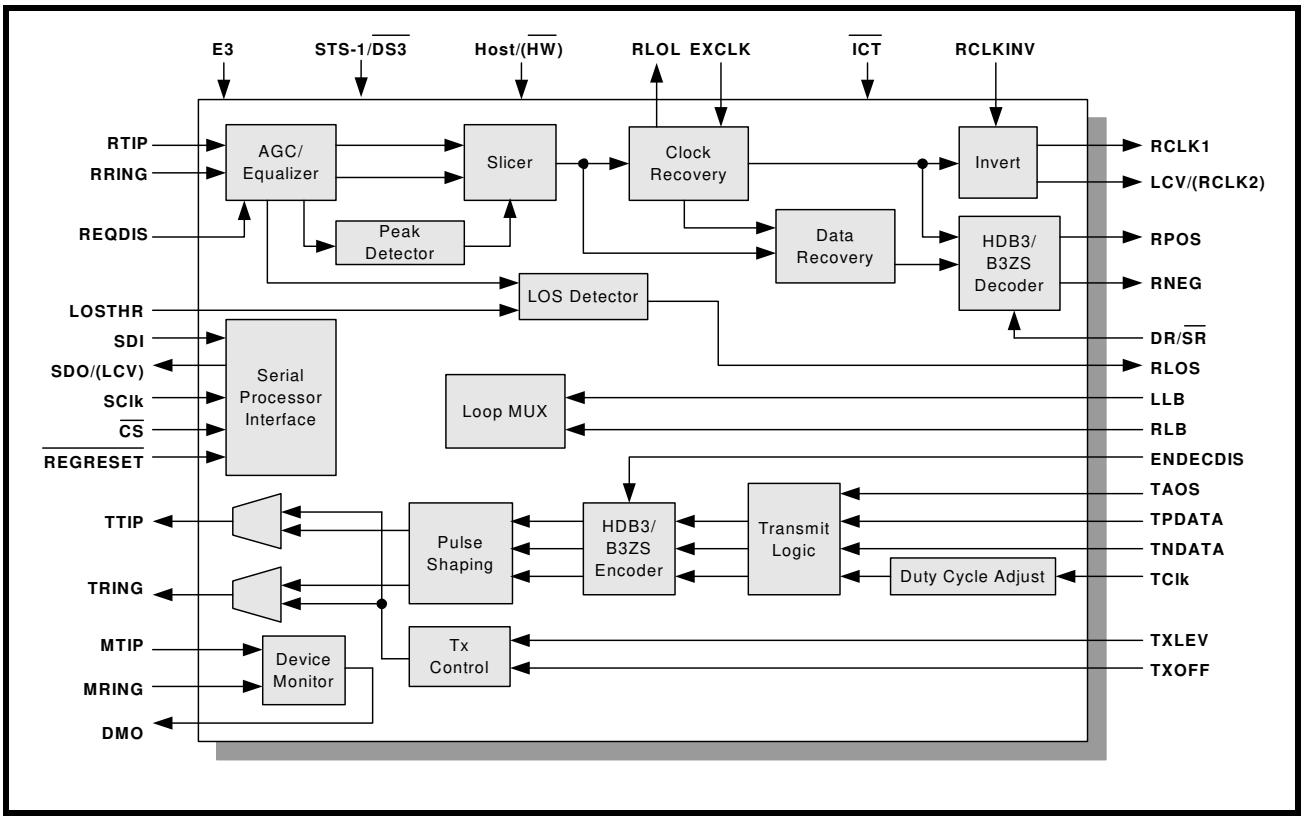
FEATURES

- Incorporates an improved Timing Recovery circuit and is pin and functional compatible to XRT73L00A
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Contains a 4-Wire Microprocessor Serial Interface
- Uses Minimum External components
- Low Power CMOS Design
- Single +3.3V Power Supply
- 5 V Tolerant pins
- -40°C to +85°C Operating Temperature Range
- Available in a 44 pin TQFP package

APPLICATIONS

- Interfaces to E3, DS3 or SONET STS-1 Networks
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

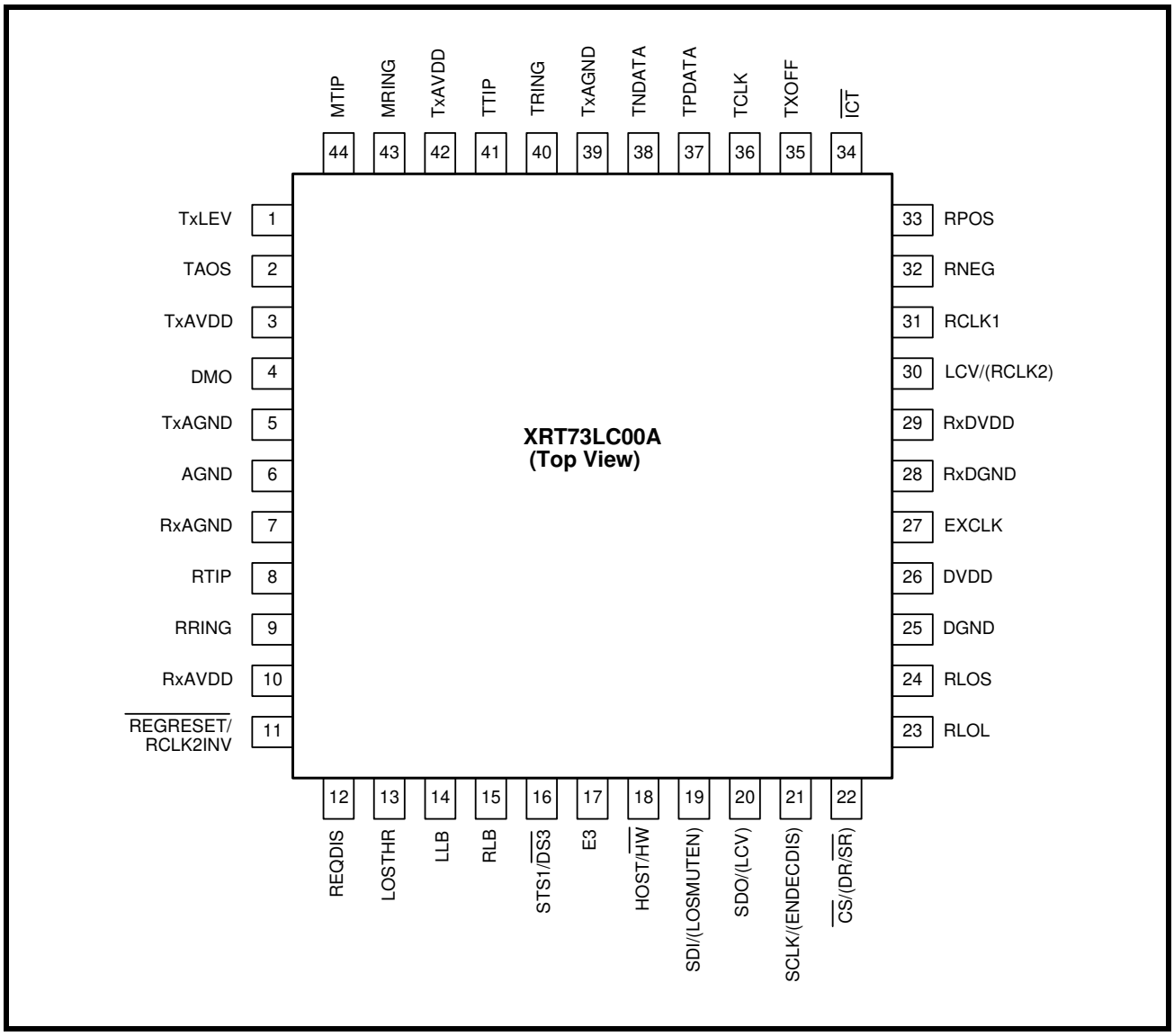
FIGURE 1. BLOCK DIAGRAM OF THE XRT73LC00A



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT73LC00AIV	44 Pin TQFP (10mm x 10mm)	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT73LC00A IN THE 44 PIN TQFP



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PIN DESCRIPTION

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
1	TXLEV	I	Transmit Line Build-Out Enable/Disable Select: This input pin is used to enable or disable the Transmit Line Build-Out circuit in the XRT73LC00A. Setting this pin to “High” disables the Line Build-Out circuit. In this mode, the XRT73LC00A outputs partially shaped pulses onto the line via the TTIP and TRING output pins. Setting this pin to “Low” enables the Line Build-Out circuit. In this mode, the XRT73LC00A outputs partially-shaped pulses onto the line via the TTIP and TRING output pins. To comply with the isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-Core or Bellcore GR-253-Core: 1. Set this input pin to a "1" if the cable length between the Cross-Connect and the transmit output of the XRT73LC00A is greater than 225 feet. 2. Set this input pin to a "0" if the cable length between the Cross-Connect and the transmit output of the XRT73LC00A is less than 225 feet. This pin is active only if both of the following are true: (a) The XRT73LC00A is configured to operate in either the DS3 or SONET STS-1 modes and (b) The XRT73LC00A is configured to operate in the Hardware Mode. ***NOTE:*** *This pin should be tied to GND if the XRT73LC00A is to be operated in the HOST mode.*
2	TAOS	I	Transmit All Ones Select: A “High” on this pin causes a continuous AMI all “1’s” pattern to be transmitted onto the line. The frequency of this “1’s” pattern is determined by TCLK. ***NOTES:*** *1. This input pin is ignored if the XRT73LC00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73LC00A is going to be operating in the HOST Mode.*
3	TxAVDD	****	Transmit Analog Power Supply
4	DMO	O	Drive Monitor Output: If no bipolar line signal is detected on the TTIP/TRING output pins via the MTIP and MRING input pins for 128±32 TCLK periods, then the DMO output pin toggles and remains “High” until the next bipolar pulse is detected.
5	TxAGND	****	Transmit Analog Ground
6	AGND	****	Analog Ground (Substrate)
7	RxAGND	****	Receive Analog Ground
8	RTIP	I	Receive TIP Input: This input pin along with RRING is used to receive the line signal from the Remote DS3/E3/STS-1 Terminal.
9	RRING	I	Receive RING Input: This input pin along with RTIP is used to receive the line signal from the Remote DS3/E3/STS-1 Terminal.
10	RxAVDD	****	Receive Analog Power Supply

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
11	$\overline{\text{REGRESET}}$/ (RCLK2INV)	I	Register Reset Input pin (Invert RCLK2 Output - Select): The function of this pin depends upon whether the XRT73LC00A is operating in the HOST Mode or in the Hardware Mode. HOST Mode - Register Reset Input pin: Setting this input pin "Low" causes the XRT73LC00A to reset the contents of the Command Registers to their default settings and operating configuration. This pin is internally pulled "High". Hardware Mode - Invert RCLK2 Output Select: Setting this input pin "Low" configures the Receive Section of the XRT73LC00A to output the recovered data via the RPOS and RNEG output pins on the rising edge of the RCLK2 output signal. Setting this input pin "High" configures the Receive Section to output the recovered data on the falling edge of the RCLK2 output signal.
12	REQDIS	I	Receive Equalization Disable Input: Setting this input pin "High" disables the Internal Receive Equalizer in the XRT73LC00A. Setting this pin "Low" enables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTES:*** *1. This input pin is ignored if the XRT73LC00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73LC00A is going to be operating in the HOST Mode.*
13	LOSTHR	I	Loss of Signal Threshold Control: This input pin is used to select the LOS (Loss of Signal) Declaration and Clearance thresholds for the Analog LOS Detector circuit. Two settings are provided by forcing this signal to either GND or VDD. ***NOTE:*** *This pin is only applicable during DS3 or STS-1 operations.*
14	LLB	I	Local Loop-Back Select: This input pin along with RLB dictates which Loop-Back mode the XRT73LC00A is operating in. A "High" on this pin with RLB being set to "Low" configures the XRT73LC00A to operate in the Analog Local Loop-Back Mode. A "High" on this pin with RLB also being set to "High" configures the XRT73LC00A to operate in the Digital Local Loop-Back Mode. ***NOTES:*** *1. This input pin is ignored if the XRT73LC00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73LC00A is going to be operating in the HOST Mode.*

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
15	RLB	I	Remote Loop-Back Select: This input pin along with LLB dictates which Loop-Back mode the XRT73LC00A is operating in. A "High" on this pin with LLB being set to "Low" configures the XRT73LC00A to operate in the Remote Loop-Back Mode. A "High" on this pin with LLB also being set to "High" configures the XRT73LC00A to operate in the Digital Local Loop-Back Mode. ***NOTES:*** *1. This input pin is ignored if the XRT73LC00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73LC00A is going to be operating in the HOST Mode.*
16	STS-1/$\overline{\text{DS3}}$	I	STS-1/$\overline{\text{DS3}}$ Select Input: A "High" on this pin configures the Clock Recovery Phase Locked Loop to set its VCO Center frequency to around 51.84 MHz for SONET STS-1 operations. A "Low" on this pin configures the Clock Recovery Phase Locked Loop to set its VCO Center frequency to around 44.736 MHz for DS3 operations. ***NOTES:*** *1. The XRT73LC00A ignores this pin if the E3 pin (pin 17) is set to "1".* *2. This input pin is ignored if the XRT73LC00A is operating in the HOST Mode.* *3. Tie this pin to GND if the XRT73LC00A is going to be operating in the HOST Mode.*
17	E3	I	E3 Select Input: A "High" on this pin configures the XRT73LC00A to operate in the E3 Mode. A "Low" on this pin configures the XRT73LC00A to check the state of the STS-1/$\overline{\text{DS3}}$ input pin. ***NOTES:*** *1. This input pin is ignored if the XRT73LC00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73LC00A is going to be operating in the HOST Mode.*
18	HOST/$\overline{\text{HW}}$	I	HOST/$\overline{\text{HW}}$ Mode Select: This input pin is used to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SCLK, $\overline{\text{CS}}$ and $\overline{\text{REGRESET}}$ pins). Setting this input pin "High" enables the Microprocessor Serial Interface (e.g. configures the XRT73LC00A to operate in the HOST Mode). In this mode, the XRT73LC00A is configured by writing data into the on-chip Command Registers via the Microprocessor Serial Interface. When the XRT73LC00A is operating in the HOST Mode, it ignores the states of many of the discrete input pins. Setting this input pin "Low" disables the Microprocessor Serial Interface (e.g., configures the XRT73LC00A to operate in the Hardware Mode). In this mode, many of the external input control pins are functional.

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
19	SDI/ (LOSMUTEN)	I	Serial Data Input for the Microprocessor Serial Interface (HOST Mode) or MUTE-upon-LOS Enable Input (Hardware Mode): The function of this input pin depends upon whether the XRT73LC00A is operating in the HOST or the Hardware Mode. Serial Data Input for the Microprocessor Serial Interface (HOST Mode): This pin is used to read or write data into the Command Registers of the Microprocessor Serial Interface. The Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations are applied to this pin. This input is sampled on the rising edge of the SCLK pin (pin 21). MUTE-upon-LOS Enable Input (Hardware Mode): In the Hardware Mode this input pin is used to configure the XRT73LC00A to Mute the recovered data via the RPOS and RNEG output pins whenever it declares an LOS condition. Setting this input pin “High” configures the XRT73LC00A to automatically pull the RPOS and RNEG output pins to GND whenever it is declaring an LOS condition, thereby Muting the data being output to the Terminal Equipment. Setting this input pin “Low” configures the XRT73LC00A to NOT automatically Mute the recovered data whenever an LOS condition is declared.
20	SDO/(LCV)	O	Serial Data Output from the Controller Port/(Line Code Violation Output (LCV) Indicator.): The function of this input pin depends upon whether the XRT73LC00A is operating in the HOST or the Hardware Mode. HOST Mode - Microprocessor Serial Interface - Serial Data Output. This pin serially outputs the contents of the specified Command Register during Read Operations. The data on this pin is updated on the falling edge of the SCLK input signal. This pin is tri-stated upon completion of data transfer. Hardware Mode - Line Code Violation Output Indicator. This pin pulses “High” for one bit period any time the Receive Section of the XRT73LC00A detects a Line Code Violation in the incoming E3, DS3 or STS-1 Data Stream.
21	SCLK/ (ENDECDIS)	I	Microprocessor Serial Interface Clock Signal/Encoder Disable: HOST Mode - Microprocessor Serial Interface Clock Signal This signal is used to sample the data on the SDI pin on the rising edge of this signal. During Read operations, the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. Hardware Mode - B3ZS/HDB3 Encoder/Decoder Disable Setting this input pin “High” disables both the B3ZS/HDB3 Encoder and Decoder. This setting configures the Transmit Section of the XRT73LC00A to transmit data to the remote terminal equipment via the AMI Line Code. This setting also configures the Receive Section to receive a line signal via the AMI Line Code. Setting this input pin “Low” enables both the B3ZS/HDB3 Encoder and Decoder. This setting configures the Transmit Section of the XRT73LC00A to transmit data in the B3ZS format for DS3/STS-1 applications or the HDB3 format for E3 applications. This setting configures the Receive Section to receive a line signal that has been encoded into the B3ZS or HDB3 line code.

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
22	$\overline{CS}$/(DR/$\overline{SR}$)	I	Microprocessor Serial Interface - Chip Select/Encoder and Decoder Disable The function of this input pin depends upon whether the XRT73LC00A is operating in the HOST or the Hardware Mode. HOST Mode - Chip Select Input: The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT73LC00A via the Microprocessor Serial Interface. Hardware Mode - Dual-Rail/Single-Rail Select Input: Setting this input pin "High" configures the XRT73LC00A to operate in the Dual-Rail Mode. When the XRT73LC00A is operating in this mode, then the Receive Section of the LIU IC outputs the Recovered Data via both RPOS and RNEG output pins. Setting this input pin "Low" configures the XRT73LC00AXRT73LC00A to operate in the Single-Rail Mode. When the XRT73LC00A is operating in this mode, the Receive Section of the LIU IC outputs the Recovered Data via the RPOS output pin in a binary data stream. No data will output via the RNEG output pin.
23	RLOL	O	Receive Loss of Lock Output Indicator This output pin toggles "High" if the XRT73LC00A has detected a Loss of Lock Condition. The XRT73LC00A declares an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXCLK input pin) by more than 0.5%. ***NOTE:*** *The RCLK1/2 output pins are sourced by the signal applied at the EXCLK input pin anytime the XRT73LC00A declares an LOL condition.*
24	RLOS	O	Receive Loss of Signal Output Indicator This output pin toggles "High" if the XRT73LC00A has detected a Loss of Signal Condition in the incoming line signal. The criteria the XRT73LC00A uses to declare an LOS Condition depends upon whether the device is operating in the E3 or DS3/STS-1 Mode.
25	DGND	****	Digital Ground
26	DVDD	****	Digital Power Supply
27	EXCLK	I	External Reference Clock Input: Apply a line-rate clock signal to this input pin. This signal is a 34.368MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications. ***NOTE:*** *This input pin functions as the source of the RxCLK output clock signal any time the XRT73LC00A declares an LOL condition.*
28	RxDGND	****	Receiver Digital Ground
29	RxDVDD	****	Receiver Digital Power Supply

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
30	LCV/(RCLK2)	O	Line Code Violation Indicator/Receive Clock Output pin 2: The function of this pin depends upon whether the XRT73LC00A is operating in the HOST Mode, the Hardware Mode or User selection. HOST Mode - Line Code Violation Indicator Output: If the XRT73LC00A is configured to operate in the HOST Mode, then this pin functions as the LCV output pin by default. However, by using the on-chip Command Registers, this pin can be configured to function as the second Receive Clock signal output pin RCLK2. Hardware Mode - Receive Clock Output pin 2: This output pin is the Recovered Clock signal from the incoming line signal. The receive section of the XRT73LC00A outputs data via the RPOS and RNEG output pins on the rising edge of this clock signal. ***NOTE:*** *If the XRT73LC00A is operating in the HOST Mode and this pin is configured to function as the additional Receive Clock signal output pin, then the XRT73LC00A can be configured to update the data on the RPOS and RNEG output pins on the falling edge of this clock signal.*
31	RCLK1	O	Receive Clock Output pin 1: This output pin is the Recovered Clock signal from the incoming line signal. The receive section of the XRT73LC00A outputs data via the RPOS and RNEG output pins on the rising edge of this clock signal. ***NOTE:*** *If the XRT73LC00A is operating in the HOST Mode, the device can be configured to update the data on the RPOS and RNEG output pins on the falling edge of this clock signal.*
32	RNEG	O	Receive Negative Pulse Output: This output pin pulses “High” whenever the XRT73LC00A has received a Negative Polarity pulse in the incoming line signal at the RTIP/RRING inputs. ***NOTES:*** 1. *If the B3ZS/HDB3 Decoder is enabled, the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are not reflected at this output.* 2. *This output pin is inactive if the XRT73LC00A has been configured to operate in the Single-Rail Mode.*
33	RPOS	O	Receive Positive Pulse Output: This output pin pulses “High” whenever the XRT73LC00A has received a Positive Polarity pulse in the incoming line signal at the RTIP/RRING inputs. ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled, the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are not reflected at this output.*
34	ICT	I	In-Circuit Test Input: Setting this input pin “Low” causes all digital and analog outputs to go into a high-impedance state in order to permit in-circuit testing. Set this pin “High” for normal operation. ***NOTE:*** *This pin is internally pulled “High”.*

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
35	TXOFF	I	Transmitter OFF Input: Setting this input pin "High" configures the XRT73LC00A to turn off the Transmitter in the device. When the Transmitter is shut-off, the TTIP and TRING output pins will be tri-stated in the XRT73LC00A. ***NOTES:*** *1. This input pin is NOT ignored if the XRT73LC00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73LC00A is going to be operating in the HOST Mode.*
36	TCLK	I	Transmit Clock Input for TPDATA and TNDATA: This input pin must be driven at 34.368 MHz for E3 applications, 44.736MHz for DS3 applications, or 51.84MHz for SONET STS-1 applications. The XRT73LC00A uses this signal to sample the TPDATA and TNDATA input pins. The XRT73LC00A is configured to sample these two pins on the falling edge of this signal. If the XRT73LC00A is operating in the HOST Mode, then the device can be configured to sample the TPDATA and TNDATA input pins on the rising edge of TCLK.
37	TPDATA	I	Transmit Positive Data Input: The XRT73LC00A samples this pin on the falling edge of TCLK. If the device samples a "1" at this input pin, then it generates and transmits a positive polarity pulse to the line. ***NOTES:*** *1. The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If the XRT73LC00A is operating in the HOST Mode, then the XRT73LC00A can be configured to sample the TPDATA pin on either the rising or falling edge of TCLK.*
38	TNDATA	I	Transmit Negative Data Input: The XRT73LC00A samples this pin on the falling edge of TCLK. If the device samples a "1" at this input pin, then it generates and transmits a negative polarity pulse to the line. ***NOTES:*** *1. This input pin is ignored and should be tied to GND if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If the XRT73LC00A is operating in the HOST Mode, then the XRT73LC00A can be configured to sample the TNDATA pin on either the rising or falling edge of TCLK.*
39	TxAGND	-	Transmit Analog Ground
40	TRING	O	Transmit TRING Output: The XRT73LC00A uses this pin along with TTIP to transmit a bipolar line signal via a 1:1 transformer. ***NOTE:*** *This output pin along with TTIP is tri-stated anytime the TxOFF input pin or bit-field is set "high".*

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
41	TTIP	O	Transmit TIP Output: The XRT73LC00A uses this pin along with TRING to transmit a bipolar line signal via a 1:1 transformer. ***NOTE:*** *This output pin along with TRING is tri-stated anytime the TxOFF input pin or bit-field is set "high".*
42	TxAVDD	-	Transmit Analog Power Supply
43	MRING	I	Monitor Ring Input: This input pin along with the MTIP pin function as the input pins for the Transmit Drive Monitor. These two input pins are used to determine whether or not a bipolar line signal is being output via the TTIP and TRING output pins. The Transmit Drive Monitor circuit will toggle the DMO output pin "high" denoting a Transmit Line Fault condition if no bipolar pulses are detected via the TTIP/TRING output pins for 128 bit-periods. Connect this input pin to the TRING output pin via a 270 ohm resistor. ***NOTE:*** *Tie this input pin to GND if you do not intend to use the Transmit Drive Monitor.*
44	MTIP	I	Monitor Tip Input: This input pin along with the MRING pin function as the input pins for the Transmit Drive Monitor. These two input pins are to be used to determine whether or not a bipolar line signal is being output via the TTIP and TRING output pins. The Transmit Drive Monitor circuit will toggle the DMO output pin "high" denoting a Transmit Line Fault condition if no bipolar pulses are detected via the TTIP/TRING output pins for 128 bit periods. Connect this input pin to the TTIP output pin via a 270 ohm resistor. ***NOTE:*** *Tie this input pin to GND if you do not intend to use the Transmit Drive Monitor.*

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

POWER SUPPLY	**-0.5 TO +3.465V**
STORAGE TEMPERATURE	**-65°C TO 150°C**
INPUT VOLTAGE AT ANY PIN	**-0.5V TO 5.0V**
POWER DISSIPATION TQFP PACKAGE	**1.2W**
INPUT CURRENT AT ANY PIN	**+100MA**
ESD RATING (MIL-STD-883, M-3015)	**1500V**

DC ELECTRICAL CHARACTERISTICS

(Ta = 25°C, Vdd = 3.3V ± 5%, unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DDD}	DC Supply Voltage	3.135	3.3	3.465	V
V_{DDA}	DC Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all “1’s”)			125	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA			0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA	2.8			V
I_L	Input Leakage Current*			±10	µA

** Not applicable to pins with pull-up/pull-down resistors.*

AC ELECTRICAL CHARACTERISTICS

(Ta = 25°C, Vdd = 3.3V ± 5%, unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Terminal Side Timing Parameters (See Figure 3 & Figure 4)					
	TCLK Clock Duty Cycle (DS3/STS-1)	30	50	70	%
	TCLK Clock Duty Cycle (E3)	30	50	70	%
	TCLK Frequency (SONET STS-1)		51.84		MHz
	TCLK Frequency (DS3)		44.736		MHz
	TCLK Frequency (E3)		34.368		MHz
t_{RTX}	TCLK Clock Rise Time (10% to 90%)			4	ns
t_{FTX}	TCLK Clock Fall Time (90% to 10%)			4	ns
t_{TSU}	TPDATA/TNDATA to TCLK Falling Set up time	3			ns
t_{THO}	TPDATA/TNDATA to TCLK Falling Hold time	3			ns
t_{LCVO}	RCLK to rising edge of LCV output delay		2.5		ns
t_{TDY}	TTIP/TRING to TCLK Rising Propagation Delay time	0.6		14	ns
	RCLK Clock Duty Cycle	45	50	55	%
	RCLK Frequency (SONET STS-1)		51.84		MHz
	RCLK Frequency (DS3)		44.736		MHz
	RCLK Frequency (E3)		34.368		MHz
t_{CO}	RCLK to RPOS/RNEG Delay Time			4	ns
t_{RRX}	RCLK Clock Rise Time (10% to 90%)		2	4	ns
t_{FRX}	RCLK Clock Fall Time (10% to 90%)		1.5	3	ns
C_i	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

FIGURE 3. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE

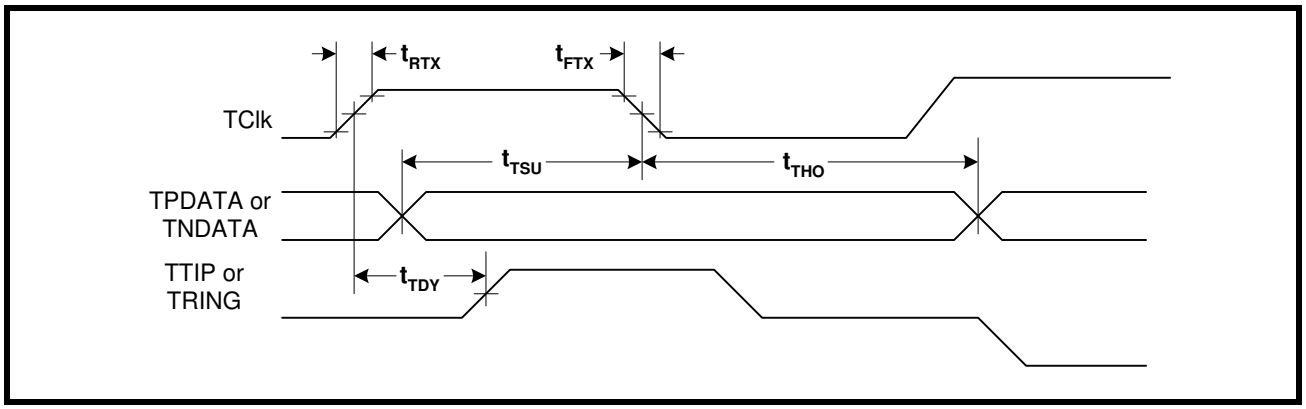


FIGURE 4. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE

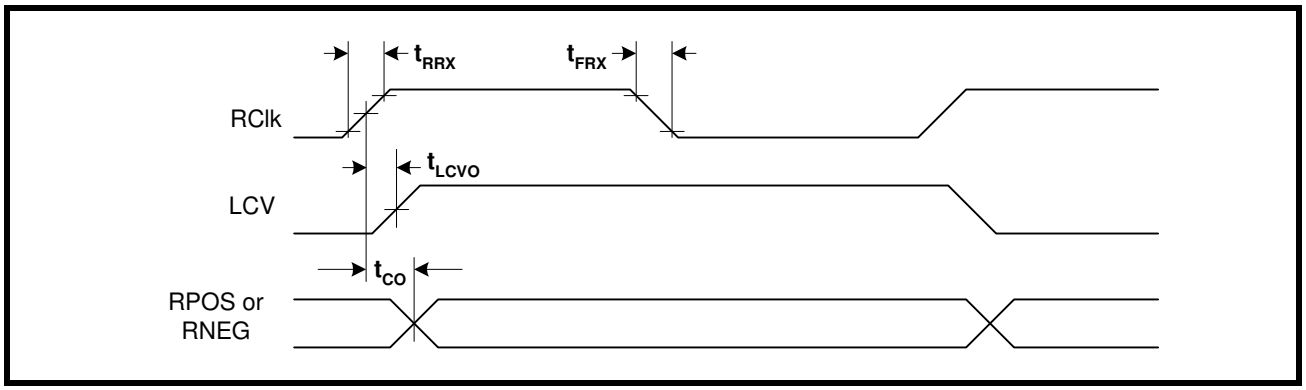
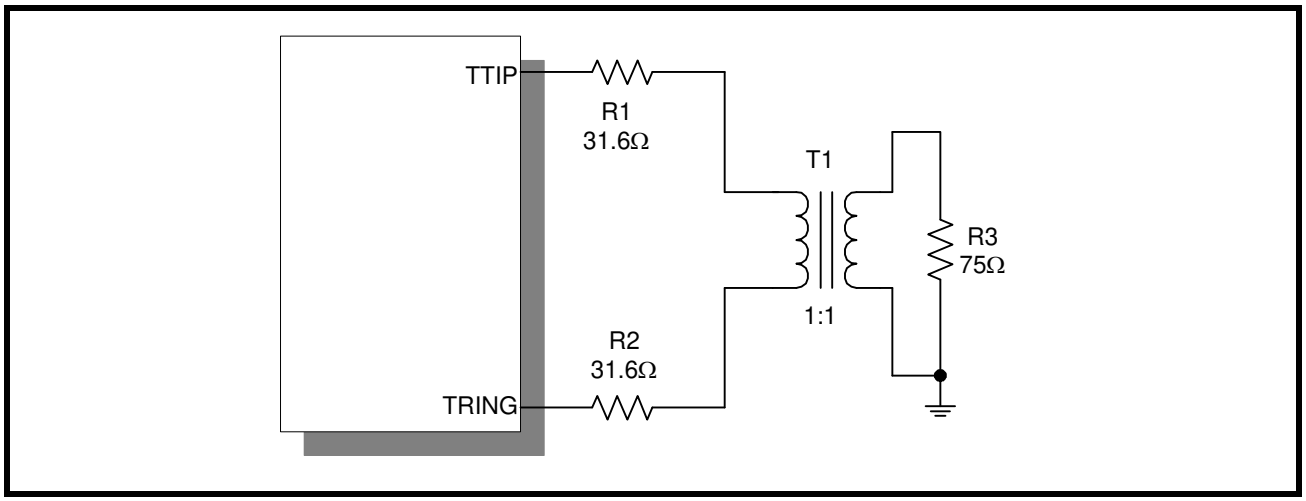


FIGURE 5. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR DS3, E3 AND STS-1 RATES



AC ELECTRICAL CHARACTERISTICS (CONT'D) Line Side Parameters

(Ta = 25°C, Vdd = 3.3V ± 5%, unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
E3 Application Parameters Transmit Line Characteristics (See Figure 5)					
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input clock at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	1200	1400		feet
	Interference Margin	-20	-17		dB
	Signal Level to Declare Loss of Signal			-35	dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10	100	255	UI
	Termination of LOS to LOS Clearance Time	10	100	255	UI
	Intrinsic Jitter (all "1's" Pattern)		0.01		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1KHz	30			UI
	Jitter Tolerance @ Jitter Frequency = 10KHz	4			UI
	Jitter Tolerance @ Jitter Frequency = 800KHz	0.15	0.20		UI

AC ELECTRICAL CHARACTERISTICS (CONT'D) Line Side Parameters

(Ta = 25°C, Vdd = 3.3V ± 5%, unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
SONET STS-1 Application Parameters Transmit Line Characteristics (See Figure 5)					
	Transmit Output Pulse Amplitude (Measured with TXLEV = 0)	0.65	0.75	0.90	Vpk
	Transmit Output Pulse Amplitude (Measured with TXLEV = 1)	0.93	0.98	1.08	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free clock input at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (see Table 4)				mV
	Intrinsic Jitter (all "1's" Pattern)		0.03		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1KHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10KHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 400KHz	0.15	0.35		UI

AC ELECTRICAL CHARACTERISTICS (CONT'D) LINE SIDE PARAMETERS

(Ta = 25°C, Vdd = 3.3V ± 5%, unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DS3 Application Parameters Transmit Line Characteristics (See Figure 5)					
	Transmit Output Pulse Amplitude (Measured at 0 feet, TXLEV = 0)	0.65	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured at 0 feet, TXLEV = 1)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input clock at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of Cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (see Table 4)				mV
	Intrinsic Jitter (All One's Pattern)		0.01		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1KHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10KHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 300KHz -- (Cat II)	0.35	0.45		UI

Figure 6, Figure 7 and Figure 8 present the Pulse Template requirements for the E3, DS3 and STS-1 Rates.

FIGURE 6. ITU-T G.703 TRANSMIT OUTPUT PULSE TEMPLATE FOR E3 APPLICATIONS

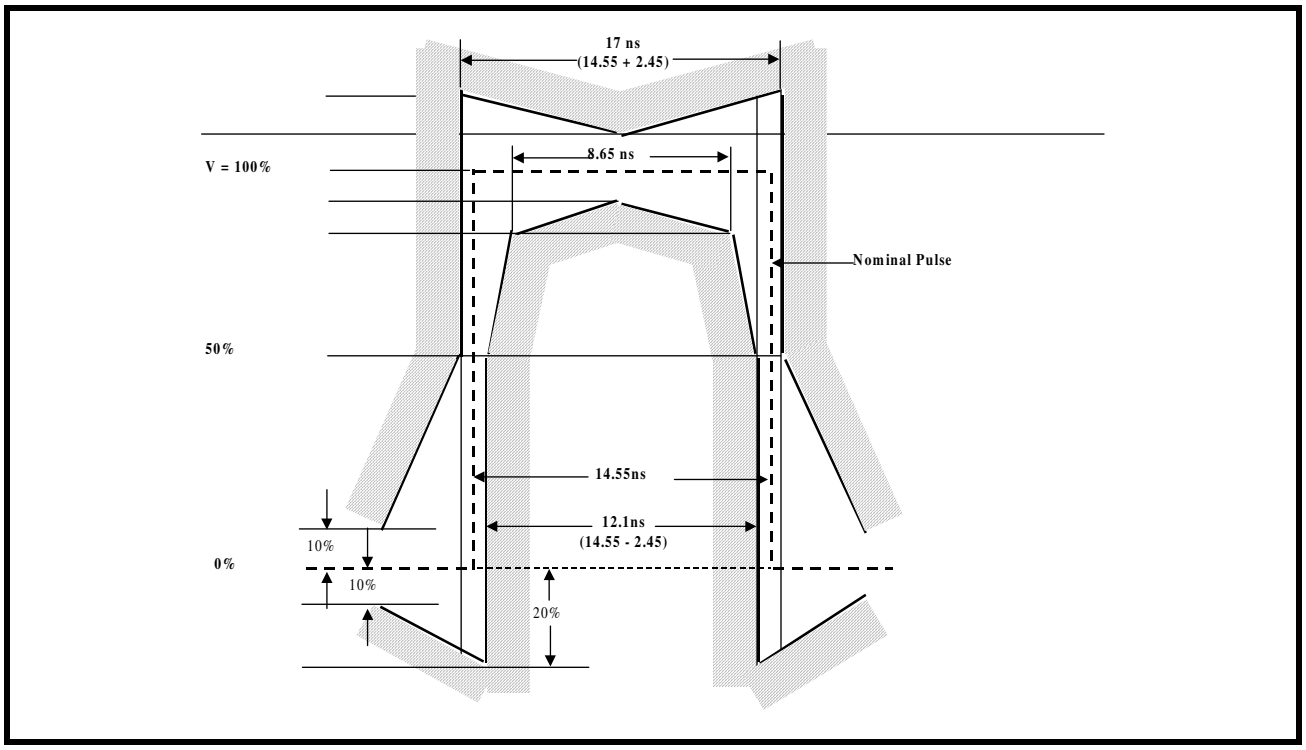


FIGURE 7. BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

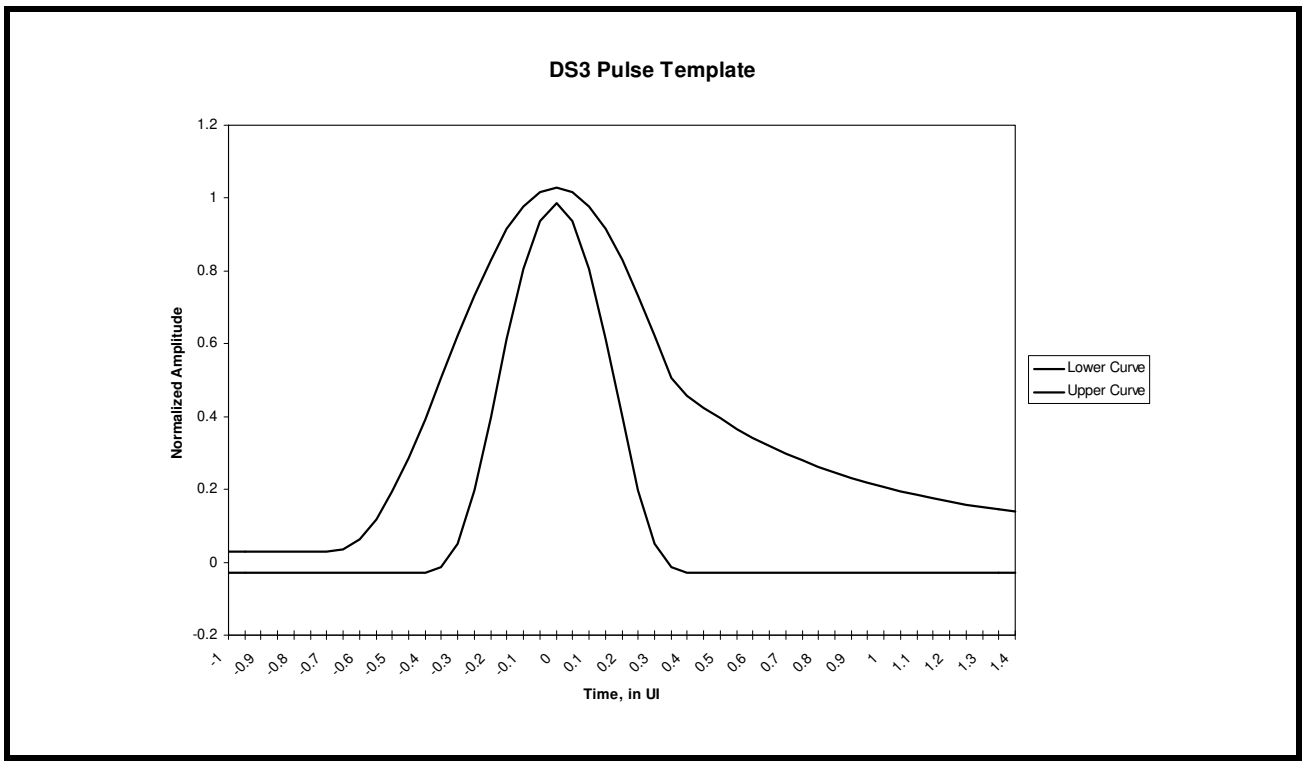


FIGURE 8. BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

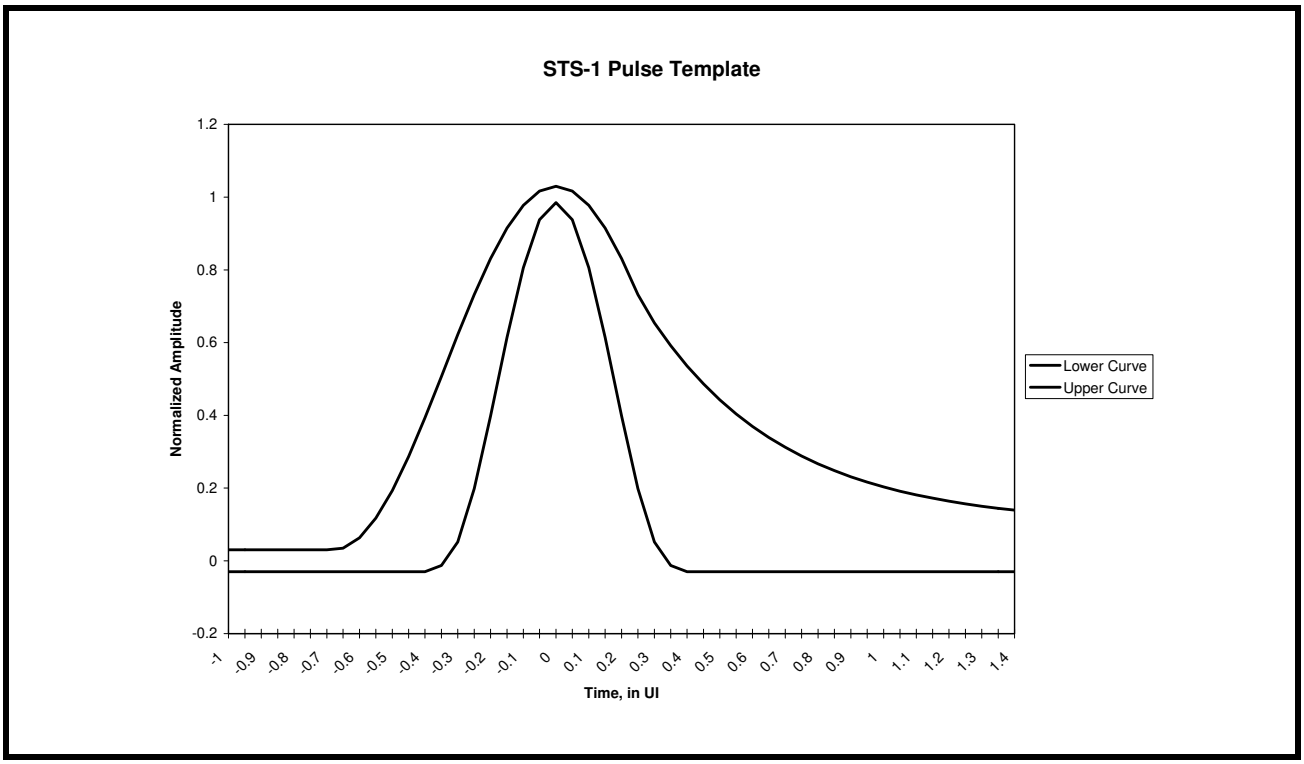
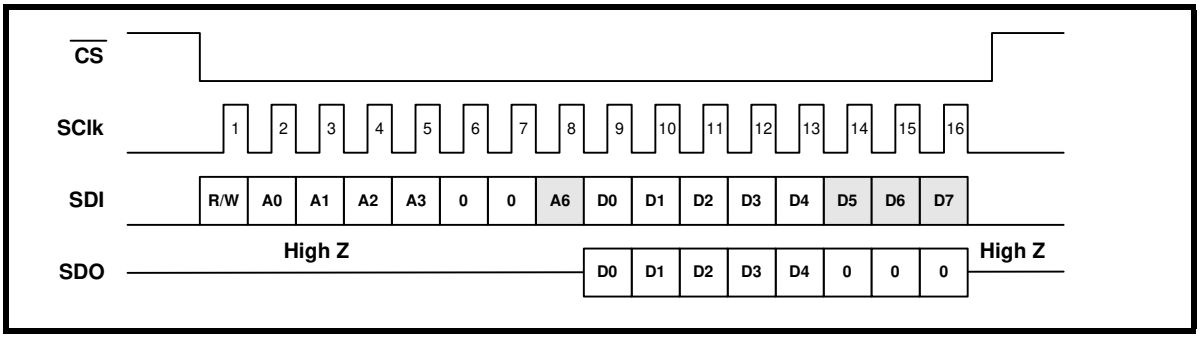


FIGURE 9. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

1. *A4 and A5 are always "0".*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*

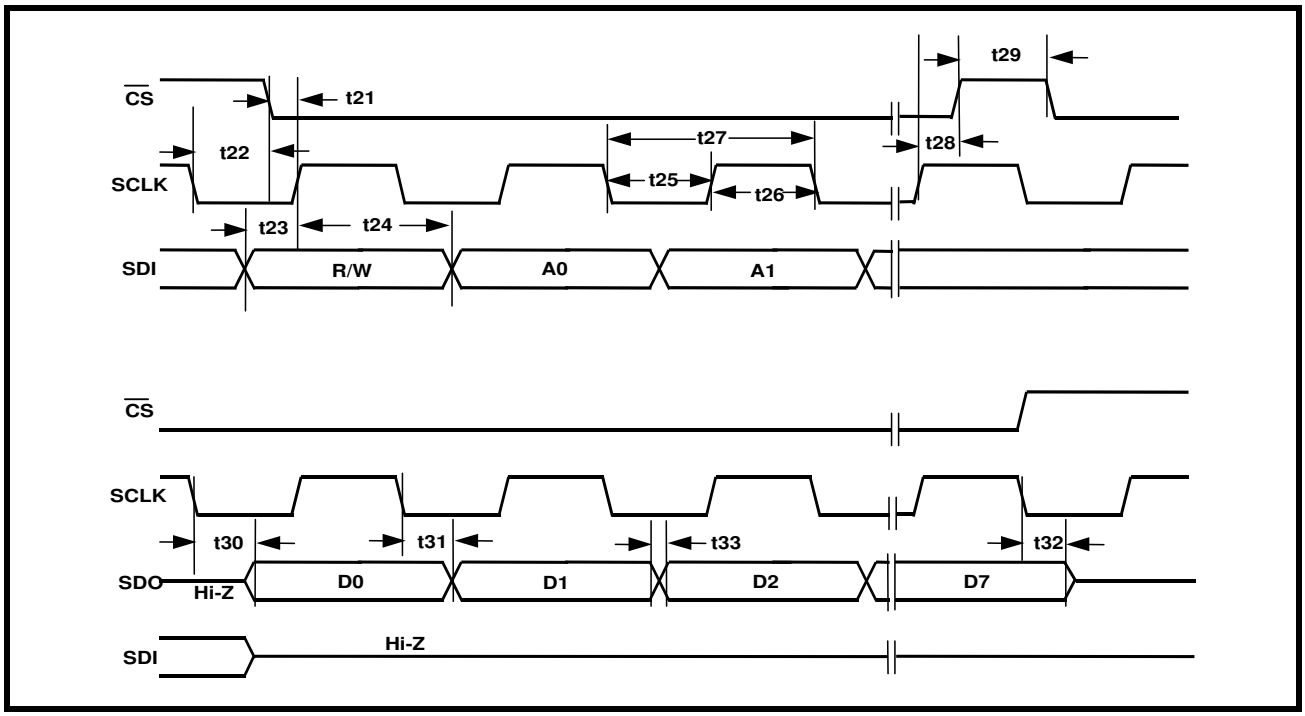
A shaded pulse, denotes a “don’t care” value.

AC ELECTRICAL CHARACTERISTICS (CONT.)

(Ta = 25°C, Vdd = 3.3V ± 5%, unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Microprocessor Serial Interface Timing (see Figure 10)					
t_{21}	$\overline{CS}$ Low to Rising Edge of SCLK Setup Time	5			ns
t_{22}	SCLK Falling Edge to $\overline{CS}$ Low Assertion Time	20			ns
t_{23}	SDI to Rising Edge of SCLK Setup Time	50			ns
t_{24}	SDI to Rising Edge of SCLK Hold Time	50			ns
t_{25}	SCLK "Low" Time	240			ns
t_{26}	SCLK "High" Time	240			ns
t_{27}	SCLK Period	500			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SCLK Hold Time	5			ns
t_{29}	$\overline{CS}$ Inactive Time	250			ns
t_{30}	Falling Edge of SCLK to SDO Valid Time			200	ns
t_{31}	Falling Edge of SCLK to SDO Invalid Time			100	ns
t_{32}	Falling Edge of SCLK or Rising Edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			40	ns

FIGURE 10. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



SYSTEM DESCRIPTION

A functional block diagram of the XRT73LC00A E3/DS3/STS-1 Transceiver IC (see Figure 1) shows that the device contains three distinct sections:

- The Transmit Section
- The Receive Section
- The Microprocessor Serial Interface

THE TRANSMIT SECTION

The Transmit Section accepts TTL/CMOS level signals from the Terminal Equipment in either a Single-Rail or Dual-Rail format. The Transmit Section then takes this data and does the following:

- Encodes the data into the B3ZS format if the DS3 or SONET STS-1 Modes have been selected or into the HDB3 format if the E3 Mode has been selected.
- Converts the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements.
- Drives these pulses onto the line via the TTIP and TRING output pins across a 1:1 Transformer.

NOTE: *The Transmit Section drives a "1" (or a Mark) on the line by driving either a positive or negative polarity pulse across the 1:1 Transformer within a given bit period. The Transmit Section drives a "0" (or a Space) onto the line by driving no pulse onto the line.*

THE RECEIVE SECTION

The Receive Section receives a bipolar signal from the line either via a 1:1 Transformer or a 0.01mF Capacitor. As the Receive Section receives this line signal it does the following:

- Adjusts the signal level through an AGC circuit.
- Optionally equalizes this signal for cable loss.
- Attempts to quantify a bit-interval within the line signal as either a “1”, “-1” or a “0” by slicing this data. This sliced data is used by the Clock Recovery PLL to recover the timing element within the line signal.
- The sliced data is routed to the HDB3/B3ZS Decoder, during which the original data content as transmitted by the Remote Terminal Equipment is restored to its original content.
- Outputs the recovered clock and data to the Local Terminal Equipment in the form of CMOS level signals via the RPOS, RNEG, RCLK1 and RCLK2 output pins.

THE MICROPROCESSOR SERIAL INTERFACE

The XRT73LC00A can be configured to operate in either the Hardware Mode or the HOST Mode.

The Hardware Mode

Connect the HOST/$\overline{\text{HW}}$ input pin (pin 18) to GND to configure the XRT73LC00A to operate in the Hardware Mode.

When the XRT73LC00A is operating in the Hardware Mode, the following is true:

1. The Microprocessor Serial Interface block is

disabled.

2. The XRT73LC00A is configured via input pin settings.

Each of the pins associated with the Microprocessor Serial Interface takes on their alternative role as defined in Table 1.

3. All of the remaining input pins become active.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT73LC00A IS OPERATING IN THE HARDWARE MODE

PIN #	PIN NAME	FUNCTION WHILE IN THE HARDWARE MODE
11	$\overline{\text{REGRESET}}$/(RCLK2INV)	RCLK2INV
19	SDI/(LOSMUTEN)	LOSMUTEN
20	SDO/(LCV)	LCV
21	SCLK/(ENDECDIS)	ENDECDIS
22	$\overline{\text{CS}}$/(DR/$\overline{\text{SR}}$)	DR/$\overline{\text{SR}}$
30	LCV/(RCLK2)	RCLK2