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XRT73LC03A

3 CHANNEL DS3/E3/STS-1 LINE INTERFACE UNIT

REV. 1.0.4

GENERAL DESCRIPTION

The XRT73LC03A, 3-Channel, DS3/E3/STS-1 Line Interface Unit is a low power CMOS version of the XRT73L03A and consists of three independent line transmitters and receivers integrated on a single chip designed for DS3, E3 or SONET STS-1 applications.

Each channel of the XRT73LC03A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channels.

In the transmit direction, each channel encodes input data to either B3ZS (DS3/STS-1) or HDB3 (E3) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT73LC03A performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of Line Code Violations.

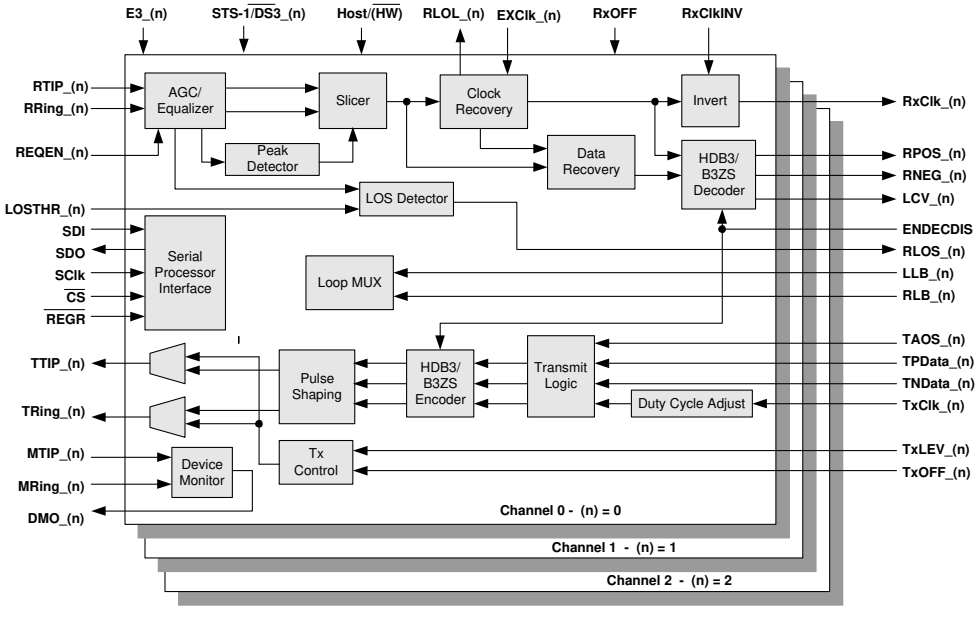
FEATURES

- Incorporates an improved Timing Recovery circuit and is pin and functional compatible to XRT73L03A
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Uses Minimum External components
- Single +3.3V Power Supply
- Low power CMOS design
- 5V tolerant I/O
- -40°C to +85°C Operating Temperature Range
- Available in a 120 pin LQFP package

APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

FIGURE 1. XRT73LC03A BLOCK DIAGRAM



Notes: 1. (n) = 0, 1, or 2 for respective Channels
2. Serial Processor Interface input pins are shared by the three Channels in HOST Mode and redefined in Hardware Mode.

TYPICAL APPLICATIONS

FIGURE 2. MULTICHANNEL ATM APPLICATION

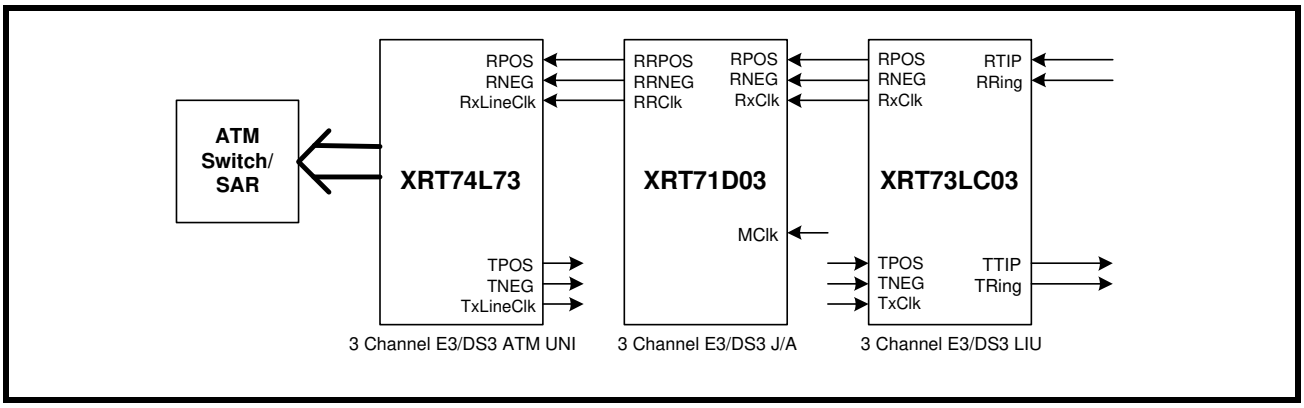
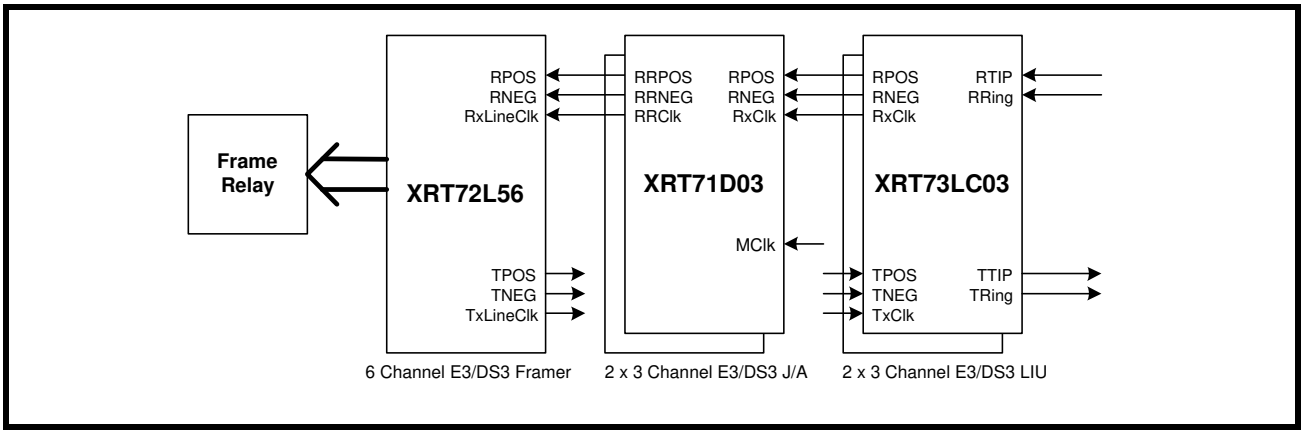


FIGURE 3. MULTISERVICE - FRAME RELAY APPLICATION



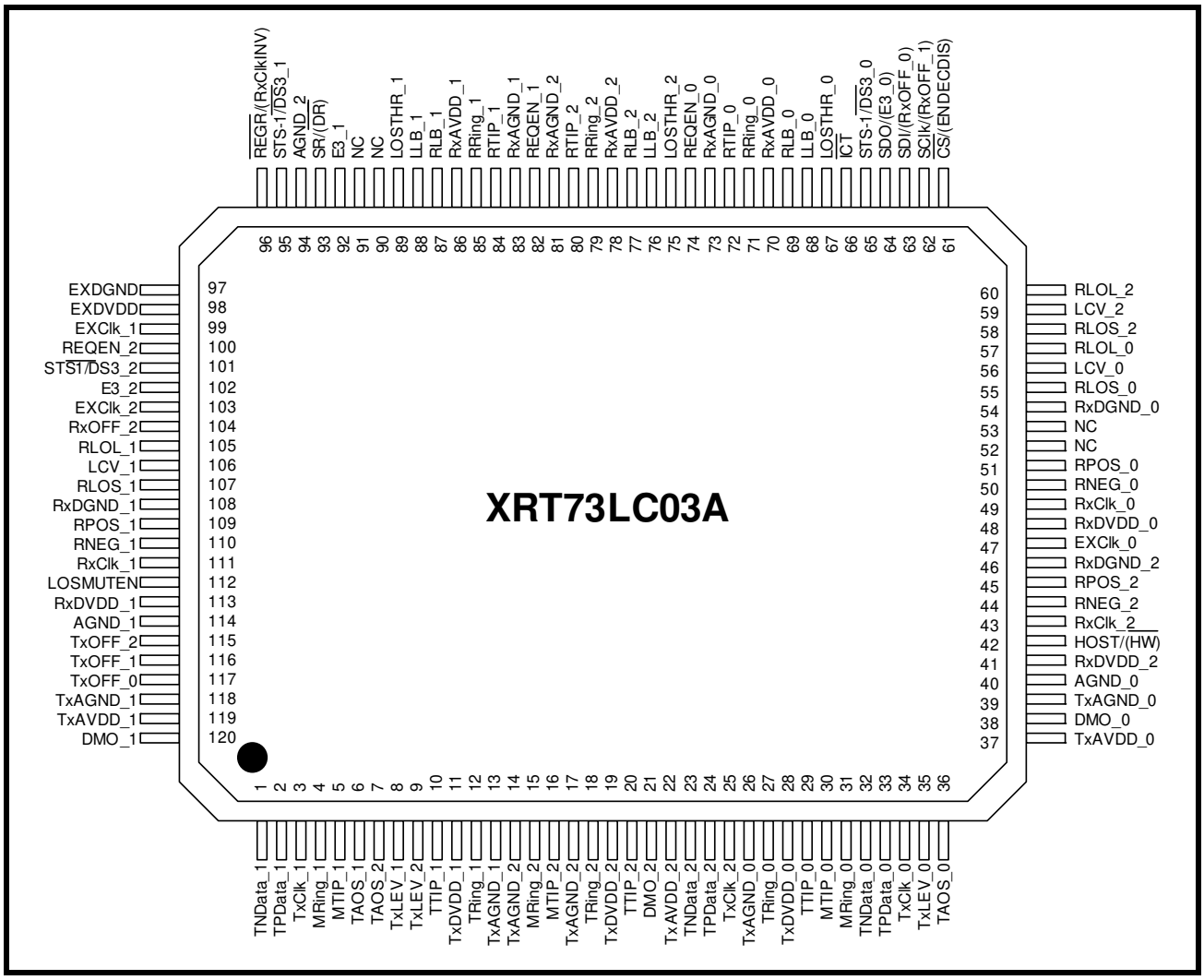
TRANSMIT INTERFACE CHARACTERISTICS:

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal from the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Contains Transmit Clock Duty Cycle Correction Circuit on-chip
- Generates pulses that comply with the ITU-T G.703 pulse template (E3 applications)
- Generates pulses that comply with the DSX-3 pulse template as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS:

- Integrated Adaptive Receive Equalization (optional) and Timing Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements (E3 and DS3 applications)
- Meets Jitter Tolerance Requirements as specified in ITU-T G.823_1993 (E3 Applications)
- Meets Jitter Tolerance Requirements as specified in Bellcore GR-499-CORE (DS3 Applications)
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment
- Receiver can be powered down in order to conserve power in redundancy designs

FIGURE 4. PIN OUT OF THE XRT73LC03A IN THE 120 PIN LQFP PACKAGE



ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73LC03AIV	120 Pin LQFP 14mm X 20mm	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
29 10 20	TTIP_0 TTIP_1 TTIP_2	O	**Transmit TTIP Output - Channel (n):** The XRT73LC03A uses this pin along with TRing_(n) to transmit a bipolar line signal via a 1:1 transformer.
27 12 18	TRing_0 TRing_1 TRing_2	O	**Transmit Ring Output - Channel (n):** The XRT73LC03A uses this pin along with TTIP_(n) to transmit a bipolar line signal via a 1:1 transformer.
34 3 25	TxClk_0 TxClk_1 TxClk_2	I	**Transmit Clock Input for TPData and TNData - Channel (n):** This input pin must be driven at 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications, or 51.84 MHz for SONET STS-1 applications. The XRT73LC03A uses this signal to sample the TPData_(n) and TNData_(n) input pins. By default, the XRT73LC03A is configured to sample these two pins on the falling edge of this signal. ***NOTE:*** *If the XRT73LC03A is operating in the HOST Mode, then the device can be configured to sample the TPData_(n) and TNData_(n) input pins on either the rising or falling edge of TxClk_(n).*
33 2 24	TPData_0 TPData_1 TPData_2	I	**Transmit Positive Data Input - Channel (n)**: The XRT73LC03A samples this pin on the falling edge of TxClk_(n). If the device samples a "1", then it generates and transmits a positive polarity pulse to the line. The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment. ***NOTE:*** *If the XRT73LC03A is operating in the HOST Mode, then the XRT73LC03A can be configured to sample the TPData_(n) pin on either the rising or falling edge of TxClk_(n).*
32 1 23	TNData_0 TNData_1 TNData_2	I	**Transmit Negative Data Input - Channel (n):** The XRT73LC03A samples this pin on the falling edge of TxClk_(n). If the device samples a "1", then it generates and transmits a negative polarity pulse to the line. In Single-Rail Mode, this pin must be tied to GND to enable the HDB3/B3ZS Encoder and Decoder, (internally pulled-down). In Dual-Rail Mode this input is the N-Rail Data input. ***NOTE:*** *If the XRT73LC03A is operating in the HOST Mode, then the XRT73LC03A can be configured to sample the TNData_(n) pin on either the rising or falling edge of TxClk_(n).*

TRANSMIT INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
35 8 9	TxLEV_0 TxLEV_1 TxLEV_2	I	**Transmit Line Build-Out Enable/Disable Select - Channel (n):** This input pin permits the Transmit Line Build-Out circuit within Channel (n) to be enabled or disabled. In E3 mode, this pin has no effect on the transmit pulse shape. Setting this pin to "High" disables the Line Build-Out circuit. In this mode, Channel (n) outputs partially-shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins. Setting this pin to "Low" enables the Line Build-Out circuit within Channel (n). In this mode, Channel (n) outputs shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: **a.** Set this input pin to "1" if the cable length between the Cross-Connect and the transmit output of Channel (n) is greater than 225 feet. **b.** Set this input pin to "0" if the cable length between the Cross-Connect and the transmit output of Channel (n) is less than 225 feet. This pin is active only if the following two conditions are true: **a.** The XRT73LC03A is configured to operate in either the DS3 or SONET STS-1 Modes. **b.** The XRT73LC03A is configured to operate in the Hardware Mode. ***NOTE:*** *This pin to should be tied to GND if the XRT73LC03A is going to be operating in the HOST Mode, (internally pulled-down).*
117 116 115	TxOFF_0 TxOFF_1 TxOFF_2	I	**Transmitter OFF Input - Channel (n):** Setting this input pin "High" turns off all of the Transmitter Sections. In this mode the TTIP and TRing outputs are tri-stated. ***NOTES:*** 1. *This input pin controls the TTIP and TRing outputs even when the XRT73LC03A is operating in the HOST Mode.* 2. *For HOST Mode Operation, this pin is tied to GND if the Transmitter is intended to be turned off via the Microprocessor Serial Interface.*

RECEIVE INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
49 111 43	RxClk_0 RxClk_1 RxClk_2	O	**Receive Clock Output - Channel (n):** This output pin is the Recovered Clock signal from the incoming line signal for Channel (n). The Receive Section of Channel (n) outputs data via the RPOS_(n) and RNEG_(n) output pins on the rising edge of this clock signal. Configure the Receive Section of Channel (n) to update the data on the RPOS_(n) and RNEG_(n) output pins on the falling edge of RxClk_(n) by doing one of the following: **a. Operating in the Hardware Mode** Pull the RxClkINV pin to "High". **b. Operating in the HOST Mode** Write a "1" into the RxClkINV bit-field within the Command Register.
50 110 44	RNEG_0 RNEG_1 RNEG_2	O	**Receive Negative Data Output - Channel (n):** This output pin pulses "High" whenever Channel (n) of the XRT73LC03A has received a Negative Polarity pulse in the incoming line signal at the RTIP_(n)/RRing_(n) inputs. ***NOTE:*** *If the Channel (n) B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
51 109 45	RPOS_0 RPOS_1 RPOS_2	O	**Receive Positive Data Output - Channel (n):** This output pin pulses “High" whenever Channel (n) of the XRT73LC03A has received a Positive Polarity pulse in the incoming line signal at the RTIP_(n)/RRing_(n) inputs. ***NOTE:*** *If the Channel (n) B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
71 85 79	RRing_0 RRing_1 RRing_2	I	**Receive Ring Input - Channel (n):** This input pin along with RTIP_(n) is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
72 84 80	RTIP_0 RTIP_1 RTIP_2	I	**Receive TIP Input - Channel (n):** This input pin along with RRing_(n) is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
74 82 100	REQEN_0 REQEN_1 REQEN_2	I	**Receive Equalization Enable Input - Channel (n):** Setting this input pin "High" enables the Internal Receive Equalizer within Channel (n). Setting this pin "Low" disables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTE:*** *This pin is ignored and should be tied to GND if the XRT73LC03A is going to be operating in the HOST Mode, (internally pulled-down).*

RECEIVE INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
96	$\overline{\text{REGR}}$/ RxClkINV	I	**Register Reset Input (Invert RxClk(n)) Output - Select:** The function of this pin depends upon whether the XRT73LC03A is operating in the HOST Mode or in the Hardware Mode. ***NOTE:*** *This pin is internally pulled "High".* **In the HOST-Mode - Register Reset Input:** Setting this input pin "Low" causes the XRT73LC03A to reset the contents of the Command Registers to their default settings and default operating configuration. **In the Hardware Mode - Invert RxClk Output Select:** Setting this input pin "High" configures the Receive Section of all Channels in the XRT73LC03A to invert their RxClk_(n) clock output signals and configures Channel (n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the falling edge of RxClk_(n). Setting this pin "Low" configures Channel (n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the rising edge of RxClk_(n).

CLOCK INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
47 99 103	EXClk_0 EXClk_1 EXClk_2	I	**External Reference Clock Input - Channel (n):** Apply a 34.368 MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications. The Channel (n) Clock Recovery PLL uses this signal as a Reference Signal for Declaring and Clearing the Receive Loss of Lock Alarm. The Clock recovery PLL also generates the exact clock for the LIU. It is permissible to use the same clock that drives the TxClk_(n) input pin. It is permissible to operate the three Channels at different data rates.

OPERATING MODE SELECT

PIN #	NAME	TYPE	DESCRIPTION
93	SR/($\overline{\text{DR}}$)	I	**Receive Output Single-Rail/Dual-Rail Select:** Setting this pin "High" configures the Receive Sections of all Channels to output data in a Single-Rail Mode to the Terminal Equipment. Setting this pin "Low" configures the Receive Section of all Channels to output data in a Dual-Rail Mode to the Terminal Equipment.

OPERATING MODE SELECT

PIN #	NAME	TYPE	DESCRIPTION
64	SDO/(E3_0)	I/O	**Serial Data Output from the Microprocessor Serial Interface/ E3_Mode Select - Channel 0:** The function of this pin depends on whether the XRT73LC03A is operating in the HOST Mode or in the Hardware Mode. **HOST Mode Operation - Serial Data Output for the Microprocessor Serial Interface:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SClk input signal and tri-stated upon completion of data transfer. **Hardware Mode Operation - E3 Mode Select - Channel 0:** This input pin is used to configure Channel 0 in the XRT73LC03A to operate in the E3 or STS/DS3 Modes. Setting this input pin to "High" configures Channel 0 to operate in the E3 Mode. Setting this input pin to "Low" configures Channel 0 to operate in either the DS3 or STS-1 Modes, depending upon the state of the STS-1/DS3_0 input pin. ***NOTE:*** *This pin is internally pulled "Low" when XRT73LC03A is in the Hardware Mode.*
92 102	E3_1 E3_2	I	**E3 Select Input - Channel (n):** A "High" on this pin configures Channel (n) of the XRT73LC03A to operate in the E3 Mode. A "Low" on this pin configures Channel (n) of the XRT73LC03A to check the state of the STS-1/DS3_(n) input pin ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73LC03A is operating in the HOST Mode.*
65 95 101	STS-1/DS3_0 STS-1/DS3_1 STS-1/DS3_2	I	**STS-1/DS3 Select Input - Channel (n):** "High" for STS-1 and "Low" for DS3 Operation. The XRT73LC03A ignores this pin if the E3_(n) pin is set to "1". This input pin is ignored if the XRT73LC03A is operating in the HOST Mode. ***NOTE:*** *This pin should be tied to GND if the XRT73LC03A is going to be operating in the HOST Mode, (internally pulled-down).*
42	HOST/(HW)	I	**HOST/Hardware Mode Select:** This input pin is used to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SClk, and CS pins). Setting this input pin "High" enables the Microprocessor Serial Interface (e.g. configures the XRT73LC03A to operate in the HOST Mode). In this mode, configure the XRT73LC03A via the Microprocessor Serial Interface. When the XRT73LC03A is operating in the HOST Mode, then it ignores the states of many of the discrete input pins. Setting this input pin "Low" disables the Microprocessor Serial Interface (e.g., configures the XRT73LC03A to operate in the Hardware Mode). In this mode, many of the external input control pins are functional.

CONTROL AND ALARM INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
31 4 15	MRing_0 MRing_1 MRing_2	I	**Monitor Ring Input - Channel (n):** The bipolar line output signal from TRing_(n) can be connected to this pin via a 270-ohm resistor in order to check for line driver failure. This pin is internally pulled "High".
30 5 16	MTIP_0 MTIP_1 MTIP_2	I	**Monitor Tip Input - Channel (n):** The bipolar line output signal from TTIP_(n) can be connected to this pin via a 270-ohm resistor in order to check for line driver failure. This pin is internally pulled "High".
38 120 21	DMO_0 DMO_1 DMO_2	O	**Drive Monitor Output - Channel (n):** If no transmitted AMI signal is present on MTIP_(n) and MRing_(n) input pins for 128±32 TxClk periods, then DMO_(n) toggles and remains "High" until the next AMI signal is detected.
36 6 7	TAOS_0 TAOS_1 TAOS_2	I	**Transmit All Ones Select - Channel (n):** A "High" on this pin causes the Transmit Section, within Channel (n), to generate and transmit a continuous AMI all “1’s" pattern onto the line. The frequency of this "1’s" pattern is determined by TxClk_(n). This input pin is ignored if the XRT73LC03A is operating in the HOST Mode. ***NOTE:*** *This pin should be tied to GND if the XRT73LC03A is going to be operating in the HOST Mode, (internally pulled-down).*
55 107 58	RLOS_0 RLOS_1 RLOS_2	O	**Receive Loss of Signal Output Indicator - Channel (n):** This output pin toggles "High" if Channel (n) has detected a Loss of Signal Condition in the incoming line signal. The criteria that the XRT73LC03A uses to declare an LOS Condition depends upon whether the device is operating in the E3 or STS-1/DS3 Mode.
57 105 60	RLOL_0 RLOL_1 RLOL_2	O	**Receive Loss of Lock Output Indicator - Channel (n):** This output pin toggles "High" if Channel (n) has detected a Loss of Lock Condition. Channel (n) declares an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXClk(n) input pin) by more than 0.5%.
56 106 59	LCV_0 LCV_1 LCV_2	O	**Line Code Violation Indicator - Channel 0:** Whenever the Receive Section of Channel (n) detects a Line Code Violation, it pulses this output pin "High". This output pin remains "Low" at all other times. ***NOTE:*** *The XRT73LC03A outputs an NRZ pulse via this output pin. It is advisable to sample this output pin via the RxClk_(n) clock output signal.*
66	$\overline{\text{ICT}}$	I	**In-Circuit Test Input**: Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. This pin should be set to "High" for normal operation. This pin is internally pulled "High".
67 89 75	LOSTHR_0 LOSTHR_1 LOSTHR_2	I	**Loss of Signal Threshold Control - Channel (n)**: Forcing the LOSTHR_(n) pin to GND or VDD provides two settings. This pin must be set to a “High” or “Low” level upon power up and should not be changed during operation. This pin is only applicable during DS3 or STS-1 operations.

CONTROL AND ALARM INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
68 88 76	LLB_0 LLB_1 LLB_2	I	**Local Loop-back - Channel (n)**: This input pin along with RLB_(n) dictates which Loop-Back mode Channel (n) is operating in. A "High" on this pin with RLB_(n) set to "Low" configures Channel (n) to operate in the Analog Local Loop-Back Mode. A "High" on this pin with RLB_(n) also being set to "High" configures Channel (n) to operate in the Digital Local Loop-Back Mode. ***NOTE:*** *This pin is ignored and should be tied to GND if the XRT73LC03A is going to be operating in the HOST Mode.*
69 87 77	RLB_0 RLB_1 RLB_2	I	**Remote Loop-Back - Channel (n):** This input pin in conjunction with LLB_(n) dictates which Loop-Back mode Channel (n) is operating in. A "High" on this pin with LLB_(n) being set to "Low" configures Channel (n) to operate in the Remote Loop-Back Mode. A "High" on this pin with LLB_(n) also being set to "High" configures Channel (n) to operate in the Digital Local Loop-Back Mode. ***NOTE:*** *This pin is ignored and should be tied to GND if the XRT73LC03A is going to be operating in the HOST Mode.*
112	LOSMUTEN	I	**MUTE-upon-LOS Enable Input (Hardware Mode):** This input pin is use to configure the XRT73LC03A, while it is operating in the Hardware Mode, to Mute the recovered data via the RPOS_(n), RNEG_(n) output pins whenever one of the Channels declares an LOS conditions. Setting this input pin “High" configures all Channels to automatically pull the RPOS_(n) and RNEG_(n) output pins “Low” whenever it is declaring an LOS condition, thereby Muting the data being output to the Terminal Equipment. Setting this input pin "Low" configures all Channels to NOT automatically Mute the recovered data whenever an LOS condition is declared. ***NOTES:*** *This pin is ignored and should be tied to GND if the XRT73LC03A is going to be operating in the HOST Mode. This pin is internally pulled "Low".*

MICROPROCESSOR INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
61	$\overline{CS}$/ (ENDECDIS)	I	**Microprocessor Serial Interface - Chip Select Input/Encoder-Decoder Disable Input:** This pin's functionality depends on whether the XRT73LC03A is operating in the HOST or Hardware Mode. **HOST Mode - Chip Select Input** The Local Microprocessor must assert this pin (set it to "0") in order to enable communication with the XRT73LC03A via the Microprocessor Serial Interface. ***NOTE:*** *This pin is internally pulled "High".* **Hardware Mode - Encoder/Decoder Disable Input** Setting this input pin "High" disables the B3ZS/HDB3 Encoder & Decoder blocks in the XRT73LC03A and configures it to transmit and receive the line signal in an AMI format. Setting this input pin "Low" enables the B3ZS/HDB3 Encoder & Decoder blocks and configures it to ransmit and receive the line signal in the B3ZS format for STS-1/DS3 operation or in the HDB3 format for E3 operation. ***NOTE:*** *If the XRT73LC03A is operating in the Hardware Mode, this pin setting configures the B3ZS/HDB3 Encoder and Decoder Blocks for all Channels.*
63	SDI/(RxOFF_0)	I	**Serial Data Input for the Microprocessor Serial Interface/Receiver Shut OFF Input - Channel 0:** The function of this input pin depends on whether the XRT73LC03A is operating in the HOST Mode or in the Hardware Mode. **HOST Mode - Serial Data Input for the Microprocessor Serial Interface:** To read or write data into the Command Registers over the Microprocessor Serial Interface, apply the Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations to this pin. This input is sampled on the rising edge of the SClk pin. **Hardware Mode - Channel 0 Receiver Shut OFF Input:** Setting this input pin "High" shuts off the Channel 0 receiver. Setting this input pin "Low" enables the Receive Section for full operation.
62	SClk/(RxOFF_1)	I	**Microprocessor Serial Interface Clock Signal/Receiver Shut OFF Input - Channel 1:** The function of this pin depends on whether the XRT73LC03A is operating in the HOST Mode or in the Hardware Mode. **HOST Mode - Microprocessor Serial Interface Clock Signal:** This signal is used to sample the data on the SDI pin on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. **Hardware Mode - Receiver Shut OFF input - Channel 1:** Setting this input pin "High" shuts off the Channel 1 receiver. Setting this input pin "Low" enables the Receive Section for full operation.

MICROPROCESSOR INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
104	RxOFF_2	I	**Receiver Shut OFF Input - Channel 2:** **Hardware Mode - Receiver Shut OFF Input - Channel 2:** Setting this input pin "High" shuts off the Receive Section in Channel 2. Setting this input pin "Low" enables the Receive Section for full operation.
96	$\overline{\text{REGR}}$/ RxClkINV	I	**Register Reset Input pin (Invert RxClk(n)) Output - Select):** The function of this pin depends upon whether the XRT73LC03A is operating in the HOST Mode or in the Hardware Mode. ***NOTE:*** *This pin is internally pulled "High".* **In the HOST-Mode - Register Reset Input:** Setting this input pin "Low" causes the XRT73LC03A to reset the contents of the Command Registers to their default settings and default operating configuration. **In the Hardware Mode - Invert RxClk Output Select:** Setting this input pin "High" configures the Receive Section of all Channels in the XRT73LC03A to invert their RxClk_(n) clock output signals and configures Channel (n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the falling edge of RxClk_(n). Setting this pin "Low" configures Channel (n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the rising edge of RxClk_(n).

POWER AND GROUND PINS

PIN #	NAME	TYPE	DESCRIPTION
11	TxDVDD_1	****	**Transmitter Digital Supply, 3.3V ± 5% - Channel(n)**
13	TxAGND_1	****	**Transmitter Analog Ground - Channel(n)**
14	TxAGND_2	****	**Transmitter Analog Ground - Channel(n)**
17	TxAGND_2	****	**Transmitter Analog Ground - Channel(n)**
19	TxDVDD_2	****	**Transmitter Digital Supply, 3.3V ± 5% - Channel(n)**
22	TxAVDD_2	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
26	TxAGND_0	****	**Transmitter Analog Ground - Channel(n)**
28	TxDVDD_0	****	**Transmitter Digital Supply, 3.3V ± 5% - Channel(n)**
37	TxAVDD_0	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
39	TxAGND_0	****	**Transmitter Analog Ground - Channel (n)**
40	AGND_0	****	**Analog Ground - Channel (n)**
41	RxDVDD_2	****	**Receiver Digital Supply 3.3V ± 5% Channel (n)**
46	RxDGND_2	****	**Receiver Digital Ground - Channel(n)**
48	RxDVDD_0	****	**Receiver Digital Supply 3.3V ± 5% Channel (n)**
54	RxDGND_0	****	**Receiver Digital Ground - Channel(n)**
70	RxAVDD_0	****	**Receiver Analog Supply 3.3V ± 5% Channel (n)**
73	RxAGND_0	****	**Reciever Analog Ground Channel (n)**
78	RxAVDD_2	****	**Receiver Analog Supply 3.3V ± 5% - Channel (n)**
81	RxAGND_2	****	**Receiver Analog Ground - Channel (n)**
83	RxAGND_1	****	**Receiver Analog Ground - Channel (n)**
86	RxAVDD_1	****	**Receiver Analog Supply 3.3V ± 5% - Channel (n)**
94	AGND_2	****	**Analog Ground - Channel (n)**
97	EXDGND	****	**External Reference Clock Ground**
98	EXDVDD	****	**External Reference Clock Power Supply**
108	RxDGND_1	****	**Receiver Digital Ground - Channel(n)**
113	RxDVDD_1	****	**Receiver Digital Supply 3.3V ± 5% Channel (n)**
114	AGND_1	****	**Analog Ground - Channel (n)**
118	TxAGND_1	****	**Transmitter Analog Ground - Channel(n)**
119	TxAVDD_1	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**

NO CONNECTION PINS

PIN #	NAME	TYPE	DESCRIPTION
52	NC		No connection
53	NC		No connection
90	NC		No connection
91	NC		No connection

ELECTRICAL CHARACTERISTICS E

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	- 65°C to + 150°C
Operating Temperature	- 40°C to + 85°C
Supply Voltage Range	-0.5V to +3.465V
Theta-JA	22.2° C/W
Theta-JC	4.0° C/W

NOTE: *The XRT73LC03A is assembled in a thermally enhanced package that uses an integral Aluminum Oxide heat spreader.*

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DC Electrical Characteristics					
DV_{DD}	Digital DC Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog DC Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all "1's") ***NOTE:*** V_{DD} = 3.465V			350	mA
V_{IL}	Input Low Voltage *			0.8	V
V_{IH}	Input High Voltage *	2.0		5.0	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA *			0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA *	2.8			V
I_L	Input Leakage Current *			±10	µA

NOTE: ** Not applicable to pins with pull-up or pull-down resistors.*

ELECTRICAL CHARACTERISTICS (CONTINUED) (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

AC ELECTRICAL CHARACTERISTICS (SEE FIGURE 5)					
TERMINAL SIDE TIMING PARAMETERS (SEE FIGURE 6 AND FIGURE 7) -- {(n) = 0, 1 OR 2 }					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
	TxClk_(n) Clock Duty Cycle (STS-1/DS3)	30	50	70	%
	TxClk_(n) Clock Duty Cycle (E3)	30	50	70	%
	TxClk_(n) Frequency (SONET STS-1)		51.84		MHz
	TxClk_(n) Frequency (DS3)		44.736		MHz
	TxClk_(n) Frequency (E3)		34.368		MHz
t_{RTX}	TxClk_(n) Clock Rise Time (10% to 90%)		3	5	ns
t_{FTX}	TxClk_(n) Clock Fall Time (90% to 10%)		3	5	ns
t_{TSU}	TPData_(n)/TNData_(n) to TxClk_(n) Falling Set up time	3	1.5		ns
t_{THO}	TPData_(n)/TNData_(n) to TxClk_(n) Falling Hold time	3	1.5		ns
t_{LCVO}	RxClk_(n) to rising edge of LCV_(n) output delay		2.5		ns
t_{TDY}	TTIP_(n)/TRing_(n) to TxClk_(n) Rising Propagation Delay time		8		ns
	RxClk_(n) Clock Duty Cycle		50		%
	RxClk_(n) Frequency (SONET STS-1)		51.84		MHz
	RxClk_(n) Frequency (DS3)		44.736		MHz
	RxClk_(n) Frequency (E3)		34.368		MHz
t_{CO}	RxClk_(n) to RPOS_(n)/RNEG_(n) Delay Time	0	2.5		ns
t_{RRX}	RxClk_(n) Clock Rise Time (10% to 90%)		1.5		ns
t_{FRX}	RxClk_(n) Clock Fall Time (10% to 90%)		1.5		ns
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *All XRT73LC03A digital inputs are designed to be TTL 5V compliant.*
2. *All XRT73LC03A digital outputs are also TTL 5V compliant. However, these outputs will not drive to 5V nor will they accept external 5V pull-ups.*

FIGURE 5. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES (TYPICAL CHANNEL)

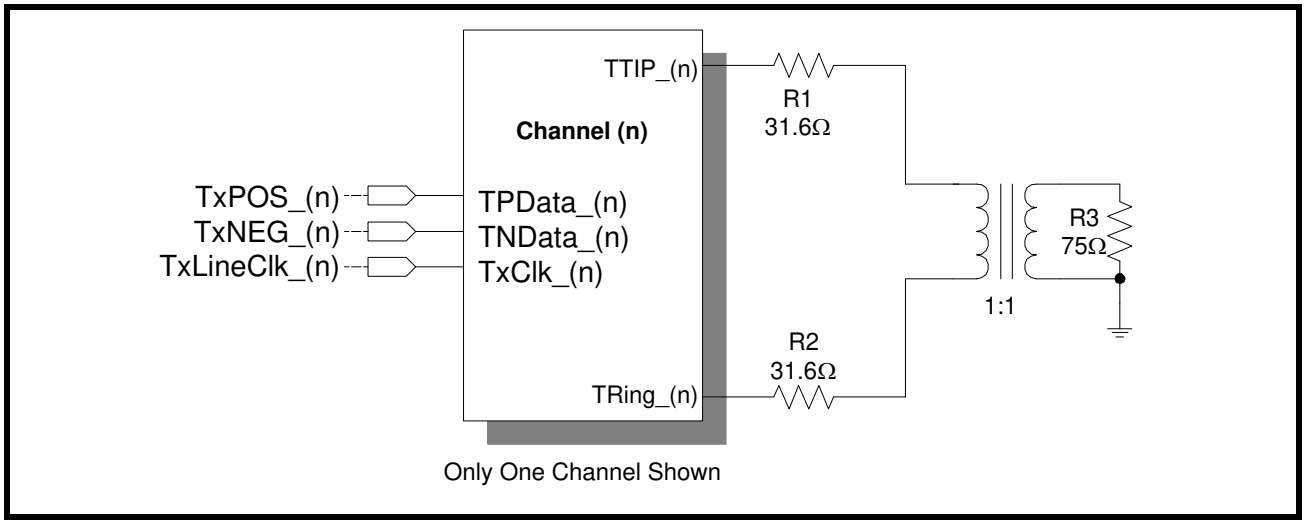


FIGURE 6. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE

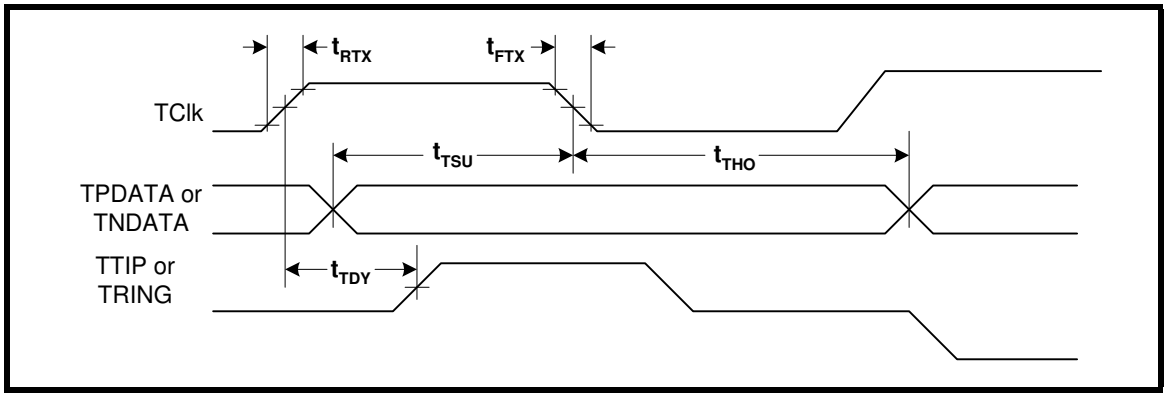
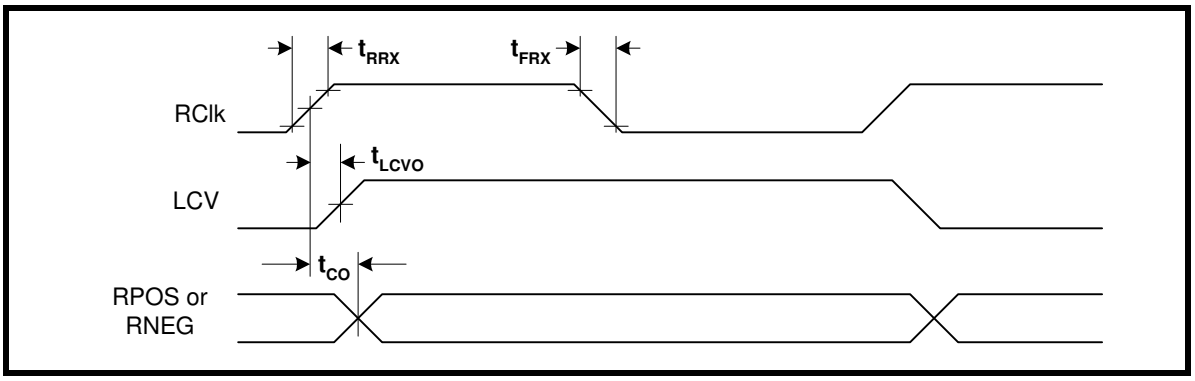


FIGURE 7. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE



ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS E3 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 5)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer)	0.90	1.00	1.10	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	1200	1400		feet
	Interference Margin	-20	-15		dB
	Signal Level to Declare Loss of Signal			-35	dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10		255	UI
	Termination of LOS to LOS Clearance Time	10		255	UI
	Intrinsic Jitter (all “1’s” pattern)		0.02		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	30			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	4			UI
	Jitter Tolerance @ Jitter Frequency = 800kHz	0.15	0.20		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS SONET STS-1 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 5)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Transmit Output Pulse Amplitude (Measured with TxLEV=0)	0.65	0.75	0.90	Vpk
	Transmit Output Pulse Amplitude (Measured with TxLEV=1)	0.90	1.00	1.10	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UI
Receive Line Characteristics					
	Receive Sensitivity (Length of Cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (see Table 5)				mV
	Intrinsic Jitter (all “1’s” pattern)		0.02		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 400kHz	0.15	0.35		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS DS3 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 5)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=0)	0.65	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=1)	0.90	1.00	1.10	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UI
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (see Table 5)		70		mV
	Intrinsic Jitter (all “1’s” pattern)		0.02		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 300kHz (Cat II)	0.35	0.45		UI

Figure 8, Figure 9 and Figure 10 present the Pulse Template requirements for the E3, DS3 and STS-1 Rates.

FIGURE 8. ITU-T G.703 TRANSMIT OUTPUT PULSE TEMPLATE FOR E3 APPLICATIONS

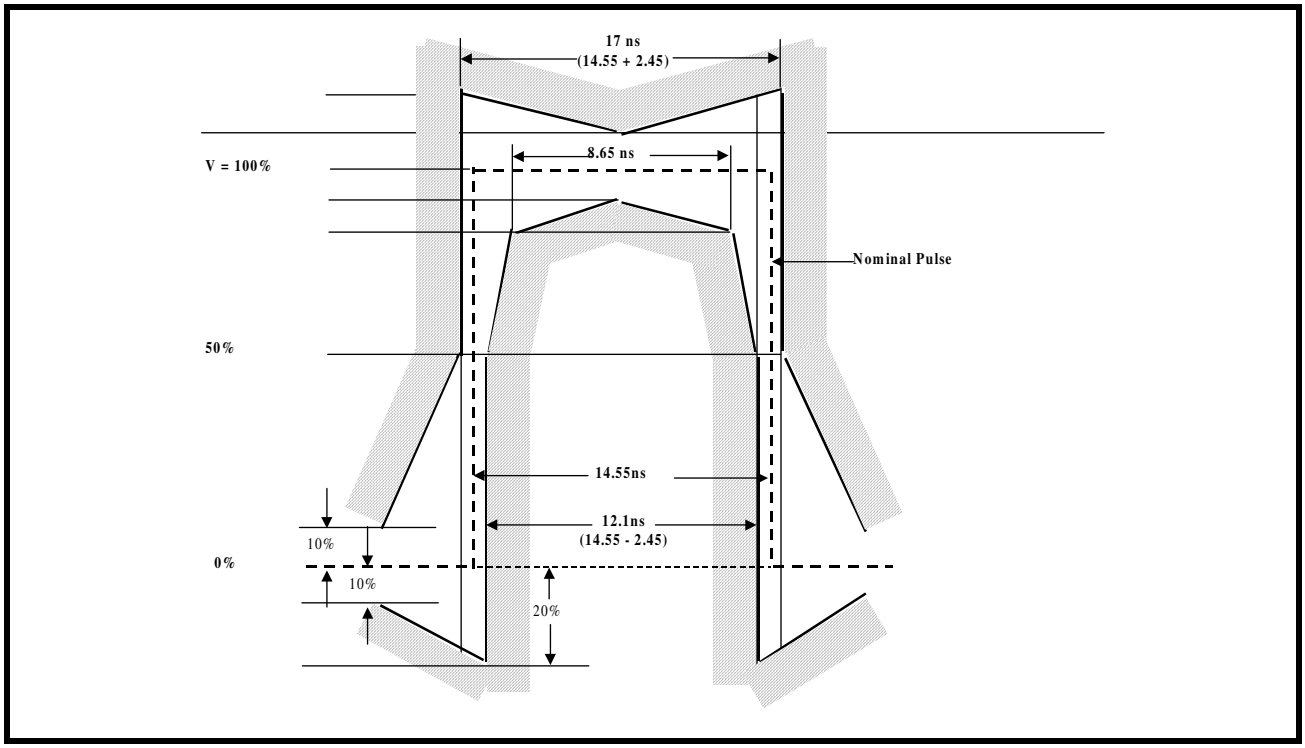


FIGURE 9. BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

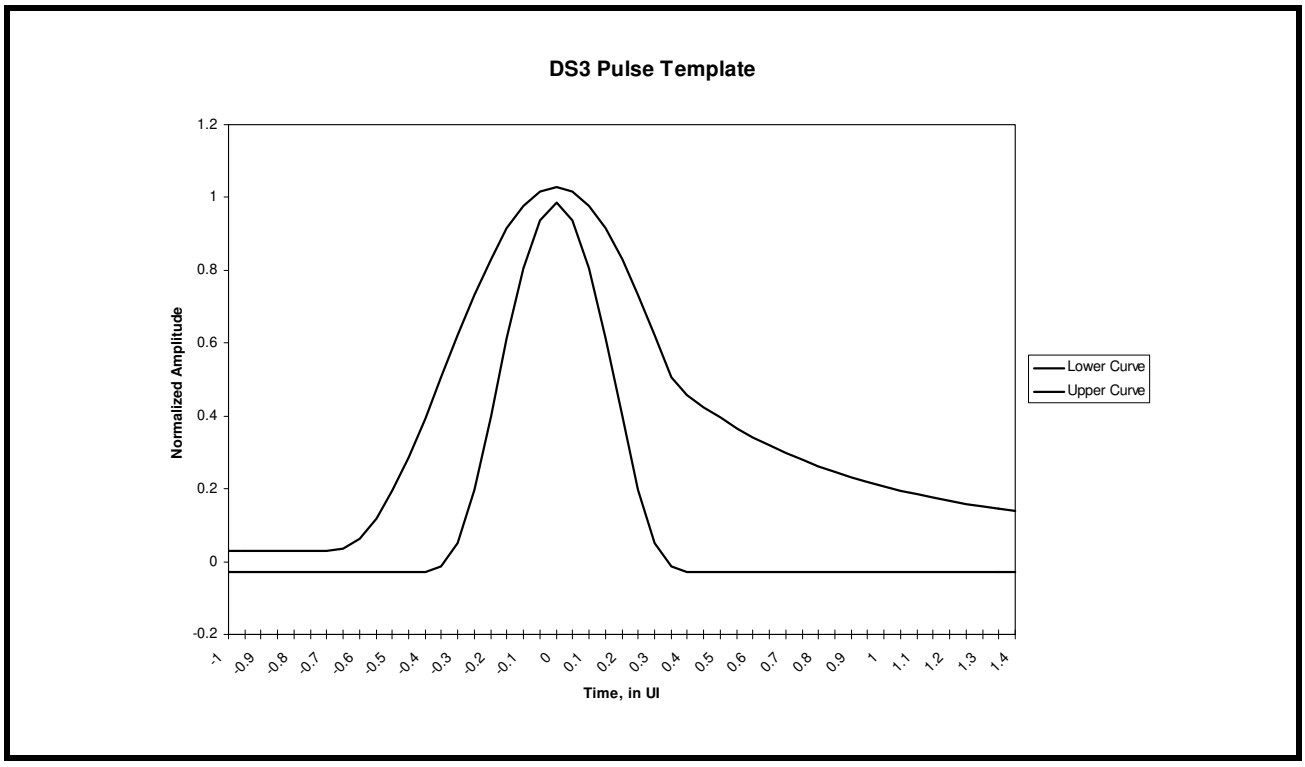


FIGURE 10. BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

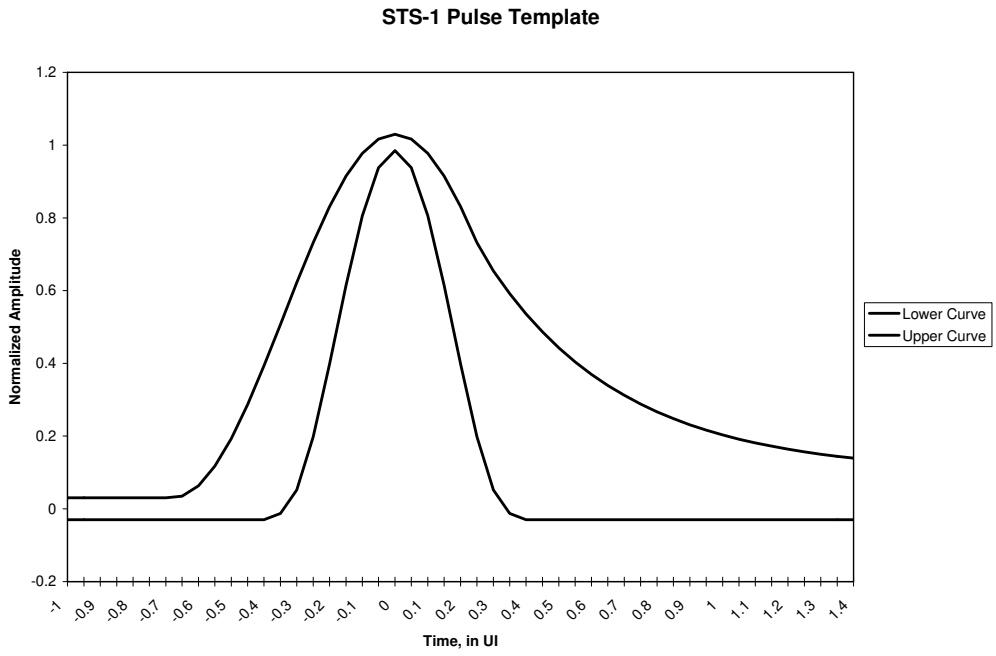
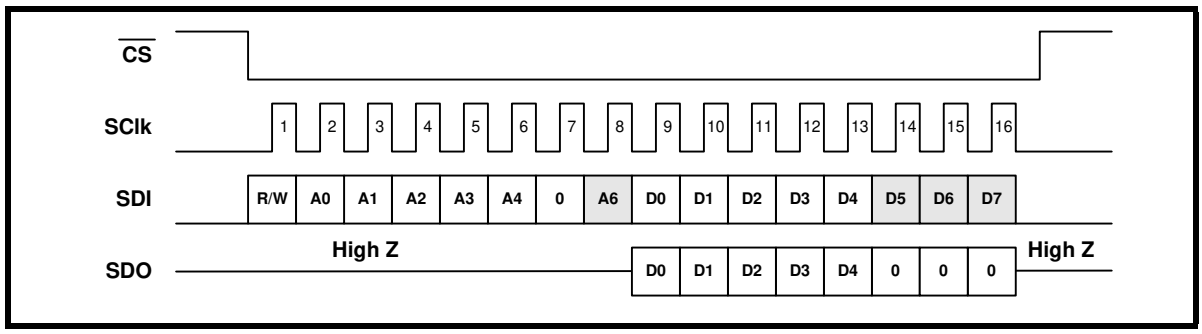


FIGURE 11. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

1. *A5 is always "0".*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*
4. *A shaded pulse, denotes a "don't care" value.*

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

MICROPROCESSOR SERIAL INTERFACE TIMING (SEE FIGURE 12)					
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk Setup Time	5			ns
t_{22}	SCLK Falling Edge to $\overline{CS}$ Low Assertion Time	5			ns
t_{23}	SDI to Rising Edge of SClk Setup Time	5			ns
t_{24}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{25}	SClk "Low" Time	65	80		ns
t_{26}	SClk "High" Time	65	80		ns
t_{27}	SClk Period	160			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SClk Hold Time	5			ns
t_{29}	$\overline{CS}$ "Inactive" Time	160			ns
t_{30}	Falling Edge of SClk to SDO Valid Time			80	ns
t_{31}	Falling Edge of SClk to SDO Invalid Time			65	ns
t_{32}	Rising edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			20	ns

NOTE: *The load is 10pF*

FIGURE 12. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE