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**GENERAL DESCRIPTION**

The XRT73R06 is a six channel fully integrated Line Interface Unit (LIU) featuring EXAR's R<sup>3</sup> Technology (Reconfigurable, Relayless, Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 6 independent Receivers, Transmitters and Jitter Attenuators in a single 217 Lead BGA package.

Each channel of the XRT73R06 can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT73R06's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12 dB of cable attenuation.

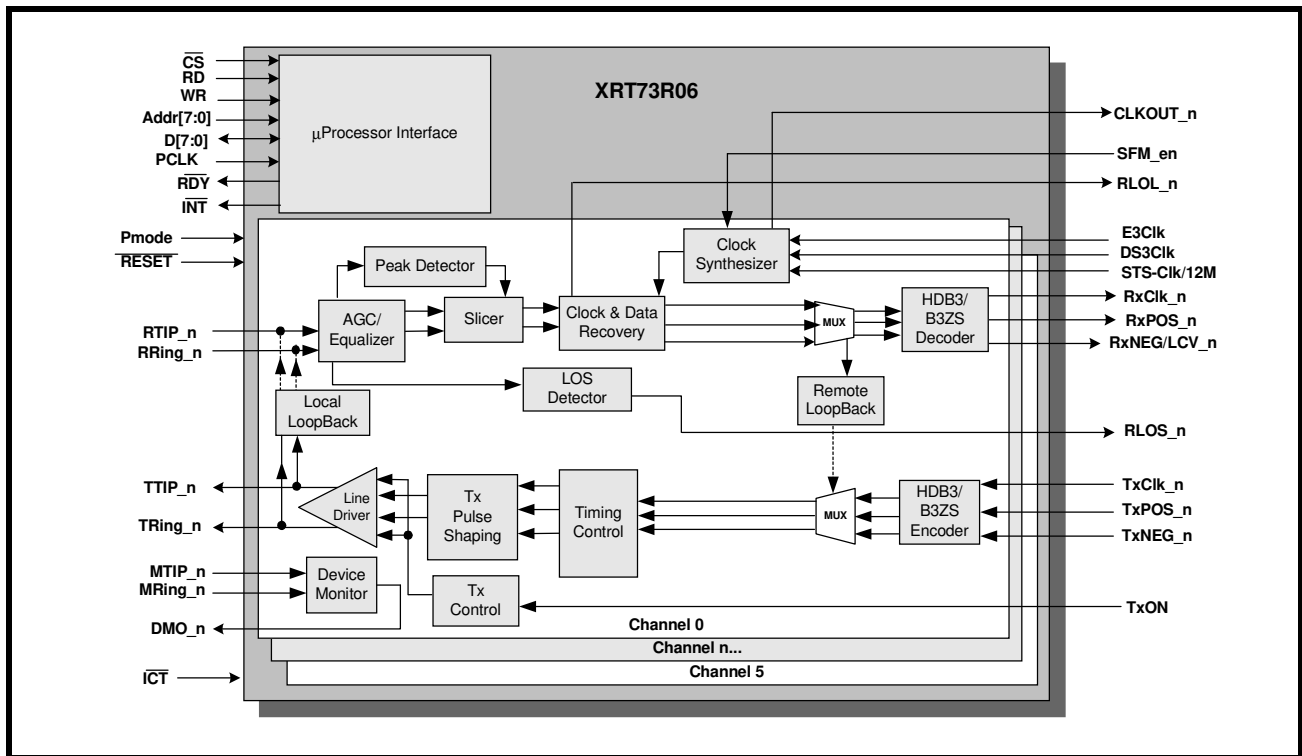
The XRT73R06 provides a Parallel Microprocessor Interface for programming and control.

The XRT73R06 supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

**APPLICATIONS**

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

**FIGURE 1. BLOCK DIAGRAM OF THE XRT 73R06**



**ORDERING INFORMATION**

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73R06IB	217 Lead BGA	-40°C to +85°C

## FEATURES

### RECEIVER

- R<sup>3</sup> Technology (Reconfigurable, Relayless, Redundancy)
- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

### TRANSMITTER

- R<sup>3</sup> Technology (Reconfigurable, Relayless, Redundancy)
- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be independently turned on or off
- Transmitters provide Voltage Output Drive

### CONTROL AND DIAGNOSTICS

- Parallel Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring
- Each channel supports Analog, Remote and Digital Loop-backs
- Single 3.3 V  $\pm$  5% power supply
- 5 V Tolerant digital inputs
- Available in 217 pin BGA Package

- - 40°C to 85°C Industrial Temperature Range

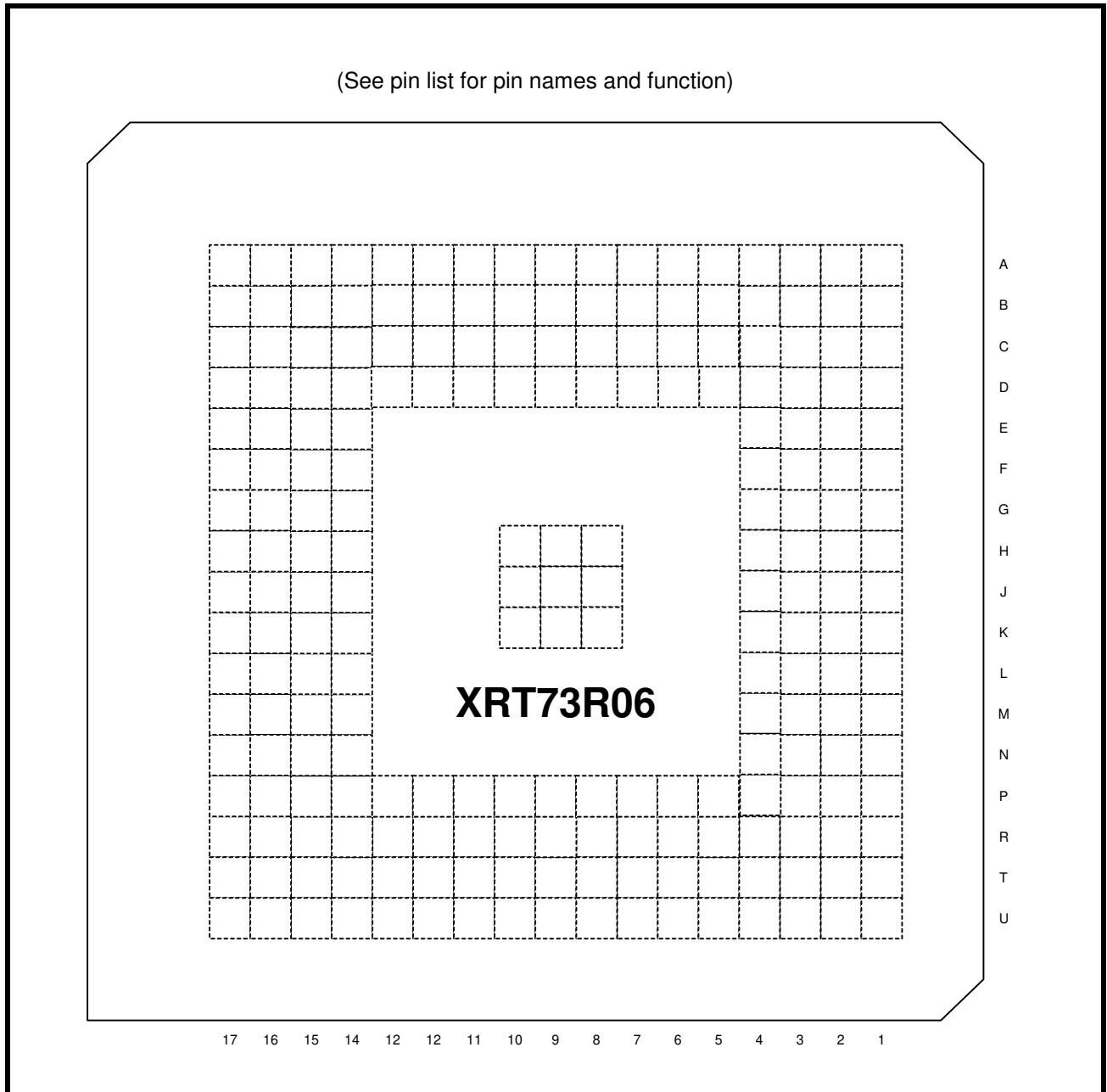
### TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102\_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

### RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823\_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Lock (LOL) Alarm
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

FIGURE 2. XRT73R06 IN BGA PACKAGE (BOTTOM VIEW)



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**PIN DESCRIPTIONS (BY FUNCTION)**
**TRANSMIT INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION															
T15 R16 R15 N14 P14 P13	TxON_0 TxON_1 TxON_2 TxON_3 TxON_4 TxON_5	I	<p><b>Transmitter ON Input - Channel 0:</b>  <b>Transmitter ON Input - Channel 1:</b>  <b>Transmitter ON Input - Channel 2:</b>  <b>Transmitter ON Input - Channel 3:</b>  <b>Transmitter ON Input - Channel 4:</b>  <b>Transmitter ON Input - Channel 5:</b></p> <p>These pins are active only when the corresponding TxON bits are set.                      Table below shows the status of the transmitter based on the TxON bit and TxON pin settings.</p> <table border="1" data-bbox="748 716 1297 953"> <thead> <tr> <th>Bit</th> <th>Pin</th> <th>Transmitter Status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>1</td> <td>ON</td> </tr> </tbody> </table> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. These pins will be active and can control the TTIP and TRING outputs only when the TxON_n bits in the channel register are set.</li> <li>2. When Transmitters are turned off the TTIP and TRING outputs are Tri-stated.</li> <li>3. These pins are internally pulled up.</li> </ol>	Bit	Pin	Transmitter Status	0	0	OFF	0	1	OFF	1	0	OFF	1	1	ON
Bit	Pin	Transmitter Status																
0	0	OFF																
0	1	OFF																
1	0	OFF																
1	1	ON																
E3 M3 F15 P16 G3 H15	TxCLK_0 TxCLK_1 TxCLK_2 TxCLK_3 TxCLK_4 TxCLK_5	I	<p><b>Transmit Clock Input for TPOS and TNEG - Channel 0:</b>  <b>Transmit Clock Input for TPOS and TNEG - Channel 1:</b>  <b>Transmit Clock Input for TPOS and TNEG - Channel 2:</b>  <b>Transmit Clock Input for TPOS and TNEG - Channel 3:</b>  <b>Transmit Clock Input for TPOS and TNEG - Channel 4:</b>  <b>Transmit Clock Input for TPOS and TNEG - Channel 5:</b></p> <p>The frequency accuracy of this input clock must be of nominal bit rate <math>\pm 20</math> ppm.                      The duty cycle can be 30%-70%.                      By default, input data is sampled on the falling edge of TxCLK.</p>															



**TRANSMIT INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
F2 P2 G15 R17 H3 K15	TNEG_0 TNEG_1 TNEG_2 TNEG_3 TNEG_4 TNEG_5	I	<p><b>Transmit Negative Data Input - Channel 0:</b>  <b>Transmit Negative Data Input - Channel 1:</b>  <b>Transmit Negative Data Input - Channel 2:</b>  <b>Transmit Negative Data Input - Channel 3:</b>  <b>Transmit Negative Data Input - Channel 4:</b>  <b>Transmit Negative Data Input - Channel 5:</b></p> <p>In Dual-rail mode, these pins are sampled on the falling or rising edge of TxCLK_n.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>These input pins are ignored and must be grounded if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.</li> </ol>
F3 N3 F16 P15 G2 J15	TPOS_0 TPOS_1 TPOS_2 TPOS_3 TPOS_4 TPOS_5	I	<p><b>Transmit Positive Data Input - Channel 0:</b>  <b>Transmit Positive Data Input - Channel 1:</b>  <b>Transmit Positive Data Input - Channel 2:</b>  <b>Transmit Positive Data Input - Channel 3:</b>  <b>Transmit Positive Data Input - Channel 4:</b>  <b>Transmit Positive Data Input - Channel 5:</b></p> <p>By default sampled on the falling edge of TxCLK.</p>
D1 N1 D17 N17 H1 H17	TTIP_0 TTIP_1 TTIP_2 TTIP_3 TTIP_4 TTIP_5	O	<p><b>Transmit TTIP Output - Channel 0:</b>  <b>Transmit TTIP Output - Channel 1:</b>  <b>Transmit TTIP Output - Channel 2:</b>  <b>Transmit TTIP Output - Channel 3:</b>  <b>Transmit TTIP Output - Channel 4:</b>  <b>Transmit TTIP Output - Channel 5:</b></p> <p>These pins along with TRING transmit bipolar signals to the line using a 1:1 transformer.</p>
E1 M1 E17 M17 J1 J17	TRING_0 TRING_1 TRING_2 TRING_3 TRING_4 TRING_5	O	<p><b>Transmit Ring Output - Channel 0:</b>  <b>Transmit Ring Output - Channel 1:</b>  <b>Transmit Ring Output - Channel 2:</b>  <b>Transmit Ring Output - Channel 3:</b>  <b>Transmit Ring Output - Channel 4:</b>  <b>Transmit Ring Output - Channel 5:</b></p> <p>These pins along with TTIP transmit bipolar signals to the line using a 1:1 transformer.</p>

**RECEIVE INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
A2 U2 A17 U17 D8 P8	RxCLK_0 RXCLK_1 RxCLK_2 RxCLK_3 RxCLK_4 RxCLK_5	○	<p><b>Receive Clock Output - Channel 0:</b>  <b>Receive Clock Output - Channel 1:</b>  <b>Receive Clock Output - Channel 2:</b>  <b>Receive Clock Output - Channel 3:</b>  <b>Receive Clock Output - Channel 4:</b>  <b>Receive Clock Output - Channel 5:</b></p> <p>By default, RPOS and RNEG data sampled on the rising edge RxCLK..  Set the RxCLKINV bit to sample RPOS/RNEG data on the falling edge of RxCLK</p>
A1 U1 A16 U16 D9 P9	RPOS_0 RPOS_1 RPOS_2 RPOS_3 RPOS_4 RPOS_5	○	<p><b>Receive Positive Data Output - Channel 0:</b>  <b>Receive Positive Data Output - Channel 1:</b>  <b>Receive Positive Data Output - Channel 2:</b>  <b>Receive Positive Data Output - Channel 3:</b>  <b>Receive Positive Data Output - Channel 4:</b>  <b>Receive Positive Data Output - Channel 5:</b></p> <p><i>NOTE: If the B3ZS/HDB3 Decoder is enabled in Single-rail mode, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are removed and replaced with '0'.</i></p>
B2 T2 B16 T16 D10 P10	RNEG_0/ LCV_0 RNEG_1/ LCV_1 RNEG_2/ LCV_2 RNEG_3/ LCV_3 RNEG_4/ LCV_4 RNEG_5/ LCV_5	○	<p><b>Receive Negative Data Output/Line Code Violation Indicator - Channel 0:</b>  <b>Receive Negative Data Output/Line Code Violation Indicator - Channel 1:</b>  <b>Receive Negative Data Output/Line Code Violation Indicator - Channel 2:</b>  <b>Receive Negative Data Output/Line Code Violation Indicator - Channel 3:</b>  <b>Receive Negative Data Output/Line Code Violation Indicator - Channel 4:</b>  <b>Receive Negative Data Output/Line Code Violation Indicator - Channel 5:</b></p> <p>In Dual Rail mode, a negative pulse is output through RNEG.</p> <p><b>Line Code Violation Indicator - Channel n:</b>  If configured in Single Rail mode then Line Code Violation will be output.</p>

**RECEIVE INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
A5 U5 A14 U14 A9 U9	RRING_0 RRING_1 RRING_2 RRING_3 RRING_4 RRING_5	I	<b>Receive Input - Channel 0:</b> <b>Receive Input - Channel 1:</b> <b>Receive Input - Channel 2:</b> <b>Receive Input - Channel 3:</b> <b>Receive Input - Channel 4:</b> <b>Receive Input - Channel 5:</b> These pins along with RTIP receive the bipolar line signal from the remote DS3/E3/STS-1 Terminal.
A6 U6 A13 U13 A10 U10	RTIP_0 RTIP_1 RTIP_2 RTIP_3 RTIP_4 RTIP_5	I	<b>Receive Input - Channel 0:</b> <b>Receive Input - Channel 1:</b> <b>Receive Input - Channel 2:</b> <b>Receive Input - Channel 3:</b> <b>Receive Input - Channel 4:</b> <b>Receive Input - Channel 5:</b> These pins along with RRING receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.

**CLOCK INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
E15	E3CLK	I	<p><b>E3 Clock Input (34.368 MHz ± 20 ppm):</b> If any of the channels is configured in E3 mode, a reference clock 34.368 MHz is applied on this pin.</p> <p><i>NOTE: In single frequency mode, this reference clock is not required.</i></p>
G16	DS3CLK	I	<p><b>DS3 Clock Input (44.736 MHz ± 20 ppm):</b> If any of the channels is configured in DS3 mode, a reference clock 44.736 MHz. is applied on this pin.</p> <p><i>NOTE: In single frequency mode, this reference clock is not required.</i></p>
C16	STS-1CLK/ 12M	I	<p><b>STS-1 Clock Input (51.84 MHz ± 20 ppm):</b> If any of the channels is configured in STS-1 mode, a reference clock 51.84 MHz is applied on this pin..</p> <p>In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the channels in E3, DS3 or STS-1 modes.</p>
L15	SFM_EN	I	<p><b>Single Frequency Mode Enable:</b> Tie this pin "High" to enable the Single Frequency Mode. A reference clock of 12.288 MHz ± 20 ppm is applied.</p> <p>In the Single Frequency Mode (SFM) a low jitter output clock is provided for each channel if the CLK_EN bit is set thus eliminating the need for a separate clock source for the framer.</p> <p>Tie this pin "Low" if single frequency mode is not selected. In this case, the appropriate reference clocks must be provided.</p> <p><i>NOTE: This pin is internally pulled down</i></p>
B1 T1 B17 T17 D11 P11	CLKOUT_0 CLKOUT_1 CLKOUT_2 CLKOUT_3 CLKOUT_4 CLKOUT_5	O	<p><b>Clock output for channel 0</b> <b>Clock output for channel 1</b> <b>Clock output for channel 2</b> <b>Clock output for channel 3</b> <b>Clock output for channel 4</b> <b>Clock output for channel 5</b></p> <p>Low jitter clock output for each channel based on the mode selection (E3,DS3 or STS-1) if the CLKOUTEN_n bit is set in the control register.</p> <p>This eliminates the need for a separate clock source for the framer.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The maximum drive capability for the clockouts is 16 mA.</li> <li>This clock out is available both in SFM and non-SFM modes.</li> </ol>

**CONTROL AND ALARM INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
B7 R6 C14 R14 C6 D14	MRING_0 MRING_1 MRING_2 MRING_3 MRING_4 MRING_5	I	<p><b>Monitor Ring Input - Channel 0:</b>  <b>Monitor Ring Input - Channel 1:</b>  <b>Monitor Ring Input - Channel 2:</b>  <b>Monitor Ring Input - Channel 3:</b>  <b>Monitor Ring Input - Channel 4:</b>  <b>Monitor Ring Input - Channel 5:</b></p> <p>The bipolar line output signal from TRING_n is connected to this pin via a 270 Ω resistor to check for line driver failure.</p> <p><i>NOTE: This pin is internally pulled up.</i></p>
B8 R7 C13 R13 C7 D13	MTIP_0 MTIP_1 MTIP_2 MTIP_3 MTIP_4 MTIP_5	I	<p><b>Monitor Tip Input - Channel 0:</b>  <b>Monitor Tip Input - Channel 1:</b>  <b>Monitor Tip Input - Channel 2:</b>  <b>Monitor Tip Input - Channel 3:</b>  <b>Monitor Tip Input - Channel 4:</b>  <b>Monitor Tip Input - Channel 5:</b></p> <p>The bipolar line output signal from TTIP_n is connected to this pin via a 270-ohm resistor to check for line driver failure.</p> <p><i>NOTE: This pin is internally pulled up.</i></p>
C5 T4 B12 T12 D5 B15	DMO_0 DMO_1 DMO_2 DMO_3 DMO_4 DMO_5	O	<p><b>Drive Monitor Output - Channel 0:</b>  <b>Drive Monitor Output - Channel 1:</b>  <b>Drive Monitor Output - Channel 2:</b>  <b>Drive Monitor Output - Channel 3:</b>  <b>Drive Monitor Output - Channel 4:</b>  <b>Drive Monitor Output - Channel 5:</b></p> <p>If MTIP_n and MRING_n has no transition pulse for <math>128 \pm 32</math> TxCLK_n cycles, DMO_n goes "High" to indicate the driver failure. DMO_n output stays "High" until the next AMI signal is detected.</p>
C8 T7 C12 T11 B11 R8	RLOS_0 RLOS_1 RLOS_2 RLOS_3 RLOS_4 RLOS_5	O	<p><b>Receive Loss of Signal - Channel 0:</b>  <b>Receive Loss of Signal - Channel 1:</b>  <b>Receive Loss of Signal - Channel 2:</b>  <b>Receive Loss of Signal - Channel 3:</b>  <b>Receive Loss of Signal - Channel 4:</b>  <b>Receive Loss of Signal - Channel 5:</b></p> <p>This output pin toggles "High" if the receiver has detected a Loss of Signal Condition.</p>

**CONTROL AND ALARM INTERFACE**

C9 T8 D12 R11 C11 R9	RLOL_0 RLOL_1 RLOL_2 RLOL_3 RLOL_4 RLOL_5	O	<b>Receive Loss of Lock - Channel 0:</b> <b>Receive Loss of Lock - Channel 1:</b> <b>Receive Loss of Lock - Channel 2:</b> <b>Receive Loss of Lock - Channel 3:</b> <b>Receive Loss of Lock - Channel 4:</b> <b>Receive Loss of Lock - Channel 5:</b>  This output pin toggles "High" if a Loss of Lock Condition is detected. LOL (Loss of Lock) condition occurs if the recovered clock frequency deviates from the Reference Clock frequency (available at either E3CLK or DS3CLK or STS-1CLK input pins) by more than 0.5%.
L16	RXA	****	<b>External Resistor of 3.01K <math>\Omega \pm 1\%</math>.</b> Should be connected between RxA and RxB for internal bias.
K16	RXB	****	<b>External Resistor of 3.01K <math>\Omega \pm 1\%</math>.</b> Should be connected between RxA and RxB for internal bias.
P12	ICT	I	<b>In-Circuit Test Input:</b> Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, tie this pin "High". <i>NOTE: This pin is internally pulled up.</i>
R12	TEST	****	<b>Factory Test Pin</b> <i>NOTE: This pin must be connected to GND for normal operation.</i>

**MICROPROCESSOR INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
K3	$\overline{CS}$	I	<b>Chip Select</b> Tie this "Low" to enable the communication with the Microprocessor Interface.
R1	PCLK	I	<b>Processor Clock Input</b> To operate the Microprocessor Interface, appropriate clock frequency is provided through this pin. Maximum frequency is 66 Mhz.
K2	$\overline{WR}$	I	<b>Write Data :</b> To write data into the registers, this active low signal is asserted.
L2	$\overline{RD}$	I	<b>Read Data:</b> To read data from the registers, this active low pin is asserted.
J3	$\overline{RESET}$	I	<b>Register Reset:</b> Setting this input pin "Low" resets the contents of the Command Registers to their default settings and default operating configuration <i>NOTE: This pin is internally pulled up.</i>
L3	PMODE	I	<b>Processor Mode Select:</b> When this pin is tied "High", the microprocessor is operating in synchronous mode which means that clock must be applied to the PCLK (pin 55). Tie this pin "Low" to select the Asynchronous mode. An internal clock is provided for the microprocessor interface.

**MICROPROCESSOR INTERFACE**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
T3	$\overline{RDY}$	O	<b>Ready Acknowledge:</b> <i>NOTE: This pin must be connected to VDD via 3 k<math>\Omega</math> <math>\pm</math> 1% resistor.</i>
U3	$\overline{INT}$	O	<b>INTERRUPT Output:</b> A transition to "Low" indicates that an interrupt has been generated. The interrupt function can be disabled by clearing the interrupt enable bit in the Channel Control Register. <b>NOTES:</b> 1. This pin will remain asserted "Low" until the interrupt is serviced. 2. This pin must be connected to VDD via 3 k $\Omega$ $\pm$ 1% resistor.
B4 A3 B3 C4 C3 C2 D3 D4	ADDR[0] ADDR[1] ADDR[2] ADDR[3] ADDR[4] ADDR[5] ADDR[6] ADDR[7]	I	<b>ADDRESS BUS:</b> 8 bit address bus for the microprocessor interface
N4 P3 P4 P5 R5 R4 R3 R2	D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	<b>DATA BUS:</b> 8 bit Data Bus for the microprocessor interface



**ANALOG POWER AND GROUND**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
E2	TxAVDD_0	****	Transmitter Analog 3.3 V $\pm$ 5% VDD - Channel 0
N2	TxAVDD_1	****	Transmitter Analog 3.3 V $\pm$ 5% VDD - Channel 1
E16	TxAVDD_2	****	Transmitter Analog 3.3 V $\pm$ 5% VDD - Channel 2
N16	TxAVDD_3	****	Transmitter Analog 3.3 V $\pm$ 5% VDD - Channel 3
J2	TxAVDD_4	****	Transmitter Analog 3.3 V $\pm$ 5% VDD - Channel 4
J16	TxAVDD_5	****	Transmitter Analog 3.3 V $\pm$ 5% VDD - Channel 5
D2	TxAGND_0	****	Transmitter Analog GND - Channel 0
M2	TxAGND_1	****	Transmitter Analog GND - Channel 1
D16	TxAGND_2	****	Transmitter Analog GND - Channel 2
M16	TxAGND_3	****	Transmitter Analog GND - Channel 3
H2	TxAGND_4	****	Transmitter Analog GND - Channel 4
H16	TxAGND_5	****	Transmitter Analog GND - Channel 5
A4	RxAVDD_0	****	Receiver Analog 3.3 V $\pm$ 5% VDD - Channel 0
U4	RxAVDD_1	****	Receiver Analog 3.3 V $\pm$ 5% VDD - Channel 1
A15	RxAVDD_2	****	Receiver Analog 3.3 V $\pm$ 5% VDD - Channel 2
U15	RxAVDD_3	****	Receiver Analog 3.3 V $\pm$ 5% VDD - Channel 3
A8	RxAVDD_4	****	Receiver Analog 3.3 V $\pm$ 5% VDD - Channel 4
U8	RxAVDD_5	****	Receiver Analog 3.3 V $\pm$ 5% VDD - Channel 5
A7	RxAGND_0	****	Receiver Analog GND - Channel_0
U7	RxAGND_1	****	Receive Analog GND - Channel 1
A12	RxAGND_2	****	Receive Analog GND - Channel 2
U12	RxAGND_3	****	Receive Analog GND - Channel 3
A11	RxAGND_4	****	Receive Analog GND - Channel 4
U11	RxAGND_5	****	Receive Analog GND - Channel 5
E4	JaAVDD_0	****	Analog 3.3 V $\pm$ 5% VDD - Jitter Attenuator Channel 0
K4	JaAVDD_1	****	Analog 3.3 V $\pm$ 5% VDD - Jitter Attenuator Channel 1
E14	JaAVDD_2	****	Analog 3.3 V $\pm$ 5% VDD - Jitter Attenuator Channel 2
K14	JaAVDD_3	****	Analog 3.3 V $\pm$ 5% VDD - Jitter Attenuator Channel 3
G4	JaAVDD_4	****	Analog 3.3 V $\pm$ 5% VDD - Jitter Attenuator Channel 4
G14	JaAVDD_5	****	Analog 3.3 V $\pm$ 5% VDD - Jitter attenuator Channel 5
F4	JaAGND_0	****	Analog GND - Jitter Attenuator Channel 0

**ANALOG POWER AND GROUND**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
J4	JaAGND_1	****	Analog GND - Jitter Attenuator Channel 1
F14	JaAGND_2	****	Analog GND - Jitter Attenuator Channel 2
J14	JaAGND_3	****	Analog GND - Jitter Attenuator Channel 3
H4	JaAGND_4	****	Analog GND - Jitter Attenuator Channel 4
H14	JaAGND_5	****	Analog GND - Jitter Attenuator Channel 5
C10	AGND	****	Analog GND
R10	AGND	****	Analog GND
H9	AGND	****	Analog GND
J9	AGND	****	Analog GND
K9	AGND	****	Analog GND
N15	REFAVDD	****	Analog 3.3 V $\pm$ 5% VDD - Reference
M15	REFGND	****	Reference GND

**DIGITAL POWER AND GROUND**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
F1	TxVDD_0	****	<b>Transmitter 3.3 V ± 5% VDD Channel 0</b>
L1	TxVDD_1	****	<b>Transmitter 3.3 V ± 5% VDD Channel 1</b>
F17	TxVDD_2	****	<b>Transmitter 3.3 V ± 5% VDD Channel 2</b>
L17	TxVDD_3	****	<b>Transmitter 3.3 V ± 5% VDD Channel 3</b>
K1	TxVDD_4	****	<b>Transmitter 3.3 V ± 5% VDD Channel 4</b>
K17	TxVDD_5	****	<b>Transmitter 3.3 V ± 5% VDD Channel 5</b>
C1	TxGND_0	****	<b>Transmitter GND - Channel 0</b>
P1	TxGND_1	****	<b>Transmitter GND - Channel 1</b>
C17	TxGND_2	****	<b>Transmitter GND - Channel 2</b>
P17	TxGND_3	****	<b>Transmitter GND - Channel 3</b>
G1	TxGND_4	****	<b>Transmitter GND - Channel 4</b>
G17	TxGND_5	****	<b>Transmitter GND - Channel 5</b>
B5	RxDVDD_0	****	<b>Receiver 3.3 V ± 5% VDD - Channel 0</b>
T5	RxDVDD_1	****	<b>Receiver 3.3 V ± 5% VDD - Channel 1</b>
B14	RxDVDD_2	****	<b>Receiver 3.3 V ± 5% VDD - Channel 2</b>
T14	RxDVDD_3	****	<b>Receiver 3.3 V ± 5% VDD - Channel 3</b>
B9	RxDVDD_4	****	<b>Receiver 3.3 V ± 5% VDD - Channel 4</b>
T9	RxDVDD_5	****	<b>Receiver 3.3 V ± 5% VDD - Channel 5</b>
B6	RxDGND_0	****	<b>Receiver Digital GND - Channel 0</b>
T6	RxDGND_1	****	<b>Receiver Digital GND - Channel 1</b>
B13	RxDGND_2	****	<b>Receiver Digital GND - Channel 2</b>
T13	RxDGND_3	****	<b>Receiver Digital GND - Channel 3</b>
B10	RxDGND_4	****	<b>Receiver Digital GND - Channel 4</b>
T10	RxDGND_5	****	<b>Receiver Digital GND - Channel 5</b>
P6	DVDD_1	****	<b>VDD 3.3 V ± 5%</b>
C15	DVDD_2	****	<b>VDD 3.3 V ± 5%</b>
L4	JaDVDD_1	****	<b>VDD 3.3 V ± 5%</b>
D6	DVDD(uP)	****	<b>VDD 3.3 V ± 5%</b>
L14	JaDVDD_2	****	<b>VDD 3.3 V ± 5%</b>
D15	DGND_1	****	<b>Digital GND</b>
D7	DGND(uP)	****	<b>Digital GND</b>

**DIGITAL POWER AND GROUND**

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
M14	JaDGND_2	****	Digital GND
M4	JaDGND_1	****	Digital GND
P7	DGND	****	Digital GND
H8	DGND	****	Digital GND
J8	DGND	****	Digital GND
K8	DGND	****	Digital GND
H10	DGND	****	Digital GND
J10	DGND	****	Digital GND
K10	DGND	****	Digital GND

**FUNCTIONAL DESCRIPTION**

The XRT73R06 is a six channel fully integrated Line Interface Unit featuring EXAR’s R<sup>3</sup> Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 6 independent Receivers, Transmitters and Jitter Attenuators in a single 217 Lead BGA package. Each channel can be independently programmed to support E3, DS-3 or STS-1 line rates using one input clock reference of 12.288MHz in Single Frequency Mode (SFM). The LIU is responsible for providing the physical connection between a line interface and an aggregate mapper or framing device. Along with the analog-to-digital processing, the LIU offers monitoring and diagnostic features to help optimize network design implementation. A key characteristic within the network topology is Automatic Protection Switching (APS).

EXAR’s proven expertise in providing redundant solutions has paved the way for R<sup>3</sup> Technology.

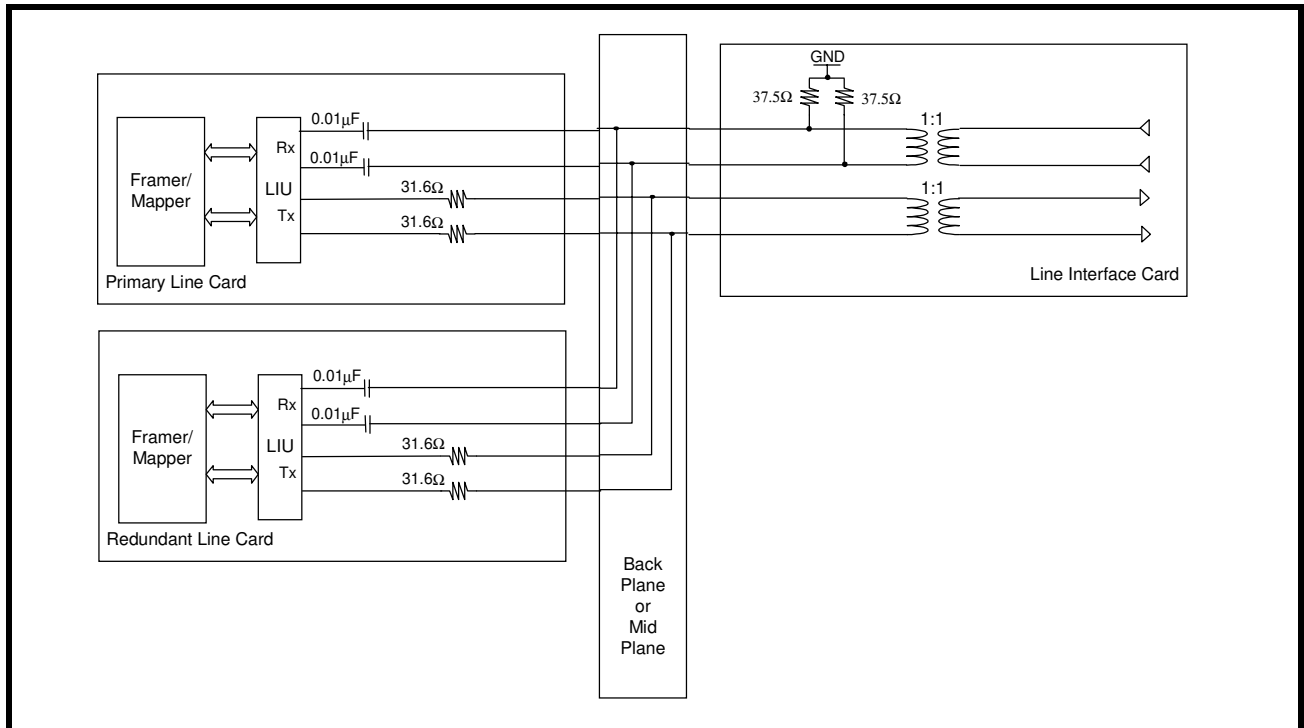
**1.0 R<sup>3</sup> TECHNOLOGY (RECONFIGURABLE, RELAYLESS REDUNDANCY)**

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. EXAR’s R<sup>3</sup> technology has re-defined E3/DS-3/STS-1 LIU design for 1:1 and 1+1 redundancy applications. Without relays and one Bill of Materials, EXAR offers multi-port, integrated LIU solutions to assist high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R<sup>3</sup> Technology with EXAR’s world leading line interface units.

**1.1 Network Architecture**

A common network design that supports 1:1 or 1+1 redundancy consists of N primary cards along with N backup cards that connect into a mid-plane or back-plane architecture without transformers installed on the network cards. In addition to the network cards, the design has a line interface card with one source of transformers, connectors, and protection components that are common to both network cards. With this design, the bill of materials is reduced to the fewest amount of components. See Figure 3. for a simplified block diagram of a typical redundancy design.

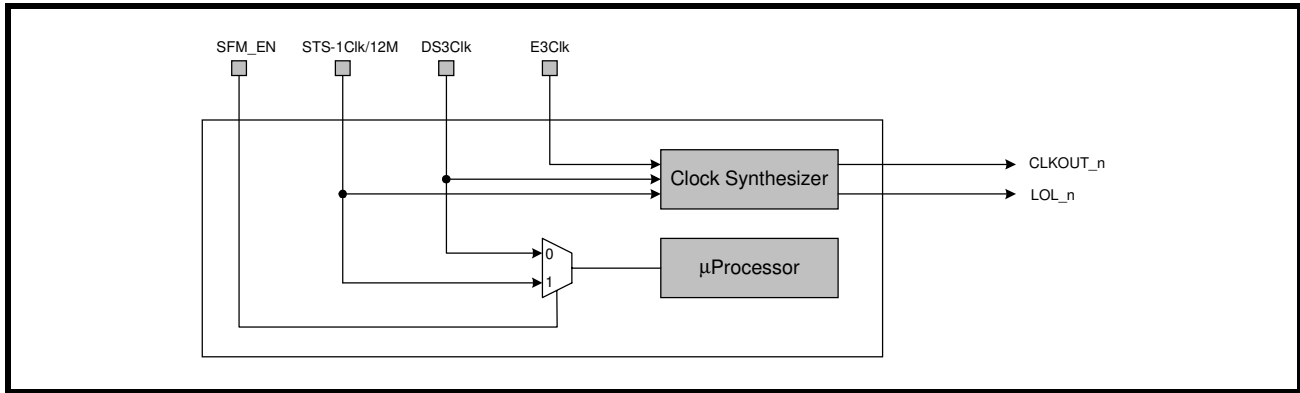
**FIGURE 3. NETWORK REDUNDANCY ARCHITECTURE**



**2.0 CLOCK SYNTHESIZER**

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS-3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS-3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS-3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM\_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS-3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 4

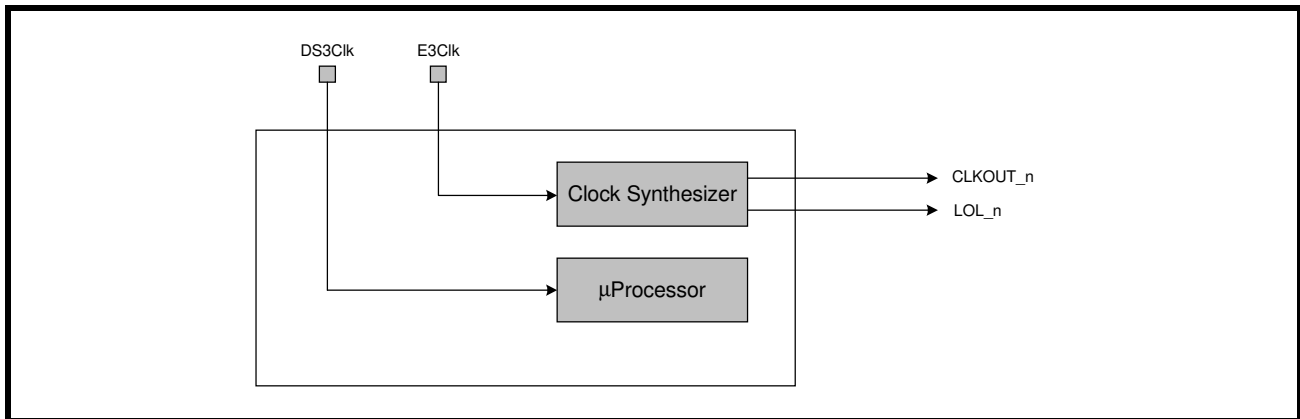
**FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR**



**2.1 Clock Distribution**

Network cards that are designed to support multiple line rates which are not configured for single frequency mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS-3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. If however, multiple line rates will not be supported, i.e. E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.

**FIGURE 5. CLOCK DISTRIBUTION CONFIGURED IN E3 MODE WITHOUT USING SFM**



**NOTE:** For one input clock reference, the single frequency mode should be used.

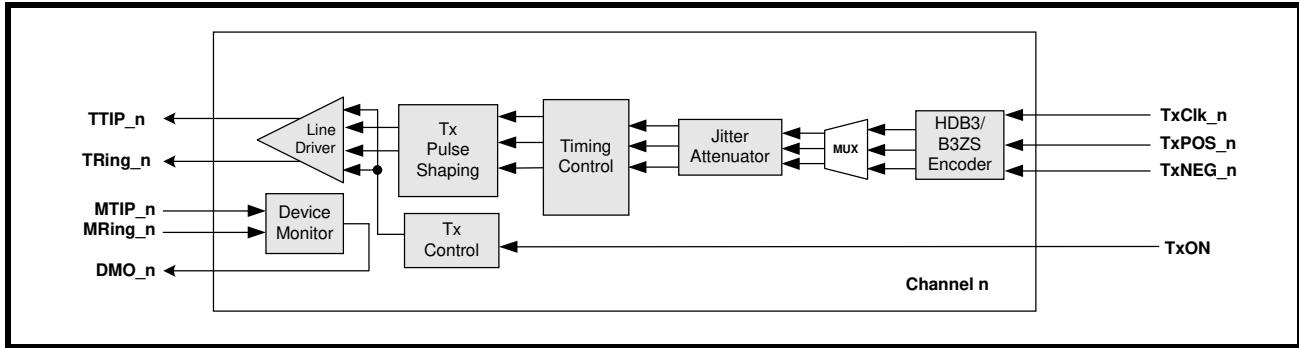




### 3.0 THE TRANSMITTER SECTION

The transmitter is designed so that the LIU can accept serial data from a local device, encode the data properly, and then output an analog pulse according to the pulse shape chosen in the appropriate registers. This section describes the detailed operation of various blocks within the transmit path. A simplified block diagram of the transmit path is shown in Figure 6.

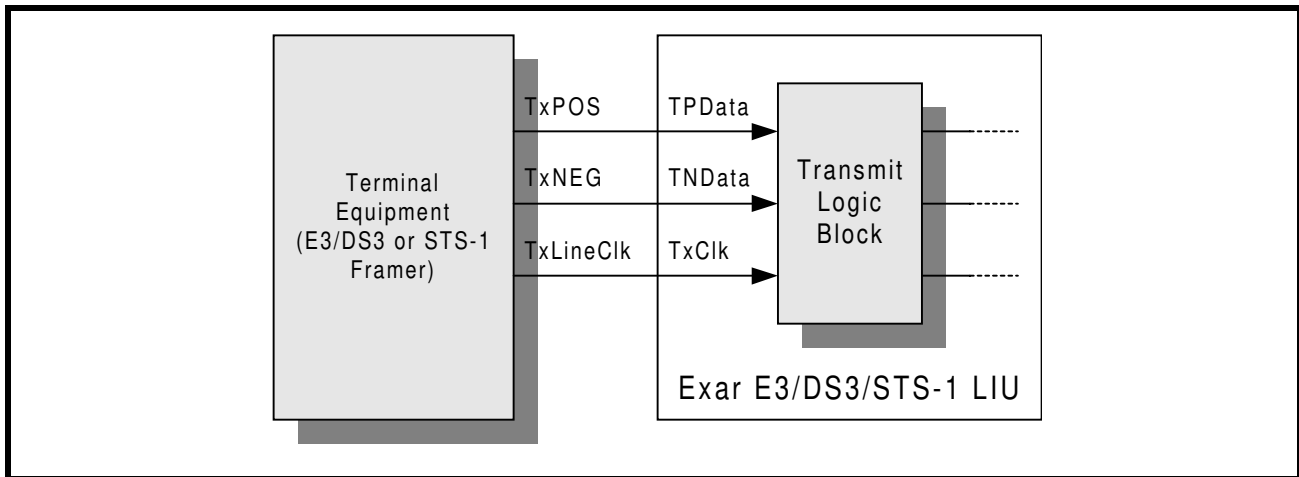
**FIGURE 6. TRANSMIT PATH BLOCK DIAGRAM**



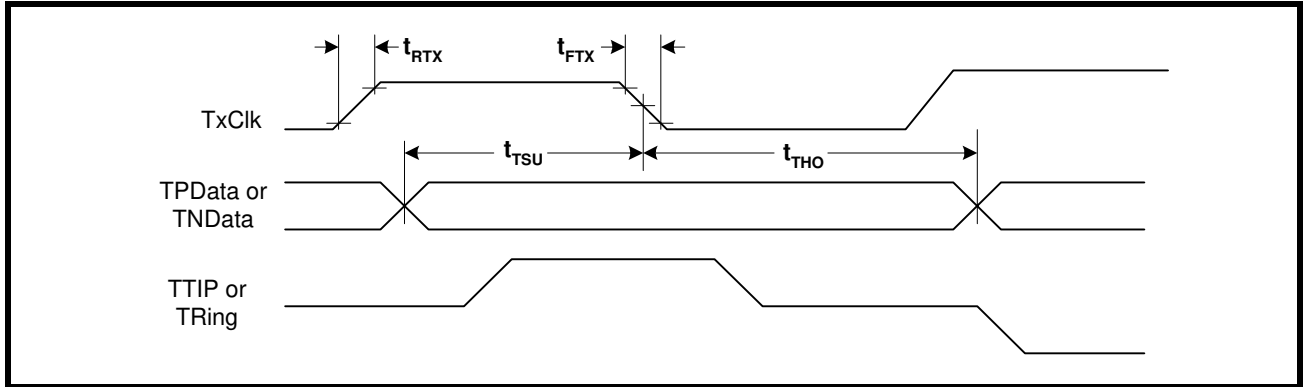
#### 3.1 Transmit Digital Input Interface

The method for applying data to the transmit inputs of the LIU is a serial interface consisting of TxClk, TxPOS, and TxNEG. For single rail mode, only TxClk and TxPOS are necessary for providing the local data from a Framer device or ASIC. Data can be sampled on either edge of the input clock signal by programming the appropriate register. A typical interface is shown in Figure 7.

**FIGURE 7. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT73R06 (DUAL-RAIL DATA)**

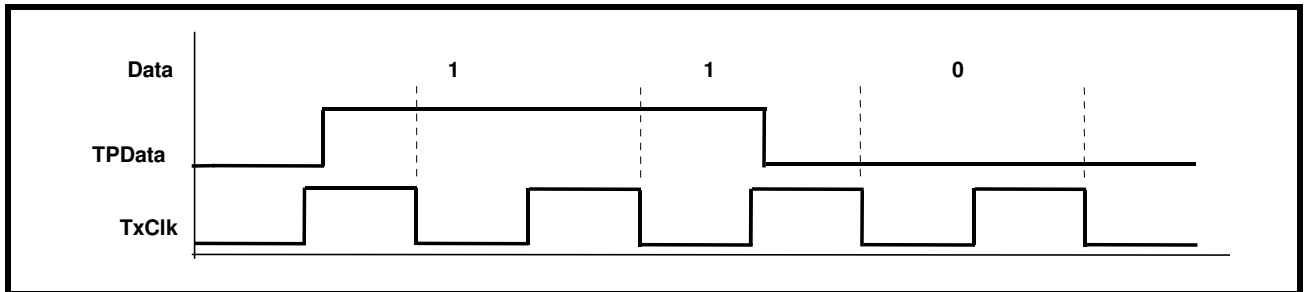


**FIGURE 8. TRANSMITTER TERMINAL INPUT TIMING**

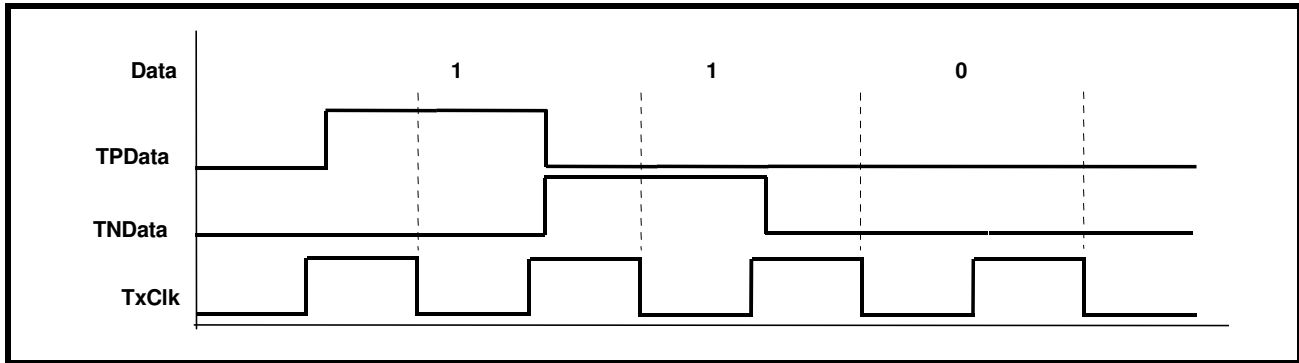


SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxCk	Duty Cycle	30	50	70	%
	TxCk Frequency				
	E3		34.368		MHz
	DS-3		44.736		MHz
	STS-1		51.84		MHz
$t_{RTX}$	TxCk Rise Time (10% to 90%)			4	ns
$t_{FTX}$	TxCk Fall Time (10% to 90%)			4	ns
$t_{TSU}$	TPData/TNData to TxCk falling set up time	3			ns
$t_{THO}$	TPData/TNData to TxCk falling hold time	3			ns

**FIGURE 9. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)**



**FIGURE 10. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)**



**3.2 Transmit Clock**

The Transmit Clock applied via TxClk\_n pins, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock to be supplied.

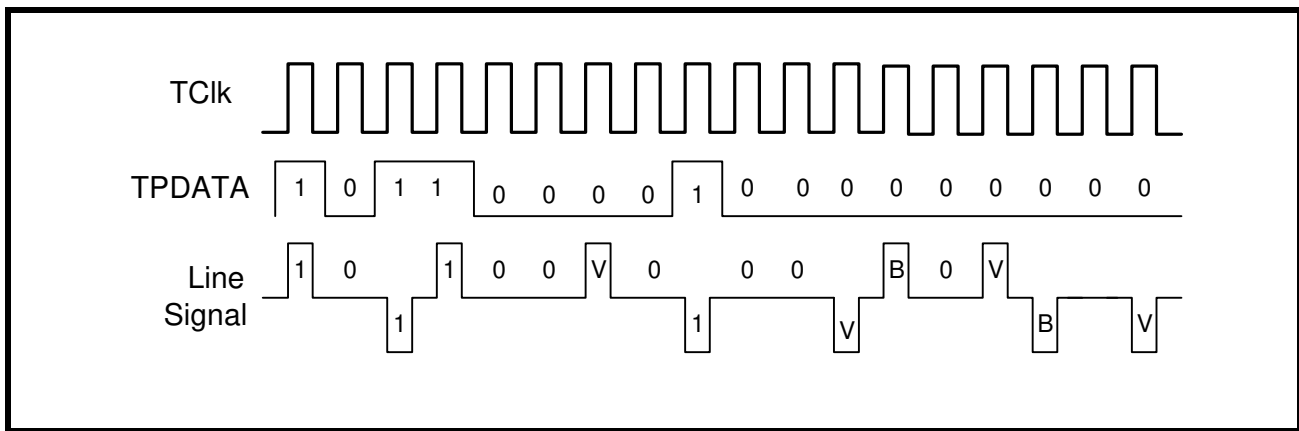
**3.3 B3ZS/HDB3 ENCODER**

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

**3.3.1 B3ZS Encoding**

An example of B3ZS encoding is shown in Figure 11. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

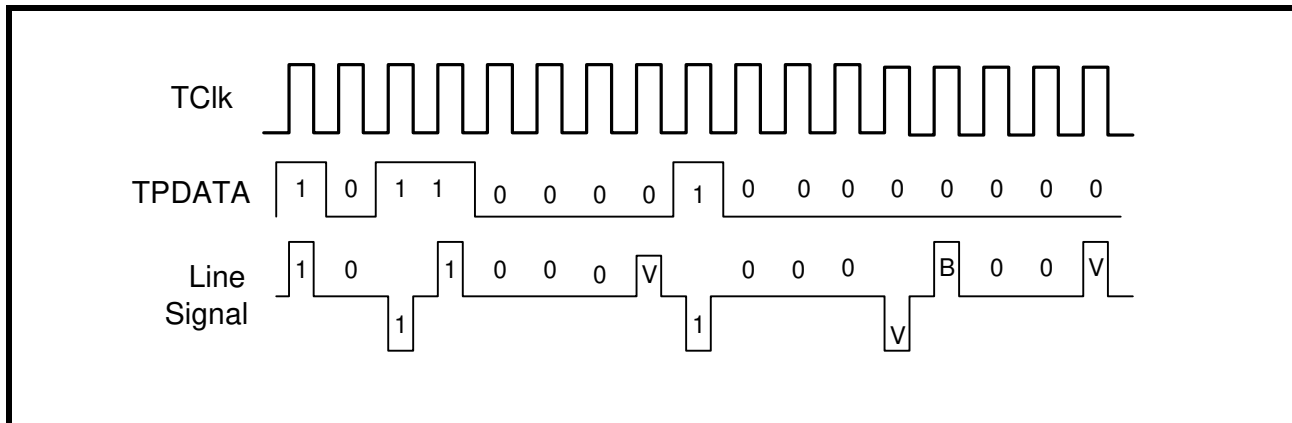
**FIGURE 11. B3ZS ENCODING FORMAT**



**3.3.2 HDB3 Encoding**

An example of the HDB3 encoding is shown in Figure 12. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

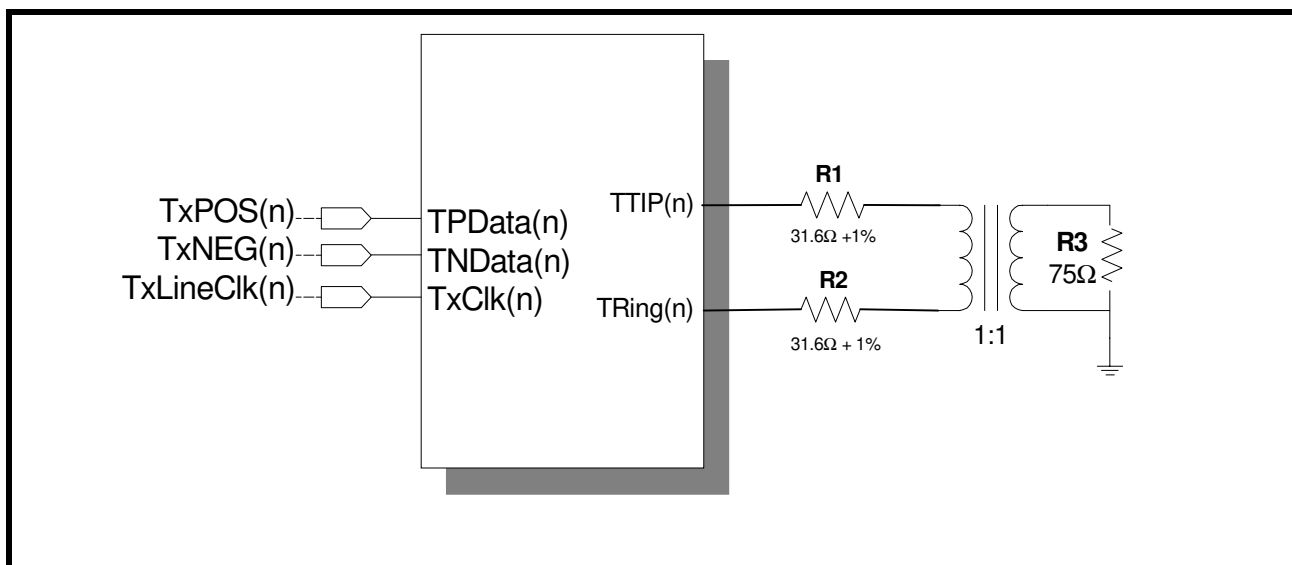
**FIGURE 12. HDB3 ENCODING FORMAT**



**3.4 TRANSMIT PULSE SHAPER**

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meets the industry standard mask template requirements for STS-1 and DS3. For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. The Pulse Shaper Block also includes a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV\_n bit to “1” or “0” in the control register. For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet. For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled. The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 13.

**FIGURE 13. TRANSMIT PULSE SHAPE TEST CIRCUIT**



**3.4.1 Guidelines for using Transmit Build Out Circuit**

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV\_n control bit to “0”. If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.