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GENERAL DESCRIPTION

The XRT75L02 is a two-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/STS-1 applications. It incorporates independent Receivers, Transmitters and Jitter Attenuators in a single 100 pin TQFP package.

The XRT75L02 can be configured to operate in either E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) modes.The transmitter can be turned off (tri-stated) for redundancy support and for conserving power.

The XRT75L02's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75L02 incorporates advanced crystal-less jitter attenuators that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

The XRT75L02 provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75L02 supports local,remote and digital loop-backs. The XRT75L02 also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES

RECEIVER:

- On chip Clock and Data Recovery circuit for high input jitter tolerance.
- Meets the jitter tolerance requirements as specified in ITU-T G.823_1993 for E3 and Telcordia GR-499-CORE for DS3 applications.
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation.
- On chip B3ZS/HDB3 encoder and decoder that can either be enabled or disabled.
- On-chip clock synthesizer generates the appropriate rate clock from a single frequency XTAL.
- Provides low jitter clock outputs for either DS3,E3 or STS-1 rates.
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock.
- Provides low jitter output clock.

TRANSMITTER:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Transmitters can be turned on or off.

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator.
- Jitter Attenuator can be selected in Receive or Transmit paths.
- 16 or 32 bits selectable FIFO size.
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards.
- Jitter Attenuators can be disabled.

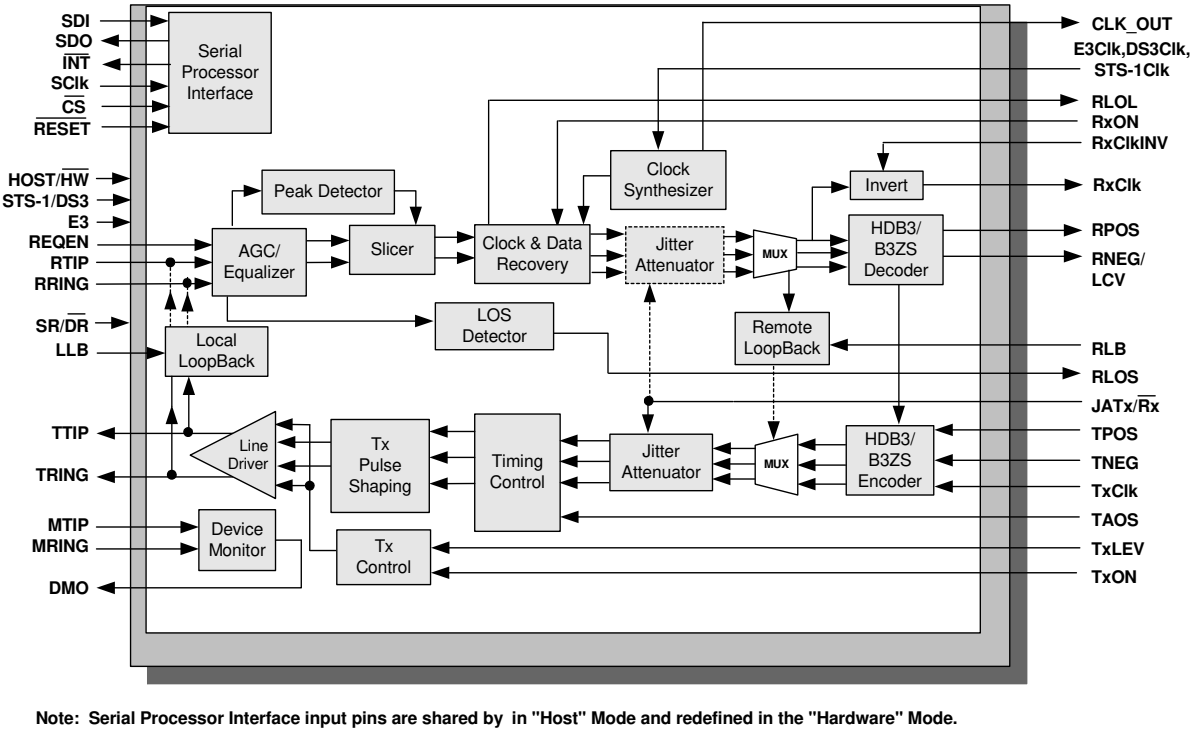
CONTROL AND DIAGNOSTICS:

- 5 wire Serial Microprocessor Interface for control and configuration.
- Supports optional internal Transmit Driver Monitoring.
- PRBS error counter register to accumulate errors.
- Hardware Mode for control and configuration.
- Supports Local, Remote and Digital Loop-backs.
- Single 3.3 V ± 5% power supply.
- 5 V Tolerant I/O.
- Available in 100 pin TQFP.
- -40℃ to 85℃ Industrial Temperature Range.

APPLICATIONS

- E3/DS3 Access Equipment.
- STS1-SPE to DS3 Mapper.
- DSLAMs.
- Digital Cross Connect Systems.
- CSU/DSU Equipment.
- Routers.
- Fiber Optic Terminals.

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75L02



Note: Serial Processor Interface input pins are shared by in "Host" Mode and redefined in the "Hardware" Mode.

TRANSMIT INTERFACE CHARACTERISTICS

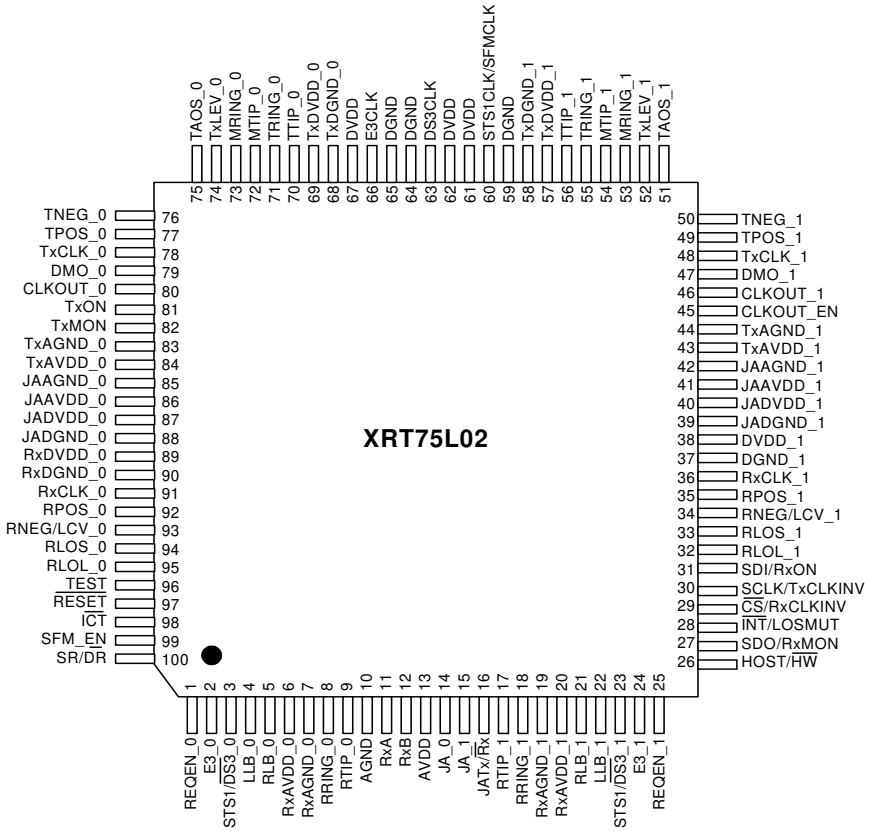
- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit.
- Built-in B3ZS/HDB3 Encoder (which can be disabled).
- Accepts Transmit Clock with duty cycle of 30%-70%.
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications.
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993.
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE.
- Transmitter can be turned off in order to support redundancy designs.

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery.
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications.
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications.
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications.
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms.
- Built-in B3ZS/HDB3 Decoder (which can be disabled).

- Recovered Data can be muted while the LOS Condition is declared.
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment.

FIGURE 2. PIN OUT OF THE XRT75L02



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L02IV	14mm x 14mm 100 Pin TQFP	-40˚C to +85˚C

TABLE OF CONTENTS

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
81	TxON	I	**Transmitter ON Input :** This input pin is used to either enable or disable the Transmit Output Driver. "Low" - Disables the Transmit Output Driver. In this setting, the TTIP and TRING output pins will be tri-stated. "High" - Enables the Transmit Output Driver. In this setting, the TTIP and TRING output pins will be enabled. ***NOTES:*** *1. Even when the XRT75L02 is configured in HOST mode, this pin will be active. To enable software control of the Transmit Output Driver output, pull this pin "High".* *2. When the Transmitter is turned off either in Host or Hardware mode, the TTIP and TRing outputs are Tri-stated.* *3. This pins are internally pulled "High"*
78 48	TxCLK_0 TxCLK_1	I	**Transmit Clock Input for TPOS and TNEG - Channel 0:** **Transmit Clock Input for TPOS and TNEG - Channel 1:** The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%. By default, input data is sampled on the falling edge of TxCLK when input data is changing on the rising edge of TxCLK..
76 50	TNEG_0 TNEG_1	I	**Transmit Negative Data Input - Channel 0:** **Transmit Negative Data Input - Channel 1:** In Dual-rail mode, these pins are sampled on the falling or rising edge of TxCLK_n ***NOTE:*** *These input pins are ignored and must be grounded if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.*
77 49	TPOS_0 TPOS_1	I	**Transmit Positive Data Input - Channel 0:** **Transmit Positive Data Input - Channel 1:** By default sampled on the falling edge of TxCLK
70 56	TTIP_0 TTIP_1	O	**Transmit TTIP Output - Channel 0:** **Transmit TTIP Output - Channel 1:** These pins along with TRING transmit bipolar signals to the line using a 1:1 transformer.
71 55	TRING_0 TRING_1	O	**Transmit Ring Output - Channel 0:** **Transmit Ring Output - Channel 1:** These pins along with TTIP transmit bipolar signals to the line using a 1:1 transformer.

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
30	TxClkINV/ SClk	I	**Hardware Mode: Transmit Clock Invert** **Host Mode: Serial Clock Input:** Function of this pin depends on whether the XRT75L02 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" configures all the Transmitters to sample the TPOS_n and TNEG_n data on the rising edge of the TxClk_n . ***NOTES:*** *1. If the XRT75L02 is configured in HOST mode, this pin functions as SClk input pin (please refer to the pin description for Microprocessor interface).*
82	TxMON	I	**Transmitter Monitor:** When this pin is pulled "High", MTIP and MRING are connected internally to TTIP and TRING and allows self monitoring of the transmitter.
74 52	TxLEV_0 TxLEV_1	I	**Transmit Line Build-Out Enable/Disable Select - Channel 0:** **Transmit Line Build-Out Enable/Disable Select - Channel 1:** These input pins select the Transmit Line Build-Out circuit. Setting these pins to "High" disables the Line Build-Out circuit of Channel n. In this mode, Channel n outputs partially-shaped pulses onto the line via the TTIP_n and TRing_n output pins. Setting these pins to "Low" enables the Line Build-Out circuit of Channel n. In this mode, Channel n outputs shaped pulses onto the line via the TTIP_n and TRing_n output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set these pins to "1" if the cable length between the Cross-Connect and the transmit output of Channel is greater than 225 feet. 2. Set these pins to "0" if the cable length between the Cross-Connect and the transmit output of Channel is less than 225 feet. These pins are active only if the following two conditions are true: a. The XRT75L02 is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT75L02 is configured to operate in the Hardware Mode. ***NOTES:*** *1. These pins are internally pulled down.* *2. If the XRT75L02 is configured in HOST mode, these pins should be tied to GND.*
75 51	TAOS_0 TAOS_1	I	**Transmit All Ones Select - Channel 0:** **Transmit All Ones Select - Channel 1:** A "High" on this pin causes the Transmitter Section of Channel_n to generate and transmit a continuous AMI all "1's" pattern onto the line. The frequency of this "1's" pattern is determined by TxClk_n. ***NOTES:*** *1. This input pin is ignored if the XRT75L02 is operating in the HOST Mode and should be tied to GND.* *2. Analog Loopback and Remote Loopback have priority over request.* *3. This pin is internally pulled down.*

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
1 25	REQEN_0 REQEN_1	I	**Receive Equalization Enable Input - Channel 0:** **Receive Equalization Enable Input - Channel 1:** Setting this input pin "High" enables the Internal Receive Equalizer of Channel_n. Setting this pin "Low" disables the Internal Receive Equalizer. ***NOTES:*** *1. This input pin is ignored and should be connected to GND if the XRT75L02 is operating in the HOST Mode* *2. This pin is internally pulled down.*
31	RxON/ SDI	I	**Hardware Mode: Receiver Turn ON Input** **Host Mode: Serial Data Input:** Function of this pin depends on whether the XRT75L02 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin “High” turns on and enables the Receivers of all the channels. ***NOTES:*** *1. If the XRT75L02 is configured in HOST mode, this pin functions as SDI input pin (please refer to the pin description for Microprocessor Interface)* *2. This pin is internally pulled down.*
27	RxMON/ SDO	I	**Hardware Mode: Receive Monitoring Mode** **Host Mode: Serial Data Output:** In Hardware mode, when this pin is tied “High” all 2 channels configure into monitoring channels. In the monitoring mode, the Receiver is capable of monitoring the signals with 20 dB flat loss plus 6 dB cable attenuation. This allows monitoring very weak signal, however the internal LOS circuitry is suppressed and LOS will never assert nor LOS be declared when operating under this mode. In HOST Mode each channel can be independently configured to be a monitoring channel by setting the bits in the channel control registers. ***NOTE:*** *If the XRT75L02 is configured in HOST mode, this pin functions as SDO pin (please refer to the pin description for the Microprocessor Interface).*
91 36	RxCLK_0 RXCLK_1	O	**Receive Clock Output - Channel 0:** **Receive Clock Output - Channel 1:** By default, RPOS and RNEG data sampled on the rising edge RxCLK.. Set the RxCLKINV bit or tie RClkINV pin “High” to sample RPOS/RNEG data on the falling edge of RxCLK
92 35	RPOS_0 RPOS_1	O	**Receive Positive Data Output - Channel 0:** **Receive Positive Data Output - Channel 1:** ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled in Single-rail mode, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is removed and replaced with ‘0’.*

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
93 34	RNEG_0/LCV_0 RNEG_1/LCV_1	O	**Receive Negative Data Output/Line Code Violation Indicator - Channel 0:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 1:** In Dual Rail mode, a negative pulse is output through RNEG. **Line Code Violation Indicator - Channel n:** If configured in Single Rail mode then Line Code Violation will be output.
8 18	RRING_0 RRING_1	I	**Receive Ring Input - Channel 0:** **Receive Ring Input - Channel 1:** These pins along with RTIP receive the bipolar line signal from the remote DS3/E3/STS-1 Terminal.
9 17	RTIP_0 RTIP_1	I	**Receive TIP Input - Channel 0:** **Receive TIP Input - Channel 1:** These pins along with RRING receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
29	RxClkINV/ $\overline{CS}$	I	**Hardware Mode: RxClk INVERT** **Host Mode: Chip Select**: Function of this pin depends on whether the XRT75L02 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" configures the Receiver Section of all channels to invert the RxClk_n output signals and outputs the recovered data via RPOS_n and RNEG_n on the falling edge of RxClk_n. ***NOTE:*** *If the XRT75L02 is configured in HOST mode, this pin functions as CS input pin (please refer to the pin description for Microprocessor Interface).*

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
66	E3CLK	I	**E3 Clock Input (34.368 MHz ± 20 ppm):** If any of the channels is configured in E3 mode, a reference clock 34.368 MHz is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
63	DS3CLK	I	**DS3 Clock Input (44.736 MHz ± 20 ppm):** If any of the channels is configured in DS3 mode, a reference clock 44.736 MHz. is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
60	STS-1CLK/ 12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm):** If any of the channels is configured in STS-1 mode, a reference clock 51.84 MHz is applied on this pin.. In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the channels in E3, DS3 or STS-1.
99	SFM_EN	I	**Single Frequency Mode Enable:** Tie this pin "High" to enable the Single Frequency Mode. A reference clock of 12.288 MHz ± 20 ppm is applied. This offers the flexibility of using a low cost reference clock and configures the board for either E3 or DS3 or STS-1 without the need to change any components on the board. In the Single Frequency Mode (SFM) an output clock is provided for each channel if the CLKOUT_EN bit is set or CLKOUT_EN pin tied "High". Tie this pin "Low" if single frequency mode is not selected. In this case, the appropriate reference clocks must be provided. ***NOTE:*** *This pin is internally pulled down*
80 46	CLKOUT_0 CLKOUT_1	O	**Clock output for channel 0** **Clock output for channel 1** Low jitter clock is output for each channel based on the mode selection (E3,DS3 or STS-1) if the CLK_EN_n bit is set in the control register or CLKOUT_EN pin is tied "High". This eliminates the need for a separate clock source for the framer. ***NOTES:*** *1. This clock output is only available in SFM mode.* *2. The maximum drive capability for the clockouts is 16 mA.*
45	CLKOUT_EN	I	**Clock Output Enable in Single Frequency Mode:** Tie this pin "High" to enable the output clocks via the CLKOUT pins.

CONTROL AND ALARM INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
73 53	MRING_0 MRING_1	I	**Monitor Ring Input - Channel 0:** **Monitor Ring Input - Channel 1:** The bipolar line output signal from TRING_n is connected to this pin via a 270 Ω resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled "High".*
72 54	MTIP_0 MTIP_1	I	**Monitor Tip Input - Channel 0:** **Monitor Tip Input - Channel 1:** The bipolar line output signal from TTIP_n is connected to this pin via a 270-ohm resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled "High".*
79 47	DMO_0 DMO_1	O	**Drive Monitor Output - Channel 0:** **Drive Monitor Output - Channel 1:** If MTIP_n and MRING_n has no transition pulse for 128 ± 32 TxCLK_n cycles, DMO_n goes “High” to indicate the driver failure. DMO_n output stays “High” until the next AMI signal is detected.
94 33	RLOS_0 RLOS_1	O	**Receive Loss of Signal Output Indicator - Channel 0:** **Receive Loss of Signal Output Indicator - Channel 1:** This output pin toggles "High" if the receiver has detected a Loss of Signal Condition. The criteria for declaring /clearing an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode.
95 32	RLOL_0 RLOL_1	O	**Receive Loss of Lock Output Indicator - Channel 0:** **Receive Loss of Lock Output Indicator - Channel 1:** This output pin toggles "High" if a Loss of Lock Condition is detected. LOL (Loss of Lock) condition occurs if the recovered clock frequency deviates from the Reference Clock frequency (available at either E3CLK or DS3CLK or STS-1CLK input pins) by more than 0.5%.
11	RXA	****	**External Resistor of 3 K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.
12	RXB	****	**External Resistor of 3K Ω ±1%.** Should be connected between RxA and RxB for internal bias.
98	$\overline{\text{ICT}}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, tie this pin "High". ***NOTE:*** *This pin is internally pulled “High”.*
96	TEST	****	**Factory Test Pin** ***NOTE:*** *This pin must be connected to GND for normal operation.*

CONTROL AND ALARM INTERFACE

28	LOSMUT/ $\overline{INT}$	I/O	**Hardware Mode: MUTE-upon-LOS Enable Input** **Host Mode: Interrupt Ouput:** In Hardware Mode, setting pin "High" configures all the channels to Mute the recovered data on the RPOS_n and RNEG_n whenever one of the channels declares an LOS condition. RPOS_n and RNEG_n outputs are pulled "Low". Muting of the output data can be configured/controlled on a per channel basis in Host Mode. ***NOTE:*** *If the XRT75L02 is configured in HOST mode, this pin functions as $\overline{INT}$ pin (please refer to the pin description for the Microprocessor Interface).*
4 22	LLB_0 LLB_1	I	**Local Loop-back - Channel 0:** **Local Loop-back - Channel 1:** This input pin along with RLB_n configures different Loop-Back modes. A "High" on this pin with RLB_n set to "Low" configures Channel_n to operate in the Analog Local Loop-back Mode. A "High" on this pin with RLB_n set to "High" configures Channel_n to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if operating in the HOST Mode.*
5 21	RLB_0 RLB_1	I	**Remote Loop-back - Channel 0:** **Remote Loop-back - Channel 1:** This input pin along with LLB_n configures different Loop-Back modes. A "High" on this pin with LLB_n set to "Low" configures Channel_n to operate in the Remote Loop-back Mode. A "High" on this pin with LLB_n set to "High" configures Channel_n to operate in the Digital Local Loop-back Mode. **RLB_n / LLB_n / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Analog Local** **1 / 0 / Remote** **1 / 1 / Digital** ***NOTE:*** *This input pin is ignored and should be connected to GND when operating in the HOST Mode.*

MODE SELECT

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
2 24	E3_0 E3_1	I	**E3 Mode Select Input** A "High" on this pin configures in E3 mode. A "Low" on this pin configures in either STS-1 or DS3 mode depending on the settings on pins 3 and 23.. ***NOTES:*** *1. This pin is internally pulled down* *2. This pin is ignored if configured to operate in HOST mode.*
3 23	STS1/$\overline{\text{DS3}}$ _0 STS1/$\overline{\text{DS3}}$ _1	I	**STS-1/DS3 Select Input** A "High" on these pins configures in STS-1 mode. A "Low" on these pins configures in DS3 mode. These pins are ignored if the E3_n pins are set to "High". ***NOTES:*** *1. This pin is internally pulled down* *2. This pin is ignored if configured to operate in HOST mode.*
26	HOST/$\overline{\text{HW}}$	I	**Host/Hardware Mode:** Tie this pin "High" to configure in Host mode and "Low" for Hardware mode.
100	SR/$\overline{\text{DR}}$	I	**Single-Rail/Dual-Rail Select:** Setting this "High" configures both the Transmitter and Receiver to operate in Single-rail mode and also enables the B3ZS/HDB3 Encoder and Decoder. In Single-rail mode, TNEG_n pin should be grounded. Setting this "Low" configures both the Transmitter and Receiver to operate in Dual-rail mode and disables the B3ZS/HDB3 Encoder and Decoder. ***NOTE:*** *This pin is internally pulled down.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
29	$\overline{\text{CS}}$ RxCLKINV	I	**Microprocessor Serial Interface - Chip Select** Tie this "Low" to enable the communication with the Microprocessor Serial Interface. ***NOTE:*** *If configured in Hardware Mode, this pin functions as RxClkINV.*
30	SCLK TxCLKINV	I	**Serial Interface Clock Input** The data on the SDI pin is sampled on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. ***NOTE:*** *If configured in Hardware Mode, this pin functions as TxClkINV.*
31	SDI RxON	I	**Serial Data Input:** Data is serially input through this pin. The input data is sampled on the rising edge of the SClk. . ***NOTES:*** *1. This pin is internally pulled down* *2. If configured in Hardware Mode, this pin functions as RxON.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
27	SDO RxMON	I/O	**Serial Data Output:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SClk and this pin is tri-stated upon completion of data transfer. ***NOTE:*** *If configured in Hardware Mode, this pin functions as RxMON.*
97	$\overline{\text{RESET}}$	I	**Register Reset:** Setting this input pin "Low" causes to reset the contents of the Command Registers to their default settings and default operating configuration ***NOTE:*** *This pin is internally pulled up.*
28	$\overline{\text{INT}}$ LOSMUT	I/O	**INTERRUPT Output:** A transition to “Low” indicates that an interrupt has been generated. The interrupt function can be disabled by setting the interrupt enable bit to “0” in the Channel Control Register. ***NOTES:*** 1. *In Hardware mode, this pin functions as LOSMUT.* 2. *This pin will remain asserted “Low” until the interrupt is serviced.*

JITTER ATTENUATOR INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
15	JA1	I	**Jitter Attenuator Select 1:** In Hardware Mode, this pin along with the pin JA0 configures the Jitter Attenuator as shown in the table. **JA0 / JA1 / Mode** **0 / 0 / 16 bit FIFO** **0 / 1 / 32 bit FIFO** **1 / 0 / Disable Jitter Attenuator** **1 / 1 / Disable Jitter Attenuator** ***NOTE:*** *This pin is internally pulled down.*
16	JATx/$\overline{\text{Rx}}$	I	**Jitter Attenuator Path Select** In Hardware Mode, tie this pin “High” to select the Jitter Attenuator in the Transmit Path . Connect this pin “Low” to select the Jitter Attenuator in the Receive Path. This applies to all channels. ***NOTE:*** *This pin is internally pulled down.*
14	JA0	I	**Jitter Attenuator Select 0:** In Hardware Mode, this pin along with pin JA1 configures the Jitter Attenuator as shown in the above table. ***NOTE:*** *This pin is internally pulled down.*

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
84	TxAVDD_0	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 0**
43	TxAVDD_1	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 1**
83	TxAGND_0	****	**Transmitter Analog GND - Channel 0**
44	TxAGND_1	****	**Transmitter Analog GND - Channel 1**
6	RxAVDD_0	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 0**
20	RxAVDD_1	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 1**
7	RxAGND_0	****	**Receiver Analog GND - Channel_0**
19	RxAGND_1	****	**Receive Analog GND - Channel 1**
86	JAAVDD_0	****	**Analog 3.3 V ± 5% VDD - Channel 0**
41	JAAVDD_1	****	**Analog 3.3 V ± 5% VDD - Channel 1**
85	JAAGND_0	****	**Analog GND - Channel 0**
42	JAAGND_1	****	**Analog GND - Channel 1**
13	AVDD	****	**Analog 3.3 V ± 5% VDD**
10	AGND	****	**Analog GND**

DIGITAL POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	TxVDD_0	****	**Transmitter 3.3 V ± 5% VDD Channel 0**
57	TxVDD_1	****	**Transmitter 3.3 V ± 5% VDD Channel 1**
68	TxGND_0	****	**Transmitter GND - Channel 0**
58	TxGND_1	****	**Transmitter GND - Channel 1**
89	RxDVDD_0	****	**Receiver 3.3 V ± 5% VDD - Channel 0**
38	RxDVDD_1	****	**Receiver 3.3 V ± 5% VDD - Channel 1**
90	RxDGND_0	****	**Receiver Digital GND - Channel 0**
37	RxDGND_1	****	**Receiver Digital GND - Channel 1**
87	JADVDD_0	****	**Jitter Attenuator 3.3 V ± 5% VDD - Channel 0**
40	JADVDD_1	****	**Jitter Attenuator 3.3 V ± 5% VDD - Channel 188**
88	JADGND_0	****	**Jitter Attenuator Digital GND - Channel 0**
39	JADGND_1	****	**Jitter Attenuator Digital GND - Channel 1**
61	DVDD	****	**Digital VDD 3.3.v ± 5%**
62	DVDD	****	**Digital VDD 3.3.v ± 5%**

DIGITAL POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
67	DVDD	****	**Digital VDD 3.3.v ± 5%**
59	DGND	****	**Digital GND**
64	DGND	****	**Digital GND**
65	DGND	****	**Digital GND**

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5+0.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^0C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^0C	linear airflow 0 ft./min
ThetaJA	Thermal Resistance		20	$^0C/W$	linear air flow 0ft/min
ThetaJC			6	$^0C/W$	
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating		2000	V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*

TABLE 2: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current (Measured while transmitting and receiving all 1's)		260	340	mA
P_{DD}	Power Dissipation		860	1200	mW
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, I_{OUT} = - 4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs and outputs are TTL 5V compliant.*

2.0 TIMING CHARACTERISTICS

FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75L02 (DUAL-RAIL DATA)

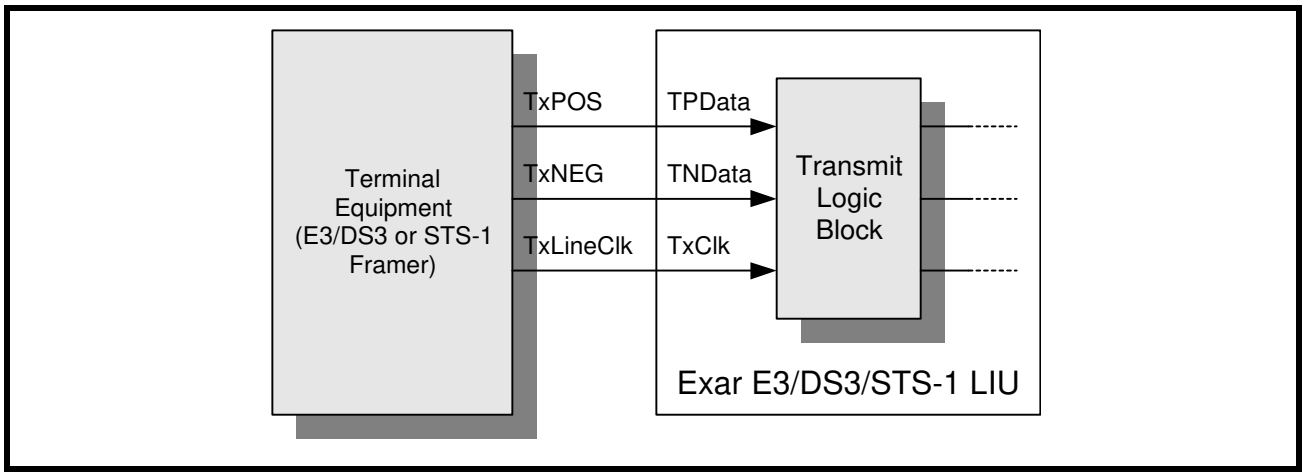
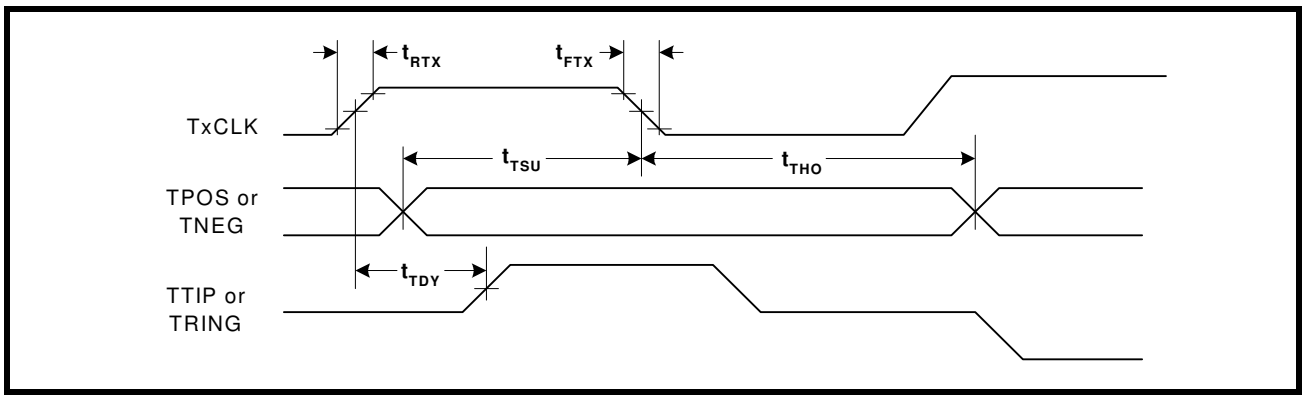
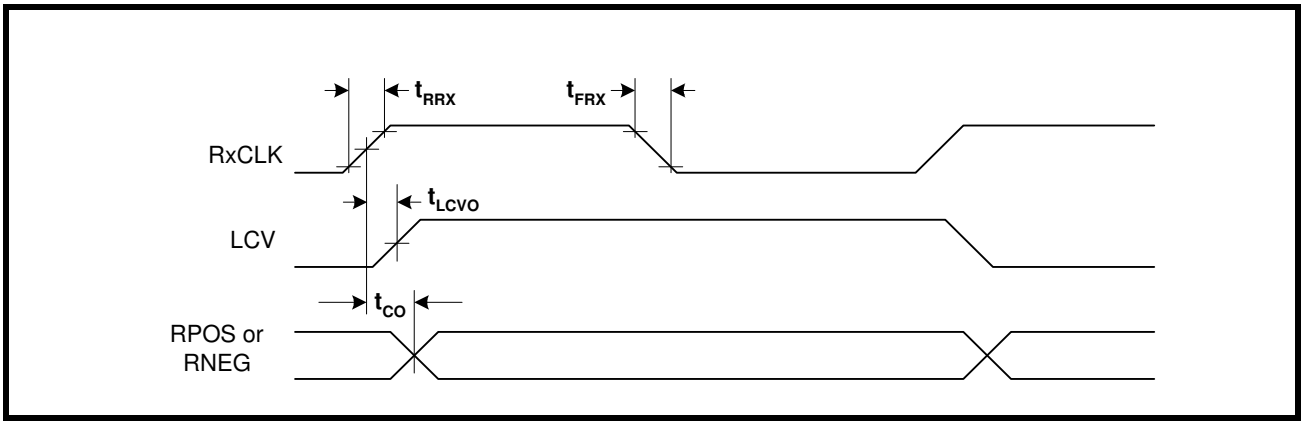


FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING



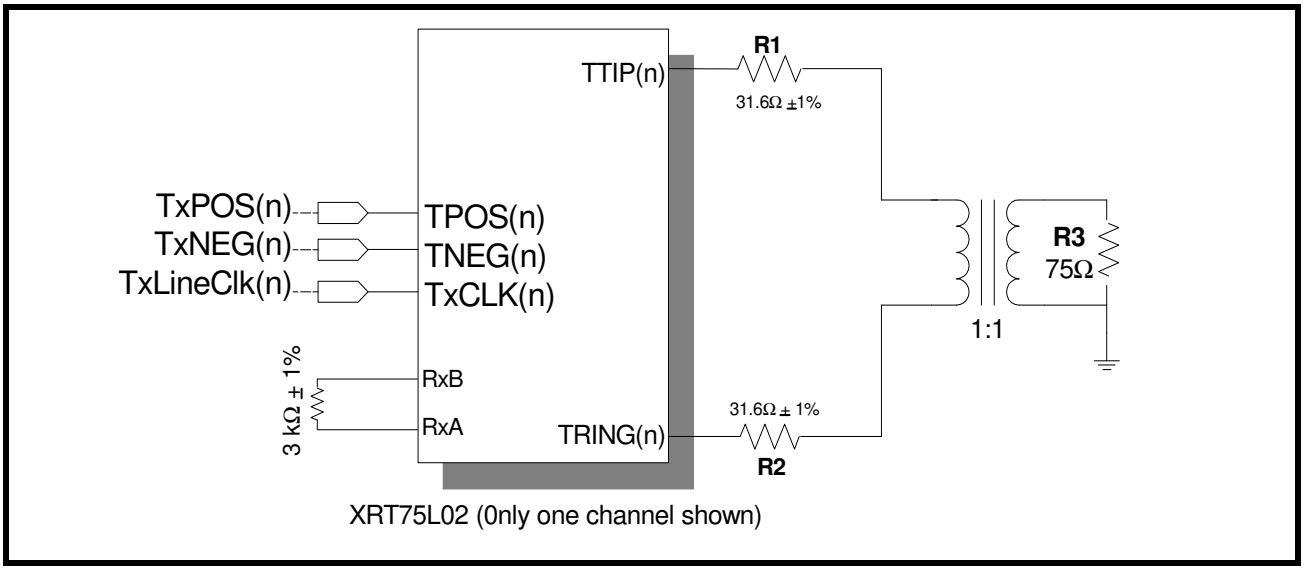
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle E3 DS3 STS-1	30	50 34.368 44.736 51.84	70	% MHz MHz MHz
t_{RTX}	TxCLK Rise Time (10% to 90%)			4	ns
t_{FTX}	TxCLKFall Time (10% to 90%)			4	ns
t_{TSU}	TPOS/TNEG to TxCLK falling set up time	3			ns
t_{THO}	TPOS/TNEG to TxCLK falling hold time	3			ns
t_{TDY}	TTIP/TRINGto TxCLK rising propagation delay time		8		ns

FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle E3 DS3 STS-1	45	50 34.368 44.736 51.84	55	% MHz MHz MHz
t_{RRX}	RxCLK rise time (10% o 90%)		2	4	ns
t_{FRX}	RxCLKfalling time (10% to 90%)		2	4	ns
t_{CO}	RxCLKto RPOS/RNEG delay time			4	ns
t_{LCVO}	RxCLK to rising edge of LCV output delay		2.5		ns

FIGURE 6. TRANSMIT INTERFACE CIRCUIT FOR E3, DS3 AND STS-1 RATES



3.0 LINE SIDE CHARACTERISTICS:

3.1 E3 line side parameters:

The XRT75L02 line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

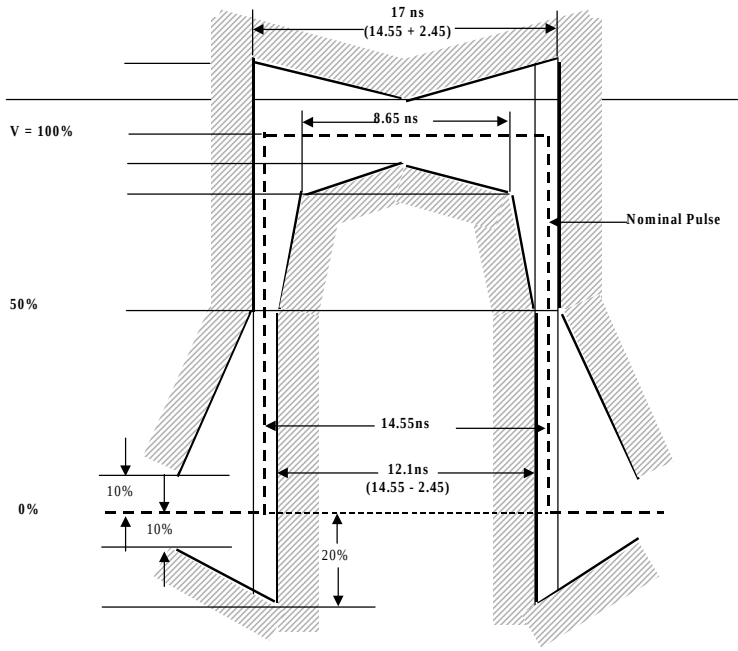


TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)		1200		feet
Interference Margin	-20	-16		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.30		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

NOTE: *The above values are at*

TA = 25^0C and V_{DD} = 3.3 V± 5%.

FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

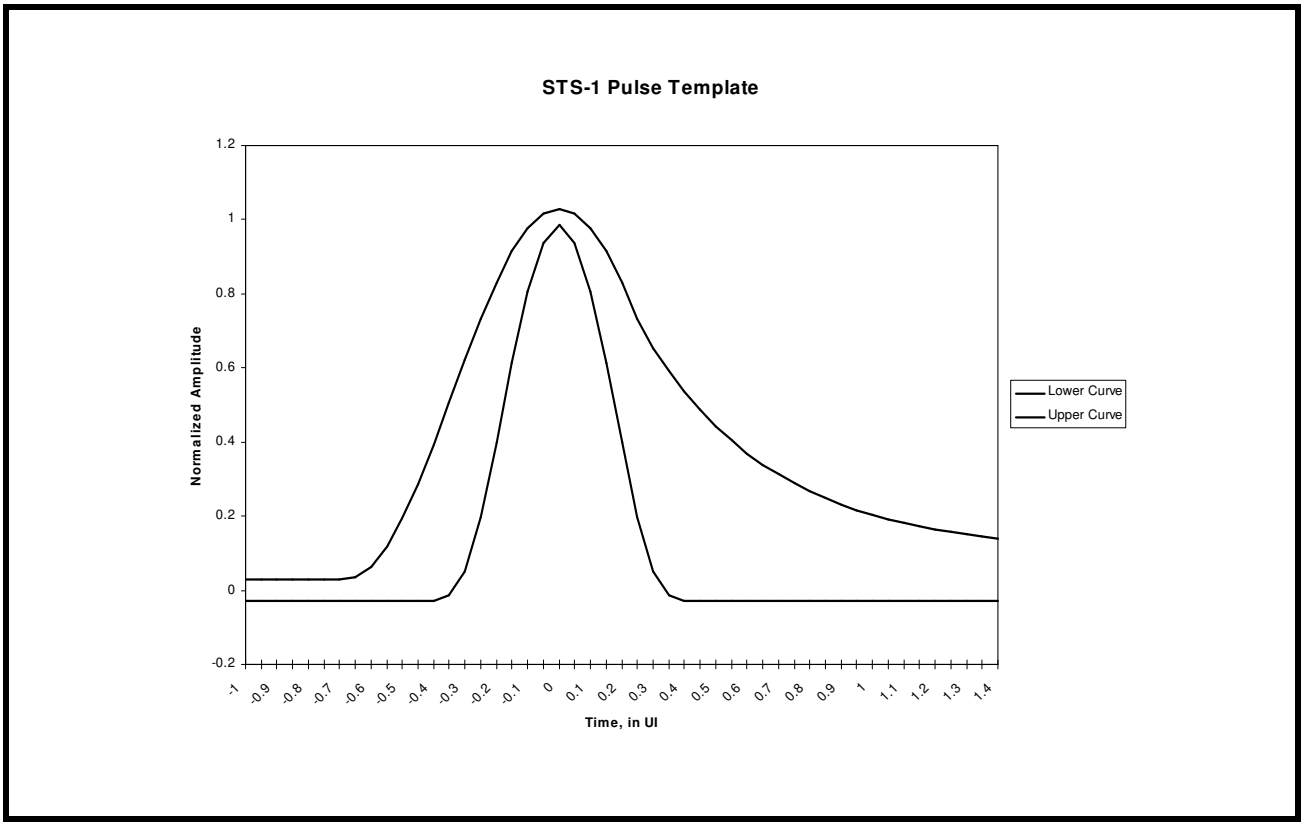


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.0$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.0$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \times e^{-2.4[T-0.26]}$

TABLE 5: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)		0.75		V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15	0.79		UI_{pp}

NOTE: *The above values are at*

TA = 25^0C and V_{DD} = 3.3 V ± 5%.

FIGURE 9. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

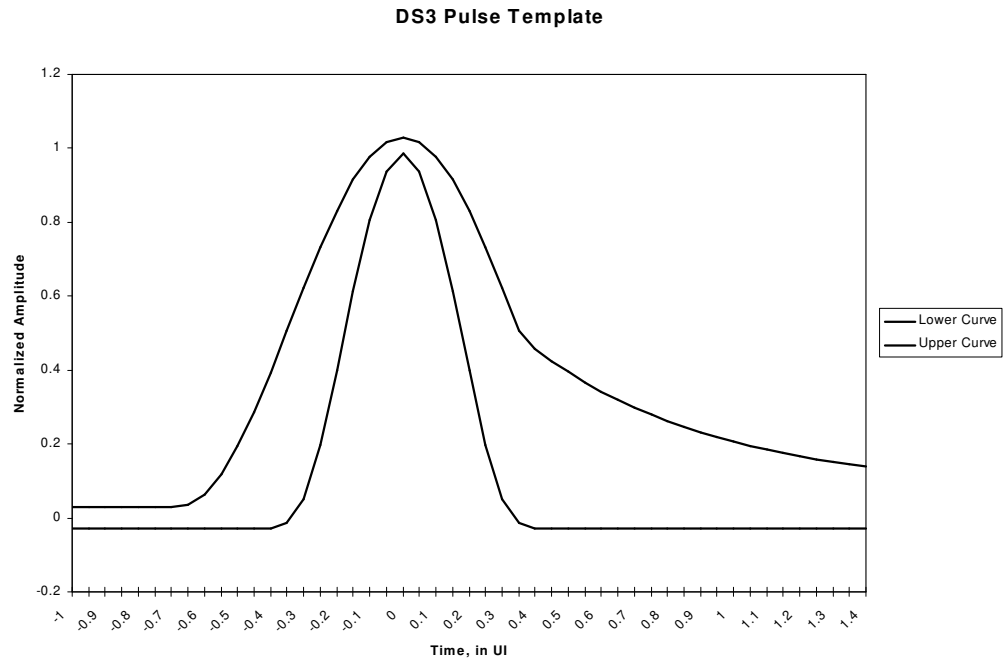


TABLE 6: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.0$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.0$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)		0.75		V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)		0.60		UI_{pp}

NOTE: *The above values are at*

TA = 25^0C and V_{DD} = 3.3V ± 5%.

FIGURE 10. MICROPROCESSOR SERIAL INTERFACE STRUCTURE

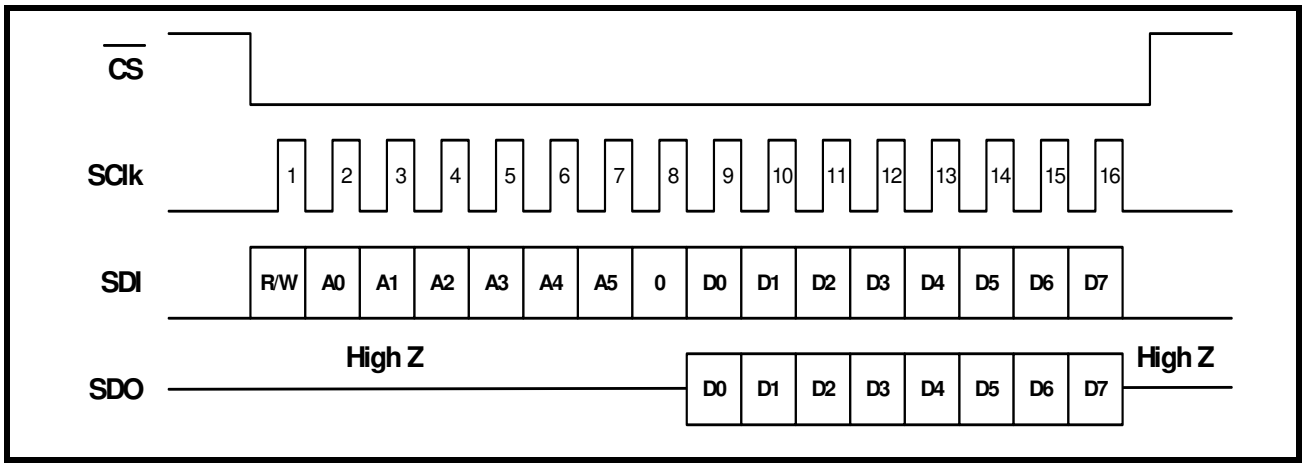


FIGURE 11. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

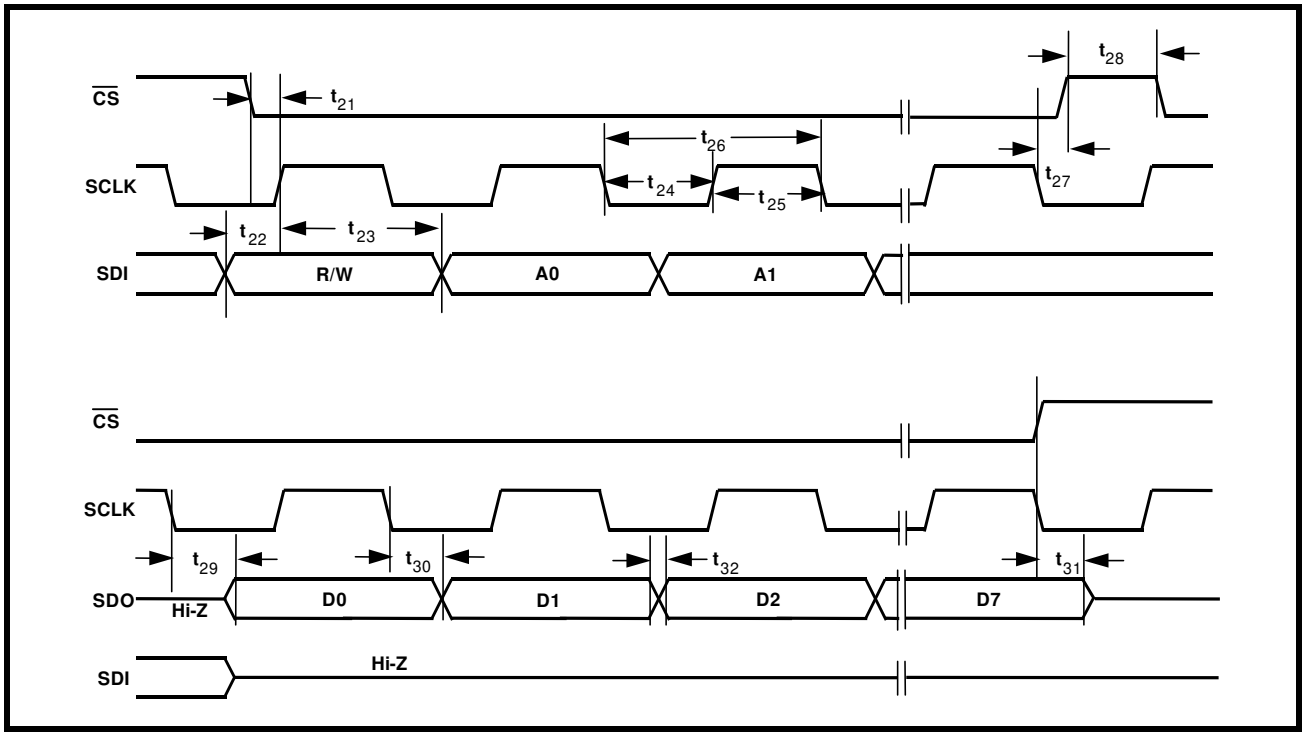


TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS (T_A = 25^{0}C, V_{DD}=3.3V± 5% AND LOAD = 10PF)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time		25		ns
t_{25}	SClk "High" Time		25		ns
t_{26}	SClk Period		50		ns
t_{27}	Falling Edge of SClk to rising edge of $\overline{CS}$	0			ns
t_{28}	$\overline{CS}$ "Inactive" Time	50			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			20	ns
t_{30}	Falling Edge of SClk to SDO Invalid Time			10	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z		10		ns
t_{32}	Rise/Fall time of SDO Output			5	ns