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THREE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

JULY 2003 *REV. 1.0.4*

GENERAL DESCRIPTION

The XRT75L03 is a three-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/STS-1 applications. It incorporates 3 independent Receivers, Transmitters and Jitter Attenuators in a single 128 pin LQFP package.

Each channel of the XRT75L03 can be independently configured to operate in the data rate, E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75L03's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75L03 incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

The XRT75L03 provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75L03 supports local, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

FEATURES

RECEIVER:

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be turned on or off
- Transmitters provide Current Output Drive

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator for each channel
- Jitter Attenuator can be selected in Receive or Transmit paths
- Meets ETSI TBR 24 Jitter Transfer Requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- 16 or 32 bits selectable FIFO size
- Jitter Attenuator can be disabled

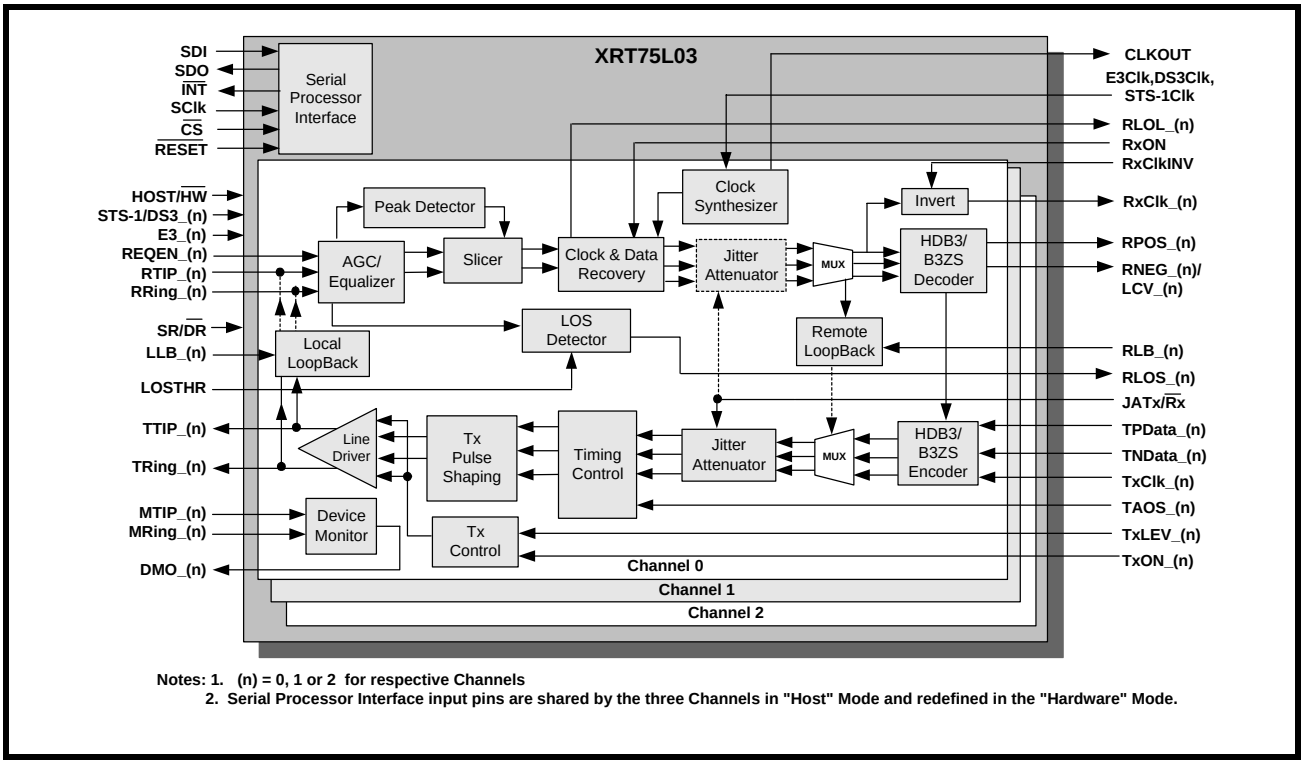
CONTROL AND DIAGNOSTICS:

- 5 wire Serial Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring
- Hardware Mode for control and configuration
- Each channel supports Local, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant digital inputs
- Available in 128 pin LQFP Package
- - 40°C to 85°C Industrial Temperature Range

APPLICATIONS

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75L03



Notes: 1. (n) = 0, 1 or 2 for respective Channels
2. Serial Processor Interface input pins are shared by the three Channels in "Host" Mode and redefined in the "Hardware" Mode.

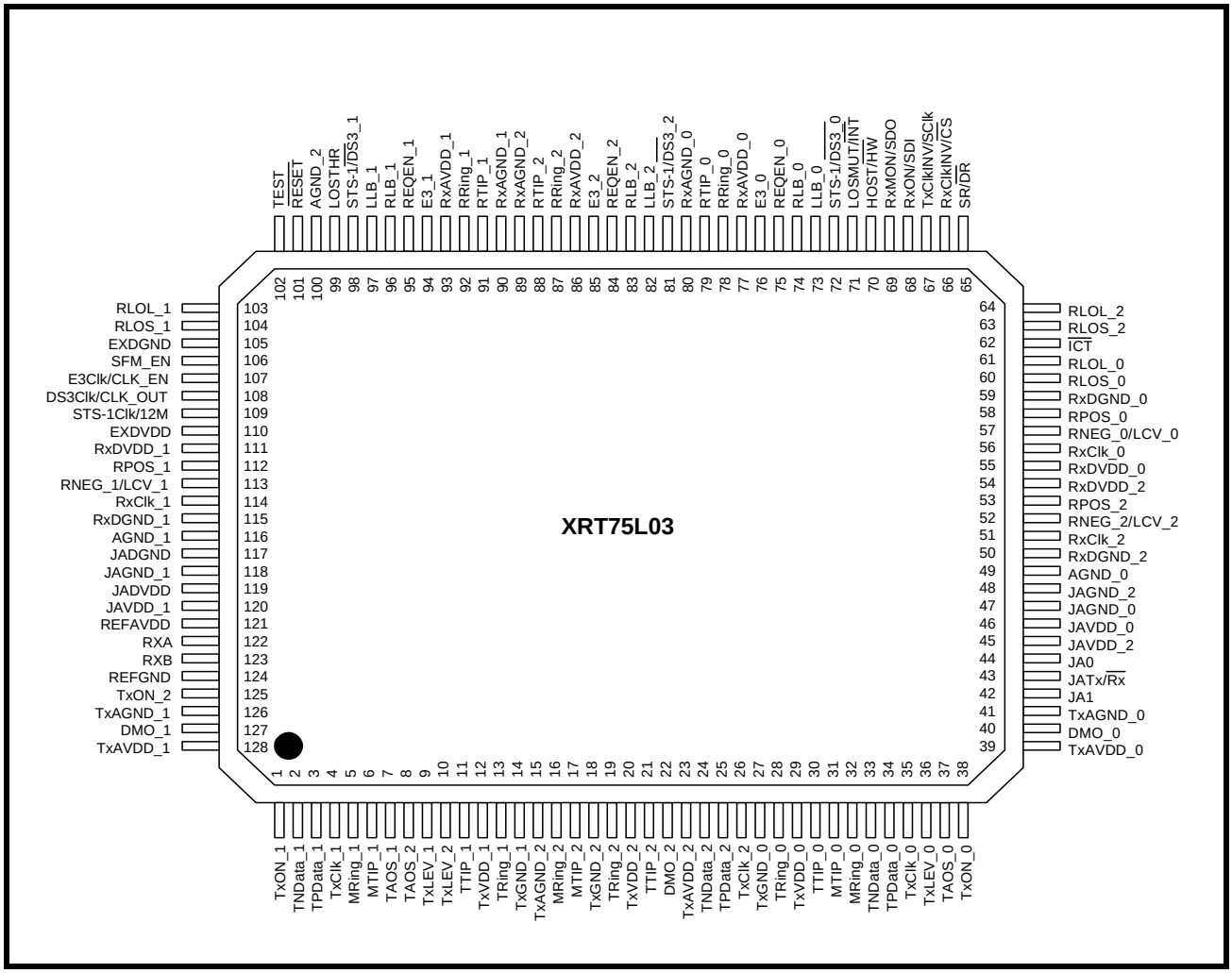
TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

FIGURE 2. PIN OUT OF THE XRT75L03



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L03IV	128 Pin LQFP	- 40°C to + 85°C

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PIN DESCRIPTIONS (BY FUNCTION)

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
38 1 125	TxON_0 TxON_1 TxON_2	I	**Transmitter ON Input - Channel 0:** **Transmitter ON Input - Channel 1:** **Transmitter ON Input - Channel 2:** These input pins are used to either enable or disable the Transmit Output Driver corresponding to Channel_n. "Low" - Disables the Transmit Output Driver of the corresponding Channel. In this setting, the corresponding TTIP_n and TRING_n output pins will be tri-stated. "High" - Enables the Transmit Output Driver of the corresponding Channel. In this setting, the corresponding TTIP_n and TRING_n output pins will be enabled. ***NOTES:*** *1. Even when the XRT75L03 is configured in HOST mode, these pins will be active. To enable software control of the Transmit Output Driver outputs, pull these pins "High".* *2. When Transmitters are turned off either in Host or Hardware mode, the TTIP and TRing outputs are Tri-stated.* *3. These pins are internally pulled "High"*
35 4 26	TxClk_0 TxClk_1 TxClk_2	I	**Transmit Clock Input - Channel 0:** **Transmit Clock Input f - Channel 1:** **Transmit Clock Input - Channel 2:** These input pins have two functions: • They function as the timing source for the Transmit Section of the corresponding channel within the XRT75L03. • They also are used by the Transmit Section of the LIU IC to sample the corresponding TPDATA_n and TNDATA_n input pin. ***NOTE:*** *The user is expected to supply a 44.736MHz ± 20ppm clock signal (for DS3 applications), 34.368MHz ± 20 ppm clock signal (for E3 applications) or a 51.84MHz ± 4.6ppm clock signal (for STS-1, Stratum 3E or better applications).*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
34 3 25	TPDATA_0/TxDATA_0 TPDATA_1/TxDATA_1 TPDATA_2/TxDATA_2	I	**Transmit Positive Data Input - Channel 0**: **Transmit Positive Data Input - Channel 1**: **Transmit Positive Data Input - Channel 2**: Transmit Positive Data/Data Input - Channel n: The function of these input pins depends upon whether the corresponding channel has been configured to operate in the Single-Rail or Dual-Rail Mode. Single Rail Mode - Transmit Data Input - Channel n: If the Channel has been configured to operate in the Single-Rail Mode, then all transmit output data will be serially applied to this input pin. This signal will latched into the Transmit Section circuitry upon either the rising or falling edge of the TxCLK_n signal, depending upon user configuration. In the Single-Rail Mode, the Transmit Section of the LIU IC will then encode this data into either the B3ZS line code (for DS3 and STS-1 applications) or the HDB3 line code (for E3 applications). **Dual Rail Mode - Transmit Positive Data Input - Channel n:** If the Channel has been configured to operate in the Dual-Rail Mode, then the user should apply a pulse to this input pin, anytime the Transmit Section of the LIU IC is suppose to generate and transmit a positive-polarity pulse onto the line. This signal will be latched into the Transmit Section circuitry upon either the rising or falling edge of the TxCLK_n signal, depending upon user configuration. In the Dual-Rail Mode, the Transmit Section of the LIU IC will NOT encode this data into either the B3ZS or HDB3 line codes. If the user configures the LIU IC to operate in the Dual-Rail Mode, then B3ZS/HDB3 encoding must have already been done prior to providing the transmit output data to this input pin.
33 2 24	TNData_0 TNData_1 TNData_2	I	**Transmit Negative Data Input - Channel 0:** **Transmit Negative Data Input - Channel 1:** **Transmit Negative Data Input - Channel 2:** If a Channel has been configured to operate in the Dual-Rail Mode, then the user should apply a pulse to this input pin anytime the Transmit Section of the LIU IC is suppose to generate and transmit a negative-polarity pulse onto the line. This signal will be latched into the Transmit Section circuitry upon either the rising or falling edge of the TxCLK_n signal, depending upon user configuration. ***NOTE:*** *If the Channel has been configured operate in the Single-Rail Mode, then this input pin has no function, and should be tied to GND.*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
37 7 8	TAOS_0 TAOS_1 TAOS_2	I	**Transmit "All Ones" Input - Channel 0:** **Transmit "All Ones" Input - Channel 1:** **Transmit "All Ones" Input - Channel 2:** These input pin are used to configure the Transmit Section of the corresponding channel to generate and transmit an unframed "All Ones" pattern via the DS3, E3 or STS-1 line signal to the remote terminal equipment. When this configuration is implemented the Transmit Section will ignore the data that it is accepting from the System-side equipment and will overwrite this data will the "All Ones" Pattern. "Low" - Does not configure the channel to transmit an unframed "All Ones" Pattern to the remote terminal equipment. In this mode, the Transmit Section of the Channel will output data based upon the signals that are applied to the TxPOS_n and TxNEG_n input pins. "High" - Configures the Channel to transmit an unframed "All Ones" Pattern to the remote terminal equipment. In this mode, the Transmit Section will override the data that is applied to the TxPOS_n and TxNEG_n input pins, and will proceed to generate and transmit an unframed "All Ones" pattern. *4. This input pin is ignored if the XRT75L03 is operating in the HOST Mode and should be tied to GND.* *5. These input pins are internally pulled down.*
36 9 10	TxLEV_0 TxLEV_1 TxLEV_2	I	**Transmit Line Build-Out Enable/Disable Select - Channel 0:** **Transmit Line Build-Out Enable/Disable Select - Channel 1:** **Transmit Line Build-Out Enable/Disable Select - Channel 2:** These input pins are used to enable or disable the Transmit Line Build-Out (e.g., pulse-shaping) circuit within the corresponding channel. The user should set these input pins either "High" or "Low" based upon the following guidelines. "Low" - If the cable length between the Transmit Output of the corresponding Channel and the DSX-3/STSX-1 location is 225 feet or less. "High" - If the cable length between the Transmit Output of the corresponding Channel and the DSX-3/STSX-1 location is 225 feet or more. ***NOTES:*** *1. These guidelines must be followed in order to insure that the Transmit Section of Channel_n will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE, or an STS-1 pulse that complies with the Pulse Template requirements per Telcordia GR-253-CORE.* *2. This input pin is inactive if the XRT75L03 has been configured to operate in the Host Mode, or if the corresponding channel has been configured to operate in the E3 Mode. If either of these cases are true, then tie this input pin to GND.* *3. These input pins are internally pulled "Low".*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
40 127 22	DMO_0 DMO_1 DMO_2	O	**Drive Monitor Output - Channel 0:** **Drive Monitor Output - Channel 1:** **Drive Monitor Output - Channel 2:** These output signals are used to indicate some sort of fault condition within the Transmit Output signal path. This output pin will toggle "High" anytime the Transmit Drive Monitor circuitry either, via the corresponding MTIP and MRING input pins or internally, detects no bipolar pulses via the Transmit Output line signal (e.g., via the TTIP_n and TRING_n output pins) for 128 bit-periods. This output pin will be driven "Low" anytime the Transmit Drive Monitor circuitry has detected at least one bipolar pulse via the Transmit Output line signal within the last 128 bit periods.
67	TxClkINV/ SClk	I	**Hardware Mode: Transmit Clock Invert** **Host Mode: Serial Clock Input:** **Hardware mode** This input pin is used to select the edge of the TxCLK_n input that the Transmit Section of all channels will use to sample the TPDATA_n and TNDATA_n input pins. Setting this input pin “High” configures all three Transmitters to sample the TPData_n and TNData_n data on the rising edge of the TxClk_n . Setting this input pin “Low” configures all three Transmitters to sample the TPData_n and TNData_n data on the falling edge of the TxClk_n . **Host Mode** In the Host Mode this pin functions as SClk input pin please refer to the pin descriptions for the Microprocessor interface.

TRANSMIT LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
30 11 21	TTIP_0 TTIP_1 TTIP_2	O	**Transmit TTIP Output - Positive Polarity Signal - Channel 0:** **Transmit TTIP Output - Positive Polarity Signal - Channel 1:** **Transmit TTIP Output - Positive Polarity Signal - Channel 2:** These output pins along with the corresponding TRING_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel, of the XRT75L03. Connect this signal and the corresponding TRING_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a "higher-voltage" than its corresponding TRING_n output pins. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a "lower-voltage" than its corresponding TRING_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the corresponding TxON_n input pin or bit-field is set to "0".*
28 13 19	TRing_0 TRing_1 TRing_2	O	**Transmit Ring Output - Negative Polarity Signal - Channel 0:** **Transmit Ring Output - Negative Polarity Signal - Channel 1:** **Transmit Ring Output - Negative Polarity Signal - Channel 2:** These output pins along with the corresponding TTIP_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel, within the XRT75L03. Connect this signal and the corresponding TTIP_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line. This output pin will be pulsed to a "lower-voltage" than its corresponding TTIP_n output pins. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line. This output pin will be pulsed to a "higher-voltage" than its corresponding TTIP_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the corresponding TxON_n input pin or bit-field is set to "0".*

TRANSMIT LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
31 6 17	MTIP_0 MTIP_1 MTIP_2	I	**Monitor Tip Input - Positive Polarity Signal - Channel 0:** **Monitor Tip Input - Positive Polarity Signal - Channel 1:** **Monitor Tip Input - Positive Polarity Signal - Channel 2:** These input pins along with MRING_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. To (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this pin MUST be connected to the corresponding TTIP_n output pin via a 274 ohm series resistor. Similarly, the MRING_n input pin MUST also be connected to its corresponding TRING_n output pin via a 274 ohm series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. These input pins are inactive if the user choose to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the XRT75L03 in is being operated in the Host Mode.*
32 5 16	MRing_0 MRing_1 MRing_2	I	**Monitor Ring Input - Channel 0:** **Monitor Ring Input - Channel 1:** **Monitor Ring Input - Channel 2:** These input pins along with MTIP_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. To (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this input pin MUST be connected to the corresponding TRING_n output pin via a 274 ohm series resistor. Similarly, the MTIP_n input pin MUST be connected to its corresponding TTIP_n output pin via a 274 ohm series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" to indicate a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. These input pins are inactive if the user chooses to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the XRT75L03 is being operated in the Host Mode.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
60 104 63	RLOS_0 RLOS_1 RLOS_2	O	**Receive Loss of Signal Output Indicator - Channel 0:** **Receive Loss of Signal Output Indicator - Channel 1:** **Receive Loss of Signal Output Indicator - Channel 2:** This output pin indicates whether or not the corresponding channel is declaring the Loss of Signal (LOS) Defect condition. "Low" - Indicates that the corresponding Channel is NOT currently declaring the LOS defect condition. "High" - Indicates that the corresponding Channel is currently declaring the LOS defect condition.
61 103 64	RLOL_0 RLOL_1 RLOL_2	O	**Receive Loss of Lock Output Indicator - Channel 0:** **Receive Loss of Lock Output Indicator - Channel 1:** **Receive Loss of Lock Output Indicator - Channel 2:** This output pin indicates whether or not the corresponding channel is declaring the Loss of Lock (LOL) Condition. "Low" - Indicates that the corresponding Channel is NOT declaring the LOL condition. "High" - Indicates that the corresponding Channel is currently declaring the LOL condition. ***NOTE:*** *The Receive Section of a given channel will declare the LOL condition anytime the frequency of the Recovered Clock (RCLK) signal differs from that of the E3CLK input clock signal (if the channel is operating in the E3 Mode), the DS3CLK input clock signal (if the channel is operating in the DS3 Mode) the STS-1CLK input clock signal (if the channel is operating in the STS-1 Mode), or that clock signal which is derived from the SFM Clock Synthesizer block (if the chip is operating in the Single-Frequency Mode) by 0.5% (or 5000ppm) or more.*
58 112 53	RPOS_0/RDATA_0 RPOS_1/RDATA_1 RPOS_2/RDATA_2	O	**Receive Positive Data Output - Receive Data Output - Channel 0:** **Receive Positive Data Output - Receive Data Output - Channel 1:** **Receive Positive Data Output - Receive Data Output - Channel 2:** The function of these output pins depends upon whether the channel/device has been configured to operate in the Single-Rail or Dual-Rail Mode. **Dual-Rail Mode - Receive Positive Polarity Data Output** If the channel/device has been configured to operate in the Dual-Rail Mode, then all positive-polarity data will be output via this output pin. The negative-polarity data will be output via the corresponding RNEG_n output pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a positive-polarity pulse via the RTIP/RRING input pins. The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal. **Single-Rail Mode - Receive Data Output** If the channel/device has been configured to operate in the Single-Rail Mode, then all Receive (or Recovered) data will be output via this output pin. The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
57 113 52	RNEG_0/LCV_0 RNEG_1/LCV_1 RNEG_2/LCV_2	O	**Receive Negative Data Output/Line Code Violation Indicator - Channel 0:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 1:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 2:** The function of these pins depends on whether the XRT75L03 is configured in Single Rail or Dual Rail mode. **Dual-Rail Mode - Receive Negative Polarity Data Output** If the channel/device has been configured to operate in the Dual-Rail Mode, then all negative-polarity data will be output via this output pin. The positive-polarity data will be output via the corresponding RPOS_n output pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a negative-polarity pulse via the RTIP/RRING input pins. The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal. **Single-Rail Mode - Line Code Violation Indicator Output** If the channel/device has been configured to operate in the Single-Rail Mode, then this particular output pin will function as the Line Code Violation indicator output. In this configuration, the Receive Section of the Channel will pulse this output pin "High" for at least one RCLK period whenever it detects either an LCV (Line Code Violation) or an EXZ (Excessive Zero Event). The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal.
56 114 51	RxClk_0 RxClk_1 RxClk_2	O	**Receive Clock Output - Channel 0:** **Receive Clock Output - Channel 1:** **Receive Clock Output - Channel 2:** This output pin functions as the Receive or recovered clock signal. All Receive (or recovered) data will output via the RPOS_n and RNEG_n outputs upon the user-selectable edge of this clock signal. Additionally, if the device/channel has been configured to operate in the Single-Rail Mode, then the RNEG_n/LCV_n output pins will also be updated upon the user-selectable edge of this clock signal.
75 95 84	REQEN_0 REQEN_1 REQEN_2	I	**Receive Equalization Enable Input - Channel 0:** **Receive Equalization Enable Input - Channel 1:** **Receive Equalization Enable Input - Channel 2:** These input pins are used to either enable or disable the Receive Equalizer block within the Receive Section of the corresponding channel. "Low" - Disables the Receive Equalizer within the corresponding channel. "High" - Enables the Receive Equalizer within the corresponding channel. ***NOTES:*** *1. For virtually all applications, it is recommend that this input pin be pulled "High" and enable the Receive Equalizer.* *2. This input pin ignored and should be tied to GND if the XRT75L03 device has been configured to operate in the Host Mode.* *3. These input pins are internally pulled low.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
71	LOSMUT/ $\overline{\text{INT}}$	I/O	**Muting Upon LOS Enable/Interrupt Output Pin** This input pin is used to configure the Receive Section, in each of the three channels within the chip, to automatically pull their corresponding Recovered Data Output pins (e.g. RPOS_n and RNEG_n) to GND anytime and for the duration that the Receive Section declares the LOS defect condition. In other words, this feature if enabled will cause the Receive Channel to automatically mute the Recovered data anytime and for the duration that the Receive Section declares the LOS defect condition. "Low" - Disables the Muting upon LOS feature. In this setting the Receive Section will NOT automatically mute the Recovered Data whenever it is declaring the LOS defect condition. "High" - Enables the Muting upon LOS feature. In this setting the Receive Section will automatically mute the Recovered Data whenever it is declaring the LOS defect condition. ***NOTES:*** *1. This input pin is will function as the Interrupt Request output pin within the Microprocessor Serial Interface, if the XRT75L03 has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to each of the three (3) channels within the XRT75L03.*
99	LOSTHR	I	**Analog LOS Detector Threshold Level Select Input:** This input pin permits the user to select both of the following parameters for the Analog LOS Detector within each of the three Receive Sections within the XRT75L03 device. **1.** The Analog LOS Defect Declaration Threshold (e.g., the maximum signal level that the Receive Section of a given channel must detect before declaring the LOS Defect condition), and **2.** The Analog LOS Defect Clearance Threshold (e.g., the minimum signal level that the Receive Section of a given channel must detect before clearing the LOS Defect condition) Setting this input pin "High" selects one set of Analog LOS Defect Declaration and Clearance thresholds. Setting this input pin "Low" selects the other set of Analog LOS Defect Declaration and Clearance thresholds. Please see Table 10 for more details. ***NOTE:*** *This input pin is only active if at least one channel within the XRT75L03 has been configured to operate in the DS3 or STS-1 Modes.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	RxMON/ SDO	I	**Receiver Monitor Mode Enable:** This input pin permits the user to configure each of the three (3) Receive Sections within the XRT75L03 device, into the Receiver Monitor Mode. If the user configures each of the Receive Sections into the Receive Monitor Mode, then each of the Receiver Sections will be able to receive a nominal DSX-3/STSX-1 signal that has been attenuated by 20dB of flat loss along with 6dB of cable loss, in an error-free manner, and without declaring the LOS defect condition. "Low" - Configures each of the Receive Sections to operate in the Normal Mode. "High" - Configures each of the Receive Sections to operate in the Receive Monitor Mode. ***NOTES:*** *1. This input pin will function as the SDO (Serial Data Output pin within the Microprocessor Serial Interface) whenever the XRT75L03 has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to all three (3) of the channels within the XRT75L03.*
68	RxON/ SDI	I	**Receive ON:** This input pin permits the user to either turn on or turn off each of the three (3) Receive Sections within the XRT75L03. If the user turns on the Receive Sections of each channel, then all three channels will begin to receive the incoming DS3, E3 or STS-1 data-streams via the RTIP_n and RRING_n input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section (e.g., the AGC and Receive Equalizer blocks, Clock Recovery PLL, etc.) will be powered down. "Low" - Shuts off the Receive Sections within each of the three (3) Channels in the XRT75L03. "High" - Turns on the Receive Sections within each of the three (3) Channels in the XRT75L03. ***NOTES:*** *1. This input pin will function as the SDI (Serial Data Input pin within the Microprocessor Serial Interface) whenever the XRT75L03 has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to all three (3) of the channels within the XRT75L03 device.* *3. This pin is internally pulled low.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
66	RxClkINV/ $\overline{CS}$	I	Receive Clock Invert Input - Chip Selectl: In Hardware Mode is pin is used to configure the Receive Sections of the three (3) channels in the XRT75L03 to either output the recovered data via the RPOS_n or RNEG_n/LCV_n output pins upon either the rising or falling edge of the RCLK_n clock output signal. "Low" - Configures each of the Receive Sections to output the recovered data via the RPOS_n and RNEG_n/LCV_n output pins upon the rising edge of the RCLK_n output clock signal. "High" - Configures each of the Receive Sections to output the recovered data via the RPOS_n and RNEG_n/LCV_n output pins upon the falling edge of the RCLK_n output clock signal. ***NOTES:*** *1. This input pin will function as the $\overline{CS}$ (Chip Select Input pin) of the Microprocessor Serial Interface when the XRT75L03 has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to all three (3) of the channels within the XRT75L03.* *3. If the Receive Sections are configured to operate in the Single-Rail Mode, then the LCV_n output pin will be updated on the user-selected edge of the RCLK_n signal, per this configuration selection.*
106	SFM_EN	I	**Single Frequency Mode Enable:** This input pin is used to configure the XRT75L03 to operate in the SFM (Single Frequency) Mode. When this feature is invoked the Single-Frequency Mode Synthesizer will become active. By applying a 12.288MHz clock signal to pin 109, STS-1CLK/ 12M the XRT75L03 will, depending upon which mode the user has configured each of the three channels, generate all of the appropriate clock signals (e.g., 34.368MHz, 44.736MHz or 51.84. Further, the XRT75L03 internal circuitry will route each of these synthesized clock signals to the appropriate nodes of the corresponding three channels in the XRT75L03. "Low" - Disables the Single Frequency Mode. In this configuration setting, the user is required to supply to the E3CLK, DS3CLK or STS-1CLK input pins all of the relevant clock signals that are to be used within the chip. "High" - Enables the Single-Frequency Mode. A 12.288MHz clock signal MUST be applied to pin 109 (STS-1CLK/12M). ***NOTE:*** *This input pin is internally pulled low.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
107	E3Clk/ CLK_EN	I	E3 Reference Clock Input/SFM Clock Output Enable: The function of this chip depends upon whether or not the XRT75L03 has been configured to operate in the Single-Frequency Mode. **If NOT operating in the Single-Frequency Mode** If the XRT75L03 has NOT been configured to operate in the SFM (Single Frequency) Mode, and if at least one channel is to be operated in the E3 Mode, then a 34.368MHz clock signal must be applied to this input pin. If the user does not intend to operate the device in the SFM Mode nor operate any of the channels in the E3 Mode tie this input signal to GND. **If operating in the Single-Frequency Mode** If the XRT75L03 is operated in the SFM Mode and is to output a clock signal that is synthesized from the SFM Clock Synthesizer PLL so that the user's system can use this clock signal as a timing source, pull this input pin to a logic "High". If the user pull this input pin "High", then the XRT75L03 will output the line rate clock signal that has been synthesized for Channel 1, via pin 108 (DS3CLK/ CLK_OUT). For example, if Channel 1 is configured to operate in the STS-1 Mode and this input pin is pulled "High", then the XRT75L03 will output a 51.84MHz clock signal via the CLK_OUT pin.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
108	DS3Clk/ CLK_OUT	I/O	**DS3 Reference Clock Input/SFM Synthesizer Clock Output:** The function of this chip depends upon whether or not the XRT75L03 has been configured to operate in the SFM Mode. **If NOT operating in the Single-Frequency Mode** If the XRT75L03 has NOT been configured to operate in the SFM Mode, and if at least one channel of the XRT75L03 is configured in the DS3 Mode, then a clock signal with a frequency of 44.736 MHz ± 20ppm must be applied to this input pin. If the XRT75L03 is not configured to operate in the SFM Mode and none of the channels are to be operated in the DS3 Mode, tie this input signal to GND. **If operating in the Single-Frequency Mode** If the XRT75L03 is configured to operate in the SFM Mode, and if pin 107 (E3CLK/CLKEN) is pulled to a logic "High", then the SFM Clock Synthesizer PLL generated line rate clock signal for Channel 1 will be output via this output pin. In this mode, this particular output pin can be used by the user's system as a timing source.
109	STS-1Clk/ 12M	I	**STS-1 Reference Clock Input/12.288MHz SFM Reference Clock Input:** The function of this pin depends upon whether or not the XRT75L03 has been configured to operate in the SFM Mode. **If NOT operating in the Single-Frequency Mode** If the XRT75L03 has NOT been configured to operate in the SFM Mode and if at least one channel is intended to operate in the STS-1 Mode, then the user must supply a clock signal with a frequency of 51.84MHz ± 4.6ppm to this input pin If the XRT75L03 is not to be operatedin the SFM Mode and none of the channels are to be operated in the STS-1 Mode, tie this input signal to GND. **If operating in the Single-Frequency Mode** If the user has configured the XRT75L03 has been configured to operate in the SFM Mode a clock signal with a frequency of 12.288MHz ± 20ppm MUST be applied to this input pin. The SFM Synthesizer will then synthesize one of the appropriate line rate frequencies (e.g., 34.368MHz for E3, 44.736MHz for DS3, and 51.84MHz for STS-1) based upon this 12.288MHz Reference Clock source.

RECEIVE LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
79 91 88	RTIP_0 RTIP_1 RTIP_2	I	**Receive TIP Input - Channel 0:** **Receive TIP Input - Channel 1:** **Receive TIP Input - Channel 2:** These input pins along with the corresponding RRing_n input pin function as the Receive DS3/E3/STS-1 Line input signal receiver for a given channel of the XRT75L03. Cconnect this signal and the corresponding RRING_n input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "higher-voltage" than its corresponding RRING_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "lower-voltage" than its corresponding RRING_n input pin.
78 92 87	RRing_0 RRing_1 RRing_2	I	**Receive Ring Input - Channel 0:** **Receive Ring Input - Channel 1:** **Receive Ring Input - Channel 2:** These input pins along with the corresponding RTIP_n input pin function as the Receive DS3/E3/STS-1 Line input signal receiver for a given channel of the XRT75L03. Connect this signal and the corresponding RTIP_n input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "lower-voltage" than its corresponding RTIP_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "higher-voltage" than its corresponding RTIP_n input pin.

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
107	E3Clk/ CLK_EN	I	**E3 Clock Input (34.368 MHz ± 20 ppm):** If all the 3 channels or any one of the channels is configured in E3 mode, a reference clock 34.368 MHz ± 20 ppm is input to this pin.. **Clock Output Enable:** If the Single Frequency Mode is selected, tie this pin “High” to enable the clock output through the CLK_OUT pin (pin 108).
108	DS3Clk/ CLK_OUT	I/O	**DS3 Clock Input (44.736 MHz ± 20 ppm):** If all the 3 channels or any one of the channels is configured in DS3 mode, a reference clock 44.736 MHz ± 20 ppm is input to this pin. **Clock Output:** When the Single Frequency Mode is enabled, this pin is configured as the clock output from Channel 1.This clock frequency is determined by the Channel 1 setting.. ***NOTE:*** *This low jitter output clock can be used as the input clock source for the framer device. thus eliminating the need for a separate clock source for the framer.*
109	STS-1Clk/ 12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm):** If all the 3 channels or any one of the channels is configured in STS-1 mode, a reference clock 51.84 MHz ± 20 ppm is input to this pin. **Single Frequency Mode Clock Input:** In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the rates (E3 or DS3 or STS-1).

GENERAL CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
65	SR/$\overline{DR}$	I	**Single-Rail/Dual-Rail Select Input - Chip Level** This input pin is used to configure the XRT75L03 to operate in either the Single-Rail or Dual-Rail Mode. If the XRT75L03 is configured to operate in the Single-Rail Mode, then all of the following will happen. • All of the B3ZS/HDB3 Encoder and Decoder blocks in the XRT75L03 will be enabled. • The Transmit Section of each channel will accept all of the outbound data from the System-side Equipment via the TPDATA_n (or TxDATA_n) input pin. • The Receive Section of each channel will output all of the recovered data to the System-side Equipment via the RPOS output pin. • Each of the RNEG/LCV output pins will now function as the LCV (Line Code Violation or Excessive Zero Event) indicator output pin. If the user configures the device to operate in the Dual-Rail Mode, then all of the following will happen. • All of the B3ZS/HDB3 Encoder and Decoder blocks in the XRT75L03 will be disabled.· • The Transmit Section of each channel will accept positive-polarity data via the TPDATA_n input pin, and negative-polarity data via the TNDATA_n input pin. • The Receive Section of each channel will pulse the RPOS_n output pin "High" for one period of RCLK_n for each time a positive-polarity pulse is received via the RTIP_n/RRING_n input pins • Likewise, the Receive Section of each channel will also pulse the RNEG_n output pin "High" for one period of RCLK_n for each time a negative-polarity pulse is received via the RTIP_n/RRING_n input pins. "Low" - Configures the XRT75L03 device to operate in the Dual-Rail Mode. "High" - Configures the XRT75L03 device to operate in the Single-Rail Mode. ***NOTES:*** *1. This input pin is ignored and should be tied to GND if the XRT75L03 has been configured to operate in the Host Mode.* *2. This pin is internally pulled "Low".*
76 94 85	E3_0 E3_1 E3_2	I	**E3 Mode Select Input - Channel 0** **E3 Mode Select Input - Channel1** **E3 Mode Select Input - Channel 2** This input pin, along with the corresponding STS-1/$\overline{DS3}$_n input pin is used the to configure a given channel within the XRT75L03 into either the DS3, E3 or STS-1 Modes. "High" - Configures the corresponding channel to operate in the E3 Mode. "Low" - Configures the corresponding channel to operate in either the $\overline{DS3}$ or STS-1 Modes, depending upon the setting of the corresponding STS-1/$\overline{DS3}$_n input pin. ***NOTES:*** *1. This input pin is ignored and should be tied to GND if the XRT75L03 has been configured to operate in the Host Mode.* *2. This input pin is internally pulled low.*

GENERAL CONTROL PINS

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>72
98
81</td><td>STS-1/$\overline{\text{DS3}}$_0
STS-1/$\overline{\text{DS3}}$_1
STS-1/$\overline{\text{DS3}}$_2</td><td>I</td><td>STS-1/DS3 Select Input - Channel 0
STS-1/DS3 Select Input - Channel 1
STS-1/DS3 Select Input - Channel 2
This input pin, along with the corresponding E3_n input pin is used the to configure a given channel within the XRT75L03 into either the DS3, E3 or STS-1 Modes.
"High" - Configures the corresponding channel to operate in the STS-1 Mode provided that the corresponding E3_n input pin is pulled "Low".
"Low" - Configures the corresponding channel to operate in DS3 Mode provided that the corresponding E3_n input pin is pulled "Low".
NOTES:
1. This input pin is ignored and should be tied to GND if the XRT75L03 has been configured to operate in the Host Mode or if the corresponding E3_n input pin is pulled "High".
2. This input pin is internally pulled low.</td></tr>
<tr><td>74
96
83</td><td>RLB_0
RLB_1
RLB_2</td><td>I</td><td>Remote Loop-back - RLB Input - Channel 0:
Remote Loop-back - RLB Input - Channel 1:
Remote Loop-back - RLB Input - Channel 2:
This input pin along with LLB_n is used to configure different Loop-Back modes.
<table><tr><th>RLB_n</th><th>LLB_n</th><th>Loopback Mode</th></tr><tr><td>0</td><td>0</td><td>Normal (No Loop-Back) Mode</td></tr><tr><td>0</td><td>1</td><td>Analog Loop-Back Mode</td></tr><tr><td>1</td><td>0</td><td>Remote Loop-Back Mode</td></tr><tr><td>1</td><td>1</td><td>Digital Local Loop-Back Mode</td></tr></table>NOTE: This input pin is ignored and should be connected to GND if the XRT75L03 is operating in the HOST Mode.</td></tr>
<tr><td>73
97
82</td><td>LLB_0
LLB_1
LLB_2</td><td>I</td><td>Loop-Back Select - LLB Input - Channel 0
Loop-Back Select - LLB Input - Channel 1
Loop-Back Select - LLB Input - Channel 2
Please see description above for RLB_n</td></tr>
<tr><td>102</td><td>TEST</td><td>****</td><td>Factory Test Mode Input Pin
This pin must be connected to GND for normal operation.
NOTE: This input pin is internally pulled "Low".</td></tr>
</table>

GENERAL CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
62	$\overline{ICT}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, set this pin "High". ***NOTE:*** *This pin is internally pulled "High".*
70	HOST/$\overline{HW}$	I	**HOST/Hardware Mode Select:** Tie this pin "High" to configure the XRT75L03 in HOST mode. Tie this "Low" to configure in Hardware mode. When the XRT75L03 is configured in HOST mode, the states of many of the discrete input pins are controlled by internal register bits. ***NOTE:*** *This pin is internally pulled up.*

CONTROL AND ALARM INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
122	RXA	****	**External Resistor of 3.01K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.
123	RXB	****	**External Resistor of 3.01K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.

JITTER ATTENUATOR INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
44	JA0	I	**Jitter Attenuator Select 0:** In Hardware Mode, this pin along with pin 42 configures the Jitter Attenuator as shown in the table below.

JA0	JA1	Mode
0	0	16 bit FIFO Depth
0	1	32 bit FIFO Depth
1	0	Disable Jitter Attenuator
1	1	Disable Jitter Attenuator

NOTES:

1. *The setting of these input pins applies globally to all three (3) channels in the XRT75L03.*
2. *This input pin is ignored and should be tied to GND if the XRT75L03 is configured to operate in the Host Mode.*

JITTER ATTENUATOR INTERFACE

42	JA1	I	**Jitter Attenuator Select 1:** Please see the Description above for JA0
43	JATx/$\overline{\text{Rx}}$	I	Jitter Attenuator in Transmit/Receive Path Select Input: This input pin is used to configure the Jitter Attenuator to operate in either the Transmit or Receive path within each of the three (3) channels of the XRT75L03. "Low" - Configures the Jitter Attenuator within each channel to operate in the Receive Path. "High" - Configures the Jitter Attenuator within each channel to operate in the Transmit Path. ***NOTES:*** *1. The setting of this input pin applies globally to all three (3) channels of the XRT75L03.* *2. This input pin is ignored and should be tied to GND if the XRT75L03 is configured to operate in the Host Mode or if the Jitter Attenuators are disabled.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	SDO/RxMON	I/O	**Microprocessor Serial Interface - Serial Data Output:** This pin serially outputs the contents of a specified on-chip Command Register during READ Operations via the Microprocessor Serial Interface. The data which is output via this pin is updated upon the falling edge of the SCLK clock signal. This output pin will be tri-stated upon completion of a given READ operation. ***NOTE:*** *This pin functions as the RxMON input pin if the XRT75L03 has been configured to operate in the Hardware Mode.*
68	SDI/RxON	I	**Microprocessor Serial Interface - Serial Data Input:** This input pin functions as the Serial Data Input pin for the Microprocessor Serial Interface. In particular, this input pin will accept all of the following data in a serial manner during READ and WRITE operations with the Microprocessor Serial Interface. • The READ/WRITE indicator bit. • The Address Value of the Targeted Command Register for this particular READ or WRITE operation. • The Data to be written into the targeted Command Register for a given WRITE operation. All data that is applied to this input will be sampled upon the rising edge of the SCLK input clock signal. ***NOTE:*** *This input pin will function as the RxON input pin if the XRT75L03 has been configured to operate in the Hardware Mode.*