



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



GENERAL DESCRIPTION

The XRT75L04D is a four-channel fully integrated Line Interface Unit (LIU) with Sonet Desynchronizer for E3/DS3/STS-1 applications. It incorporates four independent Receivers, Transmitters and Jitter Attenuators in a single 176 pin QFP package.

Each channel of the XRT75L04D can be configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) rates that are independent of each other. Each transmitter can be turned off and tri-stated for redundancy support and for conserving power.

The XRT75L04D's differential receivers provide high noise interference margin and are able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75L04D incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Telcordia GR-499, GR-253 specifications. Also, the jitter attenuator can be used for clock smoothing in SONET STS-1 to DS3 de-mapping.

The XRT75L04D provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75L04D supports local, remote and digital loop-backs. The XRT75L04D also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES**RECEIVER:**

- On chip Clock and Data Recovery circuit for high input jitter tolerance.
- Meets the jitter tolerance requirements as specified in ITU-T G.823_1993 for E3 and Telcordia GR-499-CORE for DS3 applications.
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation.
- On chip B3ZS/HDB3 encoder and decoder that can either be enabled or disabled.
- On-chip clock synthesizer generates the appropriate rate clock from a single frequency XTAL.

- Provides low jitter clock outputs for either DS3, E3 or STS-1 rates.

TRANSMITTER:

- Compliant with Telcordia GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Transmitters can be turned on or off.

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator.
- Jitter Attenuators can be selected in Receive or Transmit paths.
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755, GR-253 and GR-499-CORE, 1995 standards.
- Meets ETSI TBR 24 Jitter Transfer Requirements.
- 16, 32 or 128 bits selectable FIFO size.
- Meets the Wander specifications described in T1.105.03b.
- Jitter Attenuators can be disabled.

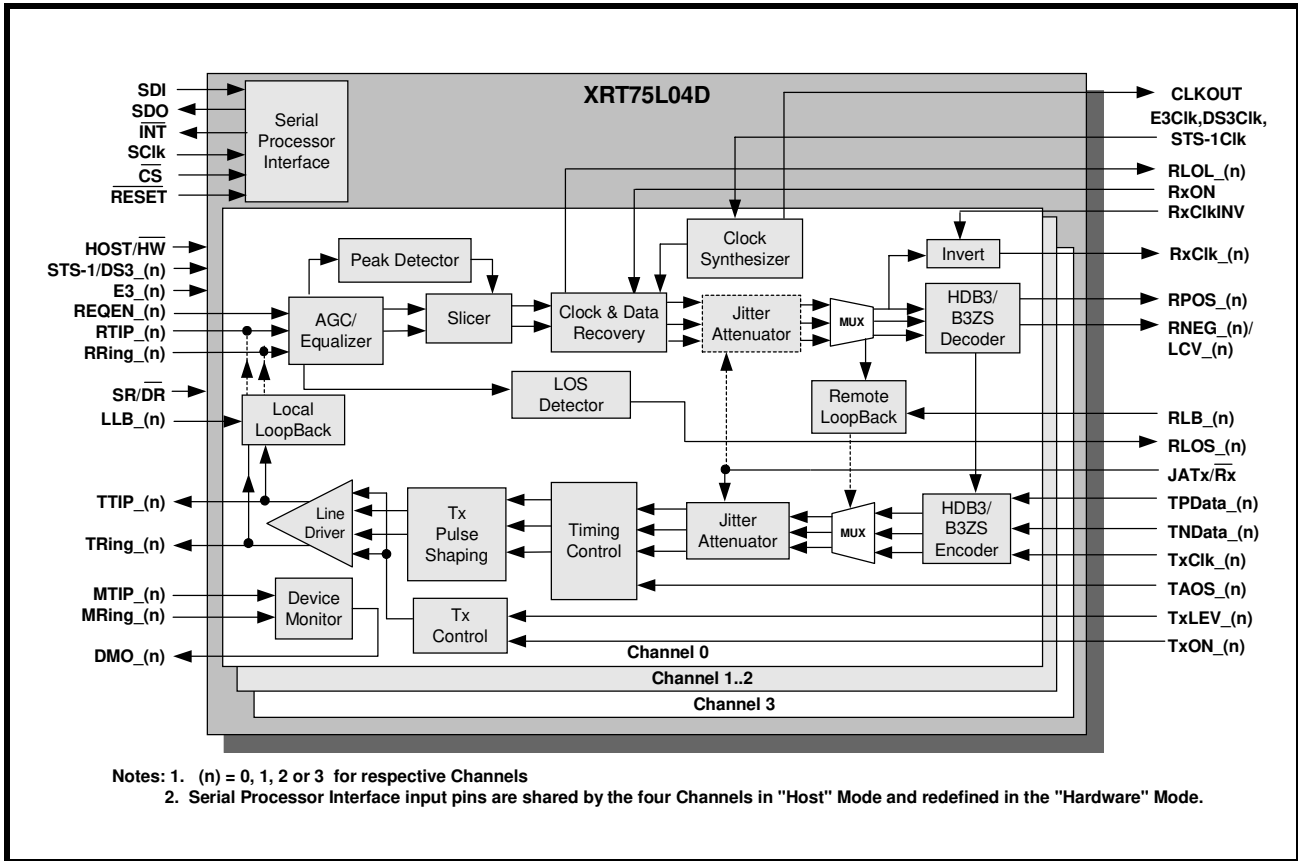
CONTROL AND DIAGNOSTICS:

- Serial Microprocessor Interface for control and configuration.
- Supports optional internal Transmit Driver Monitoring.
- PRBS error counter register to accumulate errors.
- Supports Local, Remote and Digital Loop-backs.
- Single 3.3 V \pm 5% power supply.
- 5 V Tolerant I/O.
- Maximum Power Dissipation 1.8W.
- Available in 176 pin QFP package
- - 40°C to 85°C Industrial Temperature Range.

APPLICATIONS

- E3/DS3 Access Equipment.
- STS1-SPE to DS3 Mapper.
- DSLAMs.
- Digital Cross Connect Systems.
- CSU/DSU Equipment.
- Routers.

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75L04D



TRANSMIT INTERFACE CHARACTERISTICS

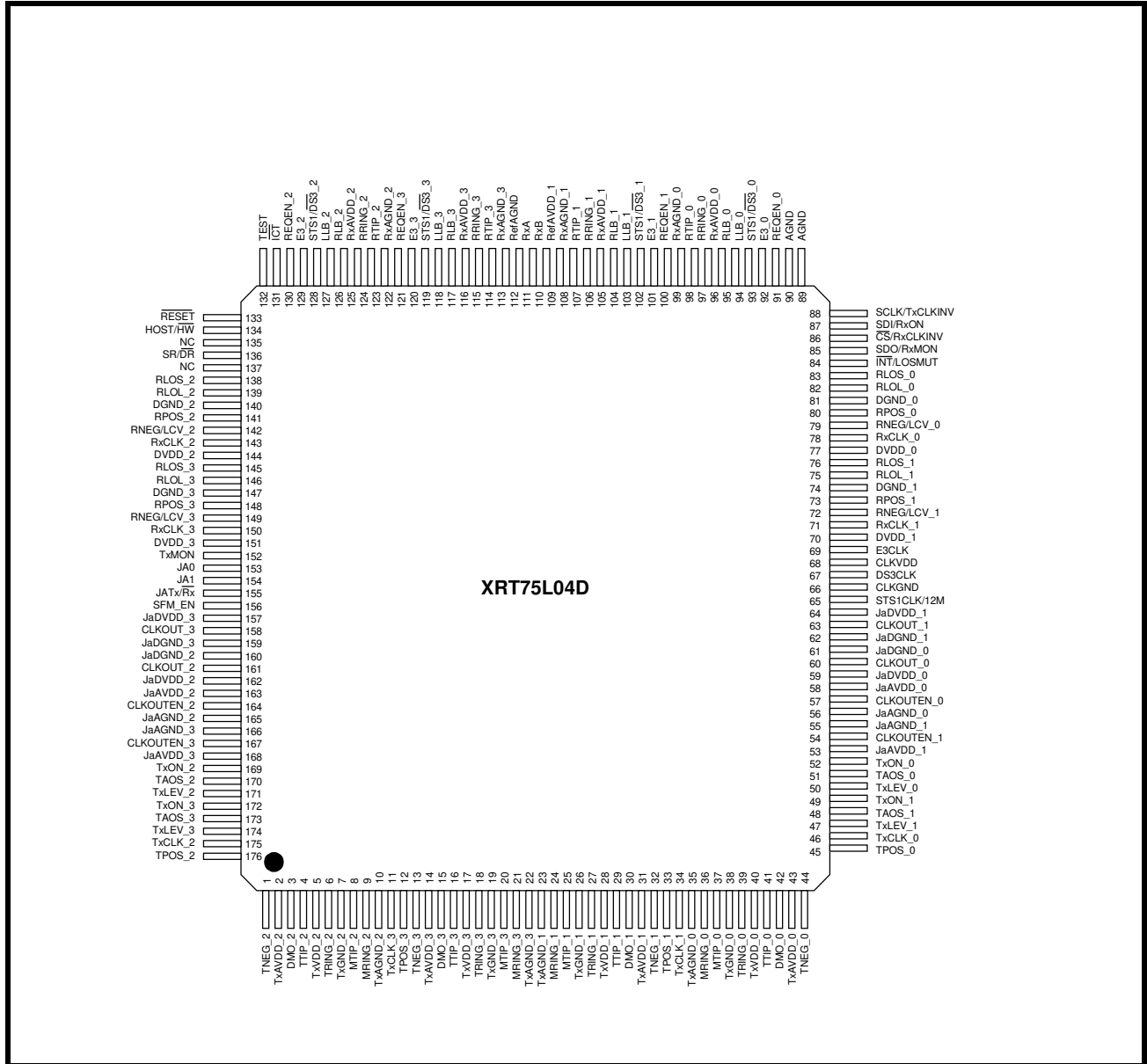
- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit.
- Built-in B3ZS/HDB3 Encoder (which can be disabled).
- Accepts Transmit Clock with duty cycle of 30%-70%.
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications.
- Generates pulses that comply with the DSX-3 pulse template, as specified in Telcordia GR-499-CORE and ANSI T1.102_1993.
- Generates pulses that comply with the STSX-1 pulse template, as specified in Telcordia GR-253-CORE.
- Transmitters can be turned off to support redundancy designs.

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery.
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications.
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications.
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms.
- Built-in B3ZS/HDB3 Decoder (which can be disabled).

- Recovered Data can be muted while the LOS Condition is declared.
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment.

FIGURE 2. PIN OUT OF THE XRT75L04D



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L04DIV	176 Pin QFP	-40°C to +85°C

TABLE OF CONTENTS

GENERAL DESCRIPTION	1
<i>FEATURES</i>	1
<i>APPLICATIONS</i>	1
<i>TRANSMIT INTERFACE CHARACTERISTICS</i>	2
<i>RECEIVE INTERFACE CHARACTERISTICS</i>	2
FIGURE 1. BLOCK DIAGRAM OF THE XRT 75L04D.....	2
FIGURE 2. PIN OUT OF THE XRT75L04D.....	3
ORDERING INFORMATION	3
PIN DESCRIPTIONS (BY FUNCTION)	4
<i>TRANSMIT INTERFACE</i>	4
<i>RECEIVE INTERFACE</i>	7
<i>CLOCK INTERFACE</i>	9
.....	10
<i>CONTROL AND ALARM INTERFACE</i>	10
<i>OPERATING MODE SELECT</i>	12
.....	13
<i>SERIAL MICROPROCESSOR INTERFACE</i>	13
.....	14
<i>JITTER ATTENUATOR INTERFACE</i>	14
<i>ANALOG POWER AND GROUND</i>	14
<i>DIGITAL POWER AND GROUND</i>	16
1.0 ELECTRICAL CHARACTERISTICS	17
TABLE 1: ABSOLUTE MAXIMUM RATINGS.....	17
TABLE 2: DC ELECTRICAL CHARACTERISTICS:.....	17
2.0 TIMING CHARACTERISTICS	18
FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75L04D (DUAL-RAIL DATA).....	18
FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING.....	18
FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING.....	19
FIGURE 6. TRANSMIT INTERFACE CIRCUIT FOR E3, DS3 AND STS-1 RATES.....	19
3.0 LINE SIDE CHARACTERISTICS:	20
3.1 E3 LINE SIDE PARAMETERS:	20
FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703.....	20
TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS.....	20
FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS.....	21
TABLE 4: STS-1 PULSE MASK EQUATIONS.....	21
TABLE 5: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253).....	22
FIGURE 9. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499.....	22
TABLE 6: DS3 PULSE MASK EQUATIONS.....	23
TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499).....	23
FIGURE 10. MICROPROCESSOR SERIAL INTERFACE STRUCTURE.....	24
FIGURE 11. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE.....	24
TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS (TA = 250C, VDD=3.3V± 5% AND LOAD = 10PF).....	25
FUNCTIONAL DESCRIPTION:	26
4.0 THE TRANSMITTER SECTION:	26
4.1 TRANSMIT CLOCK:	26
FIGURE 12. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED).....	26
FIGURE 13. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED).....	26
4.2 B3ZS/HDB3 ENCODER:	27
4.2.1 B3ZS ENCODING:	27
4.2.2 HDB3 ENCODING:	27
FIGURE 14. B3ZS ENCODING FORMAT.....	27
FIGURE 15. HDB3 ENCODING FORMAT.....	27
4.3 TRANSMIT PULSE SHAPER:	28
4.3.1 GUIDELINES FOR USING TRANSMIT BUILD OUT CIRCUIT:	28
4.3.2 INTERFACING TO THE LINE:	28
4.4 TRANSMIT DRIVE MONITOR:	28
FIGURE 16. TRANSMIT DRIVER MONITOR SET-UP.....	28
4.5 TRANSMITTER SECTION ON/OFF:	29
5.0 THE RECEIVER SECTION:	30

5.1 AGC/EQUALIZER:	30
5.1.1 INTERFERENCE TOLERANCE:	30
FIGURE 17. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1	30
5.2 CLOCK AND DATA RECOVERY:	31
5.3 B3ZS/HDB3 DECODER:	31
FIGURE 18. INTERFERENCE MARGIN TEST SET UP FOR E3	31
TABLE 9: INTERFERENCE MARGIN TEST RESULTS	31
5.4 LOS (LOSS OF SIGNAL) DETECTOR:	32
5.4.1 DS3/STS-1 LOS CONDITION:	32
DISABLING ALOS/DLOS DETECTION:	32
5.4.2 E3 LOS CONDITION:	32
TABLE 10: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF REQEN (DS3 AND STS-1 AP-PLICATIONS)	32
FIGURE 19. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775	33
FIGURE 20. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775	33
5.4.3 MUTING THE RECOVERED DATA WITH LOS CONDITION:	34
6.0 JITTER:	35
6.1 JITTER TOLERANCE - RECEIVER:	35
6.1.1 DS3/STS-1 JITTER TOLERANCE REQUIREMENTS:	35
FIGURE 21. JITTER TOLERANCE MEASUREMENTS	35
6.1.2 E3 JITTER TOLERANCE REQUIREMENTS:	36
FIGURE 22. INPUT JITTER TOLERANCE FOR DS3/STS-1	36
FIGURE 23. INPUT JITTER TOLERANCE FOR E3	36
6.2 JITTER TRANSFER - RECEIVER/TRANSMITTER:	37
6.3 JITTER GENERATION:	37
6.4 JITTER ATTENUATOR:	37
TABLE 11: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)	37
TABLE 12: JITTER TRANSFER SPECIFICATION/REFERENCES	37
TABLE 13: JITTER TRANSFER PASS MASKS	38
FIGURE 24. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE	38
7.0 SERIAL HOST INTERFACE:	39
TABLE 14: FUNCTIONS OF SHARED PINS	39
TABLE 15: REGISTER MAP AND BIT NAMES	39
TABLE 16: REGISTER MAP DESCRIPTION - GLOBAL	40
TABLE 17: REGISTER MAP AND BIT NAMES - CHANNEL 0 REGISTERS	41
TABLE 18: REGISTER MAP AND BIT NAMES - CHANNEL 1 REGISTERS	41
TABLE 19: REGISTER MAP AND BIT NAMES - CHANNEL 2 REGISTERS	42
TABLE 20: REGISTER MAP AND BIT NAMES - CHANNEL 3 REGISTERS	42
TABLE 21: REGISTER MAP DESCRIPTION	43
8.0 DIAGNOSTIC FEATURES:	47
8.1 PRBS GENERATOR AND DETECTOR:	47
8.2 LOOPBACKS:	48
8.2.1 ANALOG LOOPBACK:	48
FIGURE 25. PRBS MODE	48
8.2.2 DIGITAL LOOPBACK:	49
FIGURE 26. ANALOG LOOPBACK	49
8.2.3 REMOTE LOOPBACK:	50
FIGURE 27. DIGITAL LOOPBACK	50
FIGURE 28. REMOTE LOOPBACK	50
8.3 TRANSMIT ALL ONES (TAOS):	51
FIGURE 29. TRANSMIT ALL ONES (TAOS)	51
9.0 THE SONET/SDH DE-SYNC FUNCTION WITHIN THE LIU	52
9.1 BACKGROUND AND DETAILED INFORMATION - SONET DE-SYNC APPLICATIONS	52
FIGURE 30. A SIMPLE ILLUSTRATION OF A DS3 SIGNAL BEING MAPPED INTO AND TRANSPORTED OVER THE SONET NETWORK	53
9.2 MAPPING/DE-MAPPING JITTER/WANDER	54
9.2.1 HOW DS3 DATA IS MAPPED INTO SONET	54
9.2.1.1 A BRIEF DESCRIPTION OF AN STS-1 FRAME	54
FIGURE 31. A SIMPLE ILLUSTRATION OF THE SONET STS-1 FRAME	55
FIGURE 32. A SIMPLE ILLUSTRATION OF THE STS-1 FRAME STRUCTURE WITH THE TOH AND THE ENVELOPE CAPACITY BYTES DESIGNATED	56
FIGURE 33. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME	57
FIGURE 34. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME	58
9.2.1.2 MAPPING DS3 DATA INTO AN STS-1 SPE	59
FIGURE 35. ILLUSTRATION OF THE BYTE STRUCTURE OF THE STS-1 SPE	59

FIGURE 36. AN ILLUSTRATION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW MAP DS3 DATA INTO AN STS-1 SPE 60

FIGURE 37. A SIMPLIFIED "BIT-ORIENTED" VERSION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW TO MAP DS3 DATA INTO AN STS-1 SPE 60

9.2.2 DS3 FREQUENCY OFFSETS AND THE USE OF THE "STUFF OPPORTUNITY" BITS 61

9.2.2.1 THE IDEAL CASE FOR MAPPING DS3 DATA INTO AN STS-1 SIGNAL (E.G., WITH NO FREQUENCY OFFSETS) 62

FIGURE 38. A SIMPLE ILLUSTRATION OF A DS3 DATA-STREAM BEING MAPPED INTO AN STS-1 SPE, VIA A PTE 62

9.2.2.2 THE 44.736MBPS + 1PPM CASE 63

FIGURE 39. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE "SOURCE" PTE, WHEN MAPPING IN A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS + 1PPM, INTO AN STS-1 SIGNAL 63

9.2.2.3 THE 44.736MBPS - 1PPM CASE 64

9.3 JITTER/WANDER DUE TO POINTER ADJUSTMENTS 65

9.3.1 THE CONCEPT OF AN STS-1 SPE POINTER..... 65

FIGURE 40. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE SOURCE PTE, WHEN MAPPING A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS - 1PPM, INTO AN STS-1 SIGNAL 65

FIGURE 41. AN ILLUSTRATION OF AN STS-1 SPE STRADDLING ACROSS TWO CONSECUTIVE STS-1 FRAMES 66

9.3.2 POINTER ADJUSTMENTS WITHIN THE SONET NETWORK 67

FIGURE 42. THE BIT-FORMAT OF THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE 10 BITS, REFLECTING THE LOCATION OF THE J1 BYTE, DESIGNATED 67

FIGURE 43. THE RELATIONSHIP BETWEEN THE CONTENTS OF THE "POINTER BITS" (E.G., THE 10-BIT EXPRESSION WITHIN THE H1 AND H2 BYTES) AND THE LOCATION OF THE J1 BYTE WITHIN THE ENVELOPE CAPACITY OF AN STS-1 FRAME 67

9.3.3 CAUSES OF POINTER ADJUSTMENTS 68

FIGURE 44. AN ILLUSTRATION OF AN STS-1 SIGNAL BEING PROCESSED VIA A SLIP BUFFER..... 69

FIGURE 45. AN ILLUSTRATION OF THE BIT FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "I" BITS DESIGNATED 70

FIGURE 46. AN ILLUSTRATION OF THE BIT-FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "D" BITS DESIGNATED 71

9.3.4 WHY ARE WE TALKING ABOUT POINTER ADJUSTMENTS? 72

9.4 CLOCK GAPPING JITTER 72

FIGURE 47. ILLUSTRATION OF THE TYPICAL APPLICATIONS FOR THE LIU IN A SONET DE-SYNC APPLICATION 72

9.5 A REVIEW OF THE CATEGORY I INTRINSIC JITTER REQUIREMENTS (PER TELCORDIA GR-253-CORE) FOR DS3 APPLICATIONS 73

TABLE 22: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS 73

9.5.1 DS3 DE-MAPPING JITTER..... 74

9.5.2 SINGLE POINTER ADJUSTMENT 74

9.5.3 POINTER BURST..... 74

FIGURE 48. ILLUSTRATION OF SINGLE POINTER ADJUSTMENT SCENARIO 74

9.5.4 PHASE TRANSIENTS..... 75

FIGURE 49. ILLUSTRATION OF BURST OF POINTER ADJUSTMENT SCENARIO 75

FIGURE 50. ILLUSTRATION OF "PHASE-TRANSIENT" POINTER ADJUSTMENT SCENARIO 75

9.5.5 87-3 PATTERN..... 76

9.5.6 87-3 ADD 76

FIGURE 51. AN ILLUSTRATION OF THE 87-3 CONTINUOUS POINTER ADJUSTMENT PATTERN 76

9.5.7 87-3 CANCEL..... 77

FIGURE 52. ILLUSTRATION OF THE 87-3 ADD POINTER ADJUSTMENT PATTERN 77

FIGURE 53. ILLUSTRATION OF 87-3 CANCEL POINTER ADJUSTMENT SCENARIO 77

9.5.8 CONTINUOUS PATTERN..... 78

9.5.9 CONTINUOUS ADD 78

FIGURE 54. ILLUSTRATION OF CONTINUOUS PERIODIC POINTER ADJUSTMENT SCENARIO 78

9.5.10 CONTINUOUS CANCEL..... 79

FIGURE 55. ILLUSTRATION OF CONTINUOUS-ADD POINTER ADJUSTMENT SCENARIO 79

FIGURE 56. ILLUSTRATION OF CONTINUOUS-CANCEL POINTER ADJUSTMENT SCENARIO 79

9.6 A REVIEW OF THE DS3 WANDER REQUIREMENTS PER ANSI T1.105.03B-1997. 80

9.7 A REVIEW OF THE INTRINSIC JITTER AND WANDER CAPABILITIES OF THE LIU IN A TYPICAL SYSTEM APPLICATION 80

9.7.1 INTRINSIC JITTER TEST RESULTS..... 80

TABLE 23: SUMMARY OF "CATEGORY I INTRINSIC JITTER TEST RESULTS" FOR SONET/DS3 APPLICATIONS 80

9.7.2 WANDER MEASUREMENT TEST RESULTS..... 81

9.8 DESIGNING WITH THE LIU 81

9.8.1 HOW TO DESIGN AND CONFIGURE THE LIU TO PERMIT A SYSTEM TO MEET THE ABOVE-MENTIONED INTRINSIC JITTER AND WANDER REQUIREMENTS..... 81

FIGURE 57. ILLUSTRATION OF THE LIU BEING CONNECTED TO A MAPPER IC FOR SONET DE-SYNC APPLICATIONS 81

 CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0x06 82

 CHANNEL 1 ADDRESS LOCATION = 0x0E 82

 CHANNEL 2 ADDRESS LOCATION = 0x16 82

 CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0x06 83

CHANNEL 1 ADDRESS LOCATION = 0x0E	83
CHANNEL 2 ADDRESS LOCATION = 0x16.....	83
JITTER ATTENUATOR CONTROL REGISTER - (CHANNEL 0 ADDRESS LOCATION = 0x07	83
CHANNEL 1 ADDRESS LOCATION = 0x0F	83
CHANNEL 2 ADDRESS LOCATION = 0x17.....	83
9.8.2 RECOMMENDATIONS ON PRE-PROCESSING THE GAPPED CLOCKS (FROM THE MAPPER/ASIC DEVICE) PRIOR TO ROUTING THIS DS3 CLOCK AND DATA-SIGNALS TO THE TRANSMIT INPUTS OF THE LIU	84
9.8.2.1 SOME NOTES PRIOR TO STARTING THIS DISCUSSION:	84
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0x07.....	84
CHANNEL 1 ADDRESS LOCATION = 0x0F	84
CHANNEL 2 ADDRESS LOCATION = 0x17.....	84
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0x07.....	84
CHANNEL 1 ADDRESS LOCATION = 0x0F	84
CHANNEL 2 ADDRESS LOCATION = 0x17.....	84
9.8.2.2 OUR PRE-PROCESSING RECOMMENDATIONS	85
FIGURE 58. ILLUSTRATION OF MINOR PATTERN P1	85
FIGURE 59. ILLUSTRATION OF MINOR PATTERN P2.....	86
FIGURE 60. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE MAJOR PATTERN A	86
FIGURE 61. ILLUSTRATION OF MINOR PATTERN P3.....	87
FIGURE 62. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE PATTERN B.....	87
9.8.3 HOW DOES THE LIU PERMIT THE USER TO COMPLY WITH THE SONET APS RECOVERY TIME REQUIREMENTS OF 50MS (PER TELCORDIA GR-253-CORE)?	88
FIGURE 63. ILLUSTRATION OF THE SUPER PATTERN WHICH IS OUTPUT VIA THE "OC-N TO DS3" MAPPER IC	88
FIGURE 64. SIMPLE ILLUSTRATION OF THE LIU BEING USED IN A SONET DE-SYNCHRONIZER" APPLICATION.....	88
TABLE 24: MEASURED APS RECOVERY TIME AS A FUNCTION OF DS3 PPM OFFSET	89
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0x07.....	89
CHANNEL 1 ADDRESS LOCATION = 0x0F	89
CHANNEL 2 ADDRESS LOCATION = 0x17.....	89
9.8.4 HOW SHOULD ONE CONFIGURE THE LIU, IF ONE NEEDS TO SUPPORT "DAISY-CHAIN" TESTING AT THE END CUSTOMER'S SITE?	90
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0x07.....	90
CHANNEL 1 ADDRESS LOCATION = 0x0F	90
CHANNEL 2 ADDRESS LOCATION = 0x17.....	90
APPENDIX B	91
TABLE 25: TRANSFORMER RECOMMENDATIONS.....	91
TABLE 26: TRANSFORMER DETAILS.....	91
ORDERING INFORMATION	93
PACKAGE DIMENSIONS - 176 PIN PACKAGE	93
REVISIONS	94

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION																												
52 49 169 172	TxON_0 TxON_1 TxON_2 TxON_3	I	<p>Transmitter ON Input - Channel 0: Transmitter ON Input - Channel 1: Transmitter ON Input - Channel 2: Transmitter ON Input - Channel 3:</p> <p>These pins are active only when the corresponding TxON bit is set. Table below shows the status of the transmitter based on the TxON bit and TxON pin settings.</p> <table border="1"> <thead> <tr> <th>Host/HW</th> <th>Bit</th> <th>Pin</th> <th>Transmitter Status</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>ON</td> </tr> <tr> <td>0</td> <td>x</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>0</td> <td>x</td> <td>1</td> <td>ON</td> </tr> </tbody> </table> <p>NOTES:</p> <ol style="list-style-type: none"> 1. These pins will be active and can control the TTIP and TRING outputs only when the TxON_n bits in the channel register are set . 2. When Transmitters are turned off the TTIP and TRING outputs are Tri-stated. 3. These pins are internally pulled up. 	Host/HW	Bit	Pin	Transmitter Status	1	0	0	OFF	1	0	1	OFF	1	1	0	OFF	1	1	1	ON	0	x	0	OFF	0	x	1	ON
Host/HW	Bit	Pin	Transmitter Status																												
1	0	0	OFF																												
1	0	1	OFF																												
1	1	0	OFF																												
1	1	1	ON																												
0	x	0	OFF																												
0	x	1	ON																												
46 34 175 11	TxCLK_0 TxCLK_1 TxCLK_2 TxCLK_3	I	<p>Transmit Clock Input for TPOS and TNEG - Channel 0: Transmit Clock Input for TPOS and TNEG - Channel 1: Transmit Clock Input for TPOS and TNEG - Channel 2: Transmit Clock Input for TPOS and TNEG - Channel 3:</p> <p>The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%. By default, input data is sampled on the falling edge of TxCLK when input data is changing on the rising edge of TxCLK..</p>																												
44 32 1 13	TNEG_0 TNEG_1 TNEG_2 TNEG_3	I	<p>Transmit Negative Data Input - Channel 0: Transmit Negative Data Input - Channel 1: Transmit Negative Data Input - Channel 2: Transmit Negative Data Input - Channel 3:</p> <p>In Dual-rail mode, these pins are sampled on the falling or rising edge of TxCLK_n .</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. These input pins are ignored and must be grounded if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment. 																												

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
45 33 176 12	TPOS_0 TPOS_1 TPOS_2 TPOS_3	I	<p>Transmit Positive Data Input - Channel 0: Transmit Positive Data Input - Channel 1: Transmit Positive Data Input - Channel 2: Transmit Positive Data Input - Channel 3:</p> <p>By default sampled on the falling edge of TxCLK</p>
41 29 4 16	TTIP_0 TTIP_1 TTIP_2 TTIP_3	O	<p>Transmit TTIP Output - Channel 0: Transmit TTIP Output - Channel 1: Transmit TTIP Output - Channel 2: Transmit TTIP Output - Channel 3:</p> <p>These pins along with TRING transmit bipolar signals to the line using a 1:1 transformer.</p>
39 27 6 18	TRING_0 TRING_1 TRING_2 TRING_3	O	<p>Transmit Ring Output - Channel 0: Transmit Ring Output - Channel 1: Transmit Ring Output - Channel 2: Transmit Ring Output - Channel 3:</p> <p>These pins along with TTIP transmit bipolar signals to the line using a 1:1 transformer.</p>
50 47 171 174	TxLEV_0 TxLEV_1 TxLEV_2 TxLEV_3	I	<p>Transmit Line Build-Out Enable/Disable Select - Channel 0: Transmit Line Build-Out Enable/Disable Select - Channel 1: Transmit Line Build-Out Enable/Disable Select - Channel 2: Transmit Line Build-Out Enable/Disable Select - Channel 3:</p> <p>These input pins are used to select the Transmit Line Build-Out circuit of Channel n.</p> <p>Setting these pins to "High" disables the Line Build-Out circuit of Channel n. In this mode, Channel n outputs partially-shaped pulses onto the line via the TTIP_n and TRing_n output pins.</p> <p>Setting these pins to "Low" enables the Line Build-Out circuit of Channel n. In this mode, Channel n outputs shaped pulses onto the line via the TTIP_n and TRing_n output pins.</p> <p>To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE:</p> <ol style="list-style-type: none"> Set these pins to "1" if the cable length between the Cross-Connect and the transmit output of Channel is greater than 225 feet. Set these pins to "0" if the cable length between the Cross-Connect and the transmit output of Channel is less than 225 feet. <p>These pins are active only if the following two conditions are true:</p> <ol style="list-style-type: none"> The XRT75L04D is configured to operate in either the DS3 or SONET STS-1 Modes. The XRT75L04D is configured to operate in the Hardware Mode. <p>NOTES:</p> <ol style="list-style-type: none"> These pins are internally pulled down. If the XRT75L04D is configured in HOST mode, these pins should be tied to GND.

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
88	TxCiKINV/ SCiK	I	<p>Hardware Mode: Transmit Clock Invert</p> <p>Host Mode: Serial Clock Input:</p> <p>Function of this pin depends on whether the XRT75L04D is configured to operate in Hardware mode or Host mode.</p> <p>In Hardware mode, setting this input pin "High" configures all three Transmitters to sample the TPOS_n and TNEG_n data on the rising edge of the TxCLK_n .</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. If the XRT75L04D is configured in HOST mode, this pin functions as SCiK input pin (please refer to the pin description for Microprocessor interface).
152	TxMON	I	<p>Transmitter Monitor:</p> <p>When this pin is pulled "High", MTIP and MRING are connected internally to TTIP and TRING and allows self monitoring of the transmitter.</p>
51 48 170 173	TAOS_0 TAOS_1 TAOS_2 TAOS_3	I	<p>Transmit All Ones Select - Channel 0:</p> <p>Transmit All Ones Select - Channel 1:</p> <p>Transmit All Ones Select - Channel 2:</p> <p>Transmit All Ones Select - Channel 3:</p> <p>A "High" on this pin causes the Transmitter Section of Channel_n to generate and transmit a continuous AMI all "1's" pattern onto the line. The frequency of this "1's" pattern is determined by TxClk_n.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. This input pin is ignored if the XRT75L04D is operating in the HOST Mode and should be tied to GND. 2. Analog Loopback and Remote Loopback have priority over request. 3. This pin is internally pulled down.

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
78 71 143 150	RxCLK_0 RXCLK_1 RxCLK_2 RxCLK_3	O	Receive Clock Output - Channel 0: Receive Clock Output - Channel 1: Receive Clock Output - Channel 2: Receive Clock Output - Channel 3: By default, RPOS and RNEG data sampled on the rising edge RxCLK.. Set the RxCLKINV bit to sample RPOS/RNEG data on the falling edge of RxCLK
80 73 141 148	RPOS_0 RPOS_1 RPOS_2 RPOS_3	O	Receive Positive Data Output - Channel 0: Receive Positive Data Output - Channel 1: Receive Positive Data Output - Channel 2: Receive Positive Data Output - Channel 3: <i>NOTE: If the B3ZS/HDB3 Decoder is enabled in Single-rail mode, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is removed and replaced with '0'.</i>
79 72 142 149	RNEG_0/LCV_0 RNEG_1/LCV_1 RNEG_2/LCV_2 RNEG_3/LCV_3	O	Receive Negative Data Output/Line Code Violation Indicator - Channel 0: Receive Negative Data Output/Line Code Violation Indicator - Channel 1: Receive Negative Data Output/Line Code Violation Indicator - Channel 2: Receive Negative Data Output/Line Code Violation Indicator - Channel 3: In Dual Rail mode, a negative pulse is output through RNEG. Line Code Violation Indicator - Channel n: If configured in Single Rail mode then Line Code Violation will be output.
97 106 124 115	RRING_0 RRING_1 RRING_2 RRING_3	I	Receive Ring Input - Channel 0: Receive Ring Input - Channel 1: Receive Ring Input - Channel 2: Receive Ring Input - Channel 3: These pins along with RTIP receive the bipolar line signal from the remote DS3/E3/STS-1 Terminal.
98 107 123 114	RTIP_0 RTIP_1 RTIP_2 RTIP_3	I	Receive TIP Input - Channel 0: Receive TIP Input - Channel 1: Receive TIP Input - Channel 2: Receive TIP Input - Channel 3: These pins along with RRING receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
91 100 130 121	REQEN_0 REQEN_1 REQEN_2 REQEN_3	I	<p>Receive Equalizer On/Off - Channel 0: Receive Equalizer On/Off- Channel 1: Receive Equalizer On/Off - Channel 2: Receive Equalier On/Off- Channel 3:</p> <p>Tie these pins "High" to enable the receive equalizer.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. This input pin is ignored and should be connected to GND if the XRT75L04D is operating in the HOST Mode 2. This pin is internally pulled down.
87	RxON/ SDI	I	<p>Hardware Mode: Receiver Turn ON Input Host Mode: Serial Data Input:</p> <p>Function of this pin depends on whether the XRT75L04D is configured to operate in Hardware mode or Host mode.</p> <p>In Hardware mode, setting this input pin "High" turns on and enables the Receivers of all three channels.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. If the XRT75L04D is configured in HOST mode, this pin functions as SDI input pin (please refer to the pin description for Microprocessor Interface) 2. This pin is internally pulled down.
86	RxCiKINV/ \overline{CS}	I	<p>Hardware Mode: RxClk INVERT Host Mode: Chip Select:</p> <p>Function of this pin depends on whether the XRT75L04D is configured to operate in Hardware mode or Host mode.</p> <p>In Hardware mode, setting this input pin "High" configures the Receiver Section of all channels to invert the RxClk_n output signals and outputs the recovered data via RPOS_n and RNEG_n on the falling edge of RxClk_n.</p> <p>NOTE: If the XRT75L04D is configured in HOST mode, this pin functions as CS input pin (please refer to the pin description for Microprocessor Interface).</p>
85	RxMON/ SDO	I	<p>Hardware Mode: Receive Monitoring Mode Host Mode: Serial Data Output:</p> <p>In Hardware mode, when this pin is tied "High" all 4 channels configure into monitoring channels. In the monitoring mode, the Receiver is capable of monitoring the signals with 20 dB flat loss plus 6 dB cable attenuation. This allows monitoring very weak signal before declaring LOS.</p> <p>In HOST Mode each channel can be independently configured to be a monitoring channel by setting the bits in the channel control registers.</p> <p>NOTE: If the XRT75L04D is configured in HOST mode, this pin functions as SDO pin (please refer to the pin description for the Microprocessor Interface).</p>

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	E3CLK	I	<p>E3 Clock Input (34.368 MHz ± 20 ppm): If any of the channels is configured in E3 mode, a reference clock 34.368 MHz is applied on this pin. <i>NOTE: In single frequency mode, this reference clock is not required.</i></p>
67	DS3CLK	I	<p>DS3 Clock Input (44.736 MHz ± 20 ppm): If any of the channels is configured in DS3 mode, a reference clock 44.736 MHz. is applied on this pin. <i>NOTE: In single frequency mode, this reference clock is not required.</i></p>
65	STS-1CLK/ 12M	I	<p>STS-1 Clock Input (51.84 MHz ± 20 ppm): If any of the channels is configured in STS-1 mode, a reference clock 51.84 MHz is applied on this pin.. In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the channels in E3, DS3 or STS-1.</p>
156	SFM_EN	I	<p>Single Frequency Mode Enable: Tie this pin "High" to enable the Single Frequency Mode. A reference clock of 12.288 MHz ± 20 ppm is applied. This offers the flexibility of using a low cost reference clock and configures the board for either E3 or DS3 or STS-1 without the need to change any components on the board. In the Single Frequency Mode (SFM) an output clock is provided for each channel if the CLK_EN bit is set thus eliminating the need for a separate clock source for the framer. Tie this pin "Low" if single frequency mode is not selected. In this case, the appropriate reference clocks must be provided. <i>NOTE: This pin is internally pulled down</i></p>
57 54 164 167	CLKOUTEN_0 CLKOUTEN_1 CLKOUTEN_2 CLKOUTEN_3	O	<p>Clock output enable for channel 0 Clock output enable for channel 1 Clock output enable for channel 2 Clock output enable for channel 3 Pull this pin "High" to output low jitter clock on the CLKOUT_n pins. NOTES: 1. This clock output is only available in SFM mode. 2. The maximum drive capability for the clockouts is 16 mA.</p>
60 63 161 158	CLKOUT_0 CLKOUT_1 CLKOUT_2 CLKOUT_3	O	<p>Clock output for channel 0 Clock output for channel 1 Clock output for channel 2 Clock output for channel 3 If CLKOUTEN_n pin is "High", low jitter clock is output for each channel. Frequency of these clocks is based on the mode (E3,DS3 or STS-1) the channels are configured. This eliminates the need for a separate clock source for the framer. NOTES: 1. This clock output is only available in SFM mode. 2. The maximum drive capability for the clockouts is 16 mA.</p>

CONTROL AND ALARM INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
36 24 9 21	MRING_0 MRING_1 MRING_2 MRING_3	I	<p>Monitor Ring Input - Channel 0: Monitor Ring Input - Channel 1: Monitor Ring Input - Channel 2: Monitor Ring Input - Channel 3:</p> <p>The bipolar line output signal from TRING_n is connected to this pin via a 270 Ω resistor to check for line driver failure. NOTE: This pin is internally pulled "Low".</p>
37 25 8 20	MTIP_0 MTIP_1 MTIP_2 MTIP_3	I	<p>Monitor Tip Input - Channel 0: Monitor Tip Input - Channel 1: Monitor Tip Input - Channel 2: Monitor Tip Input - Channel 3:</p> <p>The bipolar line output signal from TTIP_n is connected to this pin via a 270-ohm resistor to check for line driver failure. NOTE: This pin is internally pulled "Low".</p>
42 30 3 15	DMO_0 DMO_1 DMO_2 DMO_3	O	<p>Drive Monitor Output - Channel 0: Drive Monitor Output - Channel 1: Drive Monitor Output - Channel 2: Drive Monitor Output - Channel 3:</p> <p>If MTIP_n and MRING_n has no transition pulse for 128 ± 32 TxCLK_n cycles, DMO_n goes "High" to indicate the driver failure. DMO_n output stays "High" until the next AMI signal is detected.</p>
83 76 138 145	RLOS_0 RLOS_1 RLOS_2 RLOS_3	O	<p>Receive Loss of Signal Output Indicator - Channel 0: Receive Loss of Signal Output Indicator - Channel 1: Receive Loss of Signal Output Indicator - Channel 2: Receive Loss of Signal Output Indicator - Channel 3:</p> <p>This output pin toggles "High" if the receiver has detected a Loss of Signal Condition. The criteria for declaring /clearing an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode.</p>
82 75 139 146	RLOL_0 RLOL_1 RLOL_2 RLOL_3	O	<p>Receive Loss of Lock Output Indicator - Channel 0: Receive Loss of Lock Output Indicator - Channel 1: Receive Loss of Lock Output Indicator - Channel 2: Receive Loss of Lock Output Indicator - Channel 3:</p> <p>This output pin toggles "High" if a Loss of Lock Condition is detected. LOL (Loss of Lock) condition occurs if the recovered clock frequency deviates from the Reference Clock frequency (available at either E3CLK or DS3CLK or STS-1CLK input pins) by more than 0.5%.</p>
111	RXA	****	<p>External Resistor of 3 K Ω ± 1%. Should be connected between RxA and RxB for internal bias.</p>
110	RXB	****	<p>External Resistor of 3K Ω ±1%. Should be connected between RxA and RxB for internal bias.</p>

CONTROL AND ALARM INTERFACE

131	\overline{ICT}	I	<p>In-Circuit Test Input: Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, tie this pin "High". <i>NOTE: This pin is internally pulled "High".</i></p>
132	TEST	****	<p>Factory Test Pin <i>NOTE: This pin must be connected to GND for normal operation.</i></p>
84	LOSMUT/ \overline{INT}	I/O	<p>Hardware Mode: MUTE-upon-LOS Enable Input Host Mode: Interrupt Output: In Hardware Mode, setting pin "High" configures all three channels to Mute the recovered data on the RPOS_n and RNEG_n whenever one of the channels declares an LOS condition. RPOS_n and RNEG_n outputs are pulled "Low". Muting of the output data can be configured/controlled on a per channel basis in Host Mode. <i>NOTE: If the XRT75L04D is configured in HOST mode, this pin functions as \overline{INT} pin (please refer to the pin description for the Microprocessor Interface).</i></p>

CONTROL AND ALARM INTERFACE

94 103 127 118	LLB_0 LLB_1 LLB_2 LLB_3	I	<p>Local Loop-back - Channel 0:</p> <p>Local Loop-back - Channel 1:</p> <p>Local Loop-back - Channel 2:</p> <p>Local Loop-back - Channel 3:</p> <p>This input pin along with RLB_n configures different Loop-Back modes. A "High" on this pin with RLB_n set to "Low" configures Channel_n to operate in the Analog Local Loop-back Mode. A "High" on this pin with RLB_n set to "High" configures Channel_n to operate in the Digital Local Loop-back Mode.</p> <p>NOTE: This input pin is ignored and should be connected to GND if the XRT75L04D is operating in the HOST Mode.</p>															
95 104 126 117	RLB_0 RLB_1 RLB_2 RLB_3	I	<p>Remote Loop-back - Channel 0:</p> <p>Remote Loop-back - Channel 1:</p> <p>Remote Loop-back - Channel 2:</p> <p>Remote Loop-back - Channel 3:</p> <p>This input pin along with LLB_n configures different Loop-Back modes. A "High" on this pin with LLB_n set to "Low" configures Channel_n to operate in the Remote Loop-back Mode. A "High" on this pin with LLB_n set to "High" configures Channel_n to operate in the Digital Local Loop-back Mode.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RLB_n</th> <th>LLB_n</th> <th>Loopback Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Normal Operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>Analog Local</td> </tr> <tr> <td>1</td> <td>0</td> <td>Remote</td> </tr> <tr> <td>1</td> <td>1</td> <td>Digital</td> </tr> </tbody> </table> <p>NOTE: This input pin is ignored and should be connected to GND if the XRT75L04D is operating in the HOST Mode.</p>	RLB_n	LLB_n	Loopback Mode	0	0	Normal Operation	0	1	Analog Local	1	0	Remote	1	1	Digital
RLB_n	LLB_n	Loopback Mode																
0	0	Normal Operation																
0	1	Analog Local																
1	0	Remote																
1	1	Digital																

OPERATING MODE SELECT

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
134	HOST/(HW)	I	<p>HOST/Hardware Mode Select:</p> <p>Tie this pin "High" to configure in HOST mode. Tie this "Low" to configure in Hardware mode.</p> <p>When configured in HOST mode, the states of many of the discrete input pins are controlled by internal register bits.</p> <p>NOTE: This pin is internally pulled up.</p>

OPERATING MODE SELECT

92	E3_0	I	E3 Mode Select Input A "High" on this pin configures Channel_n to operate in E3 mode. A "Low" on this pin configures Channel_n to operate in either STS-1 or DS3 mode depending on the settings on pins 93,102,128 and 119 pins. NOTES: <ol style="list-style-type: none"> This pin is internally pulled down This pin is ignored and should be tied to GND if configured to operate in HOST mode.
101	E3_1		
129	E3_2		
120	E3_3		
93	STS-1/ $\overline{\text{DS3}}_0$	I	STS-1/DS3 Select Input A "High" on these pins configures the Channel_n to operate in STS-1 mode. A "Low" on these pins configures the Channel_n to operate in DS3 mode. These pins are ignored if the E3_n pins are set to "High". NOTES: <ol style="list-style-type: none"> This pin is internally pulled down This pin is ignored and should be tied to GND if configured to operate in HOST mode.
102	STS-1/ $\overline{\text{DS3}}_1$		
128	STS-1/ $\overline{\text{DS3}}_2$		
119	STS-1/ $\overline{\text{DS3}}_3$		
136	SR/ $\overline{\text{DR}}$	I	Single-Rail/Dual-Rail Select: Setting this "High" configures both the Transmitter and Receiver to operate in Single-rail mode and also enables the B3ZS/HDB3 Encoder and Decoder. In Single-rail mode, TNEG_n pin should be grounded. Setting this "Low" configures both the Transmitter and Receiver to operate in Dual-rail mode and disables the B3ZS/HDB3 Encoder and Decoder. NOTE: This pin is internally pulled down.

SERIAL MICROPROCESSOR INTERFACE

86	$\overline{\text{CS}}$ RxCLKINV	I	Microprocessor Serial Interface - Chip Select Toggle this pin "Low" to enable the communication with the Microprocessor Serial Interface.(see figures 10 & 11) NOTE: If configured in Hardware Mode, this pin functions as RxClkINV.
88	SClk TxCLKINV	I	Serial Interface Clock Input The data on the SDI pin is sampled on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. NOTE: If configured in Hardware Mode, this pin functions as TxClkINV.
87	SDI RxON	I	Serial Data Input: Data is serially input through this pin. The input data is sampled on the rising edge of the SClk pin (pin 88). NOTES: <ol style="list-style-type: none"> This pin is internally pulled down If configured in Hardware Mode, this pin functions as RxON.
85	SDO RxMON	I/O	Serial Data Output: This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SClk and this pin is tri-stated upon completion of data transfer. NOTE: If configured in Hardware Mode, this pin functions as RxMON.

SERIAL MICROPROCESSOR INTERFACE

84	$\overline{\text{INT}}$ LOSMUT	I/O	<p>INTERRUPT Output: This pin functions as Interrupt Output for Serial Interface. A transition to “Low” indicates that an interrupt has been generated by the Serial Interface. The interrupt function can be disabled by setting the interrupt enable bit to “0” in the Channel Control Register.</p> <p>NOTES:</p> <ol style="list-style-type: none"> In Hardware mode, this pin functions as LOSMUT. This pin will remain asserted “Low” until the interrupt is serviced.
133	$\overline{\text{RESET}}$	I	<p>Register Reset: Setting this input pin “Low” causes the XRT75L04D to reset the contents of the Command Registers to their default settings and default operating configuration</p> <p>NOTE: This pin is internally pulled up.</p>

JITTER ATTENUATOR INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION															
154	JA1	I	<p>Jitter Attenuator Select 1: In Hardware Mode, this pin along with the pin JA0 configures the Jitter Attenuator as shown in the table.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>JA0</th> <th>JA1</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>16 bit FIFO</td> </tr> <tr> <td>0</td> <td>1</td> <td>32 bit FIFO</td> </tr> <tr> <td>1</td> <td>0</td> <td>128 bit FIFO</td> </tr> <tr> <td>1</td> <td>1</td> <td>Disable Jitter Attenuator</td> </tr> </tbody> </table> <p>NOTE: This pin is internally pulled down.</p>	JA0	JA1	Mode	0	0	16 bit FIFO	0	1	32 bit FIFO	1	0	128 bit FIFO	1	1	Disable Jitter Attenuator
JA0	JA1	Mode																
0	0	16 bit FIFO																
0	1	32 bit FIFO																
1	0	128 bit FIFO																
1	1	Disable Jitter Attenuator																
155	JATx/ $\overline{\text{Rx}}$	I	<p>Jitter Attenuator Path Select In Hardware Mode, tie this pin “High” to select the Jitter Attenuator in the Transmit Path . Connect this pin “Low” to select the Jitter Attenuator in the Receive Path. This applies to all4 channels.</p> <p>NOTE: This pin is internally pulled down.</p>															
153	JA0	I	<p>Jitter Attenuator Select 0: In Hardware Mode, this pin along with pin 154 configures the Jitter Attenuator as shown in the above table f.</p> <p>NOTE: This pin is internally pulled down.</p>															

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
43	TxAVDD_0	****	Transmitter Analog 3.3 V ± 5% VDD - Channel 0
31	TxAVDD_1	****	Transmitter Analog 3.3 V ± 5% VDD - Channel 1

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
2	TxAVDD_2	****	Transmitter Analog 3.3 V \pm 5% VDD - Channel 2
14	TxAVDD_3	****	Transmitter Analog 3.3 V \pm 5% VDD - Channel 3
35	TxAGND_0	****	Transmitter Analog GND - Channel 0
23	TxAGND_1	****	Transmitter Analog GND - Channel 1
10	TxAGND_2	****	Transmitter Analog GND - Channel 2
22	TxAGND_3	****	Transmitter Analog GND - Channel 3
96	RxAVDD_0	****	Receiver Analog 3.3 V \pm 5% VDD - Channel 0
105	RxAVDD_1	****	Receiver Analog 3.3 V \pm 5% VDD - Channel 1
125	RxAVDD_2	****	Receiver Analog 3.3 V \pm 5% VDD - Channel 2
116	RxAVDD_3	****	Receiver Analog 3.3 V \pm 5% VDD - Channel 3
99	RxAGND_0	****	Receiver Analog GND - Channel_0
108	RxAGND_1	****	Receive Analog GND - Channel 1
122	RxAGND_2	****	Receive Analog GND - Channel 2
113	RxAGND_3	****	Receive Analog GND - Channel 3
58	JaAVDD_0	****	Analog 3.3 V \pm 5% VDD - Channel 0
53	JaAVDD_1	****	Analog 3.3 V \pm 5% VDD - Channel 1
163	JaAVDD_2	****	Analog 3.3 V \pm 5% VDD - Channel 2
168	JaAVDD_3	****	Analog 3.3 V \pm 5% VDD - Channel 3
56	JaAGND_0	****	Analog GND - Channel 0
55	JaAGND_1	****	Analog GND - Channel 1
165	JaAGND_2	****	Analog GND - Channel 2
166	JaAGND_3	****	Analog GND - Channel 3
89	AGND	****	Analog GND
90	AGND	****	Analog GND
109	REFAVDD	****	Analog 3.3 V \pm 5% VDD - Reference
112	REFAGND	****	Reference GND

DIGITAL POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
40	TxVDD_0	****	Transmitter 3.3 V \pm 5% VDD Channel 0
28	TxVDD_1	****	Transmitter 3.3 V \pm 5% VDD Channel 1
5	TxVDD_2	****	Transmitter 3.3 V \pm 5% VDD Channel 2
17	TxVDD_3	****	Transmitter 3.3 V \pm 5% VDD Channel 3
38	TxGND_0	****	Transmitter GND - Channel 0
26	TxGND_1	****	Transmitter GND - Channel 1
7	TxGND_2	****	Transmitter GND - Channel 2
19	TxGND_3	****	Transmitter GND - Channel 3
77	DVDD_0	****	Receiver 3.3 V \pm 5% VDD - Channel 0
70	DVDD_1	****	Receiver 3.3 V \pm 5% VDD - Channel 1
144	DVDD_2	****	Receiver 3.3 V \pm 5% VDD - Channel 2
151	DVDD_3	****	Receiver 3.3 V \pm 5% VDD - Channel 3
81	DGND_0	****	Receiver Digital GND - Channel 0
74	DGND_1	****	Receiver Digital GND - Channel 1
140	DGND_2	****	Receiver Digital GND - Channel 2
147	DGND_3	****	Receiver Digital GND - Channel 3
59	JaDVDD_0	****	VDD 3.3 V \pm 5%
64	JaDVDD_1	****	VDD 3.3 V \pm 5%
162	JaDVDD_2	****	VDD 3.3 V \pm 5%
157	JaDVDD_3	****	VDD 3.3 V \pm 5%
61	JaDGND_0	****	GND
62	JaDGND_1	****	Digital GND
160	JaDGND_2	****	Digital GND
159	JaDGND_3	****	Digital GND
68	CLKVDD	****	VDD 3.3 V \pm 5%
66	CLKGND	****	Digital GND

1.0 ELECTRICAL CHARACTERISTICS
TABLE 1: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V _{DD}	Supply Voltage	-0.5	5.0	V	Note 1
V _{IN}	Input Voltage at any Pin	-0.5	5+0.5	V	Note 1
I _{IN}	Input current at any pin		100	mA	Note 1
S _{TEMP}	Storage Temperature	-65	150	°C	Note 1
A _{TEMP}	Ambient Operating Temperature	-40	85	°C	linear airflow 0 ft./min
ThetaJA	Thermal Resistance		20	°C/W	linear air flow 0ft/min
ThetaJC			6	°C/W	
M _{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating		2000	V	Note 2

NOTES:

1. Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.
2. ESD testing method is per MIL-STD-883D,M-3015.7

TABLE 2: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV _{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV _{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I _{CC}	Supply current (Measured while transmitting and receiving all 1's)		450	520	mA
P _{DD}	Power Dissipation		1.5	1.8	W
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage	2.0		5.0	V
V _{OL}	Output Low Voltage, I _{OUT} = - 4mA			0.4	V
V _{OH}	Output High Voltage, I _{OUT} = 4 mA	2.4			V
I _L	Input Leakage Current ¹			±10	µA
C _I	Input Capacitance			10	pF
C _L	Load Capacitance			10	pF

NOTES:

1. Not applicable for pins with pull-up or pull-down resistors.
2. The Digital inputs and outputs are TTL 5V compliant.

2.0 TIMING CHARACTERISTICS

FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75L04D (DUAL-RAIL DATA)

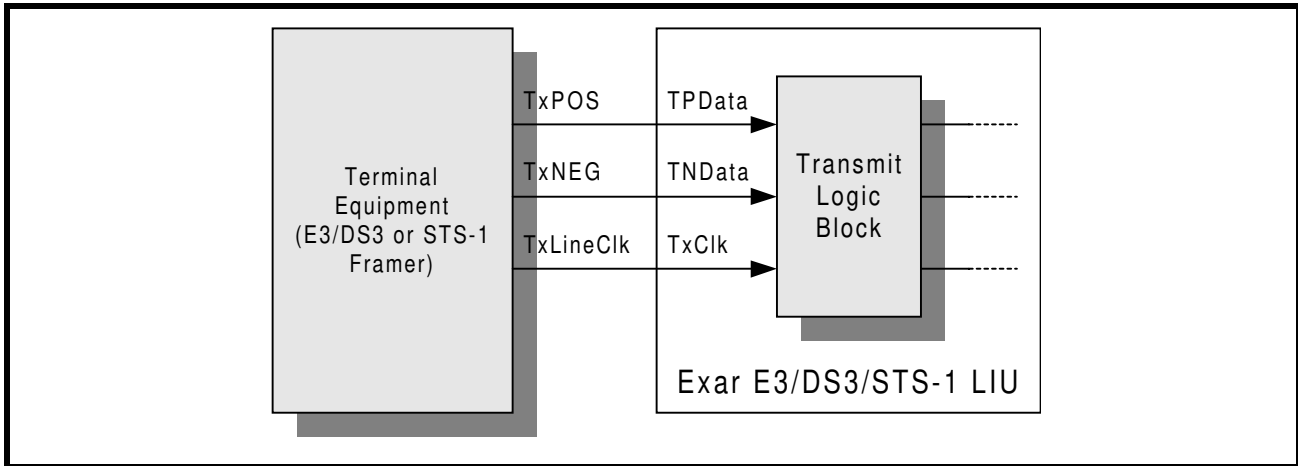
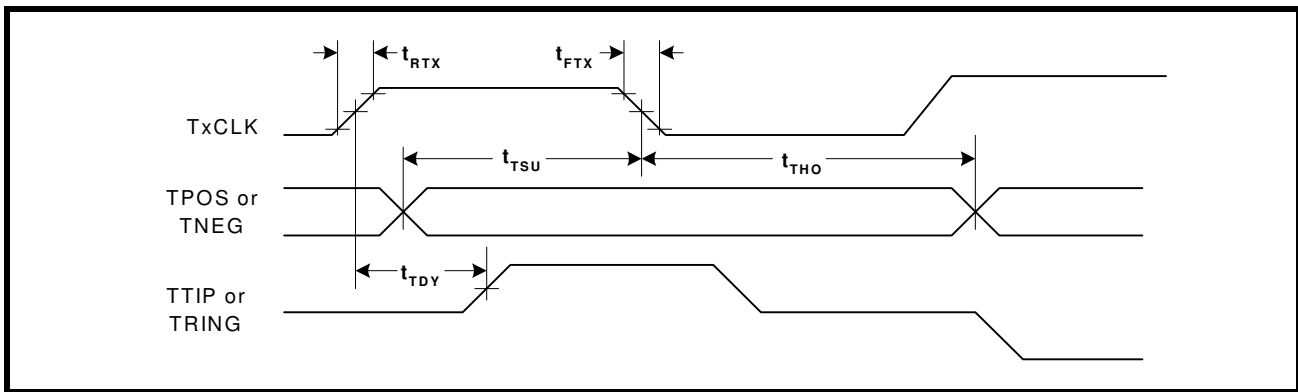
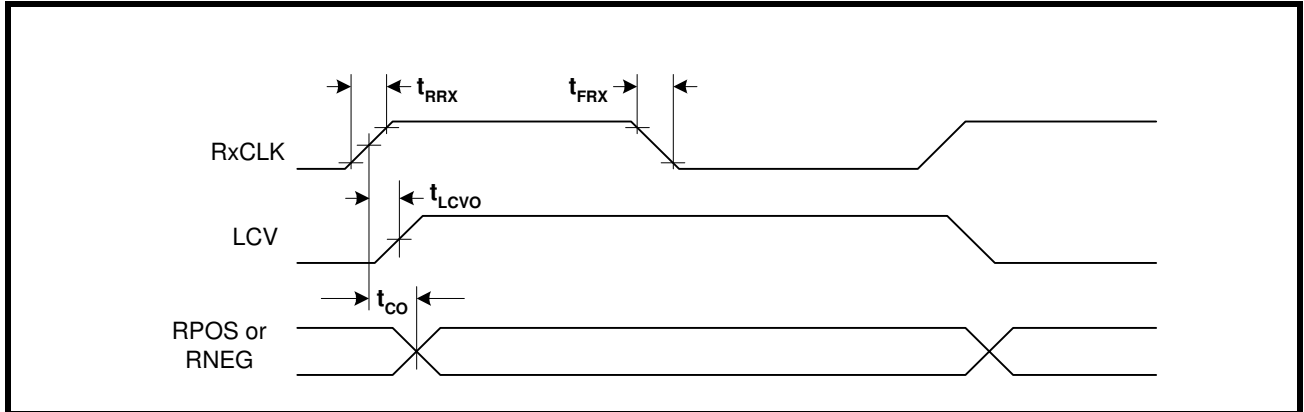


FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING



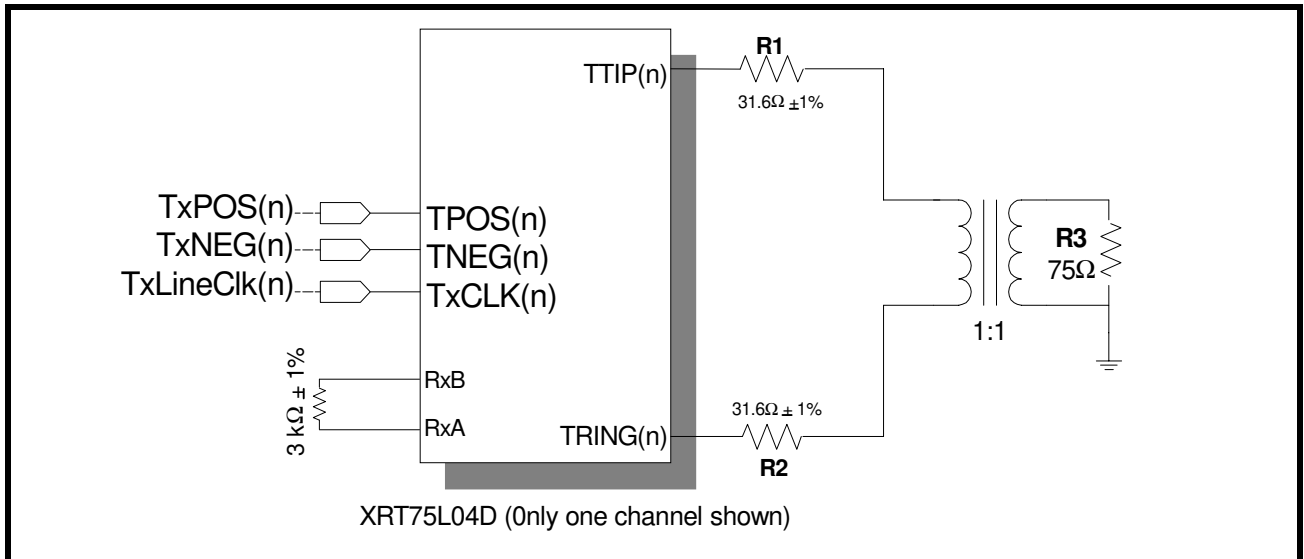
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle	30	50	70	%
	E3		34.368		MHz
	DS3		44.736		MHz
	STS-1		51.84		MHz
t _{RTX}	TxCLK Rise Time (10% to 90%)			4	ns
t _{FTX}	TxCLK Fall Time (10% to 90%)			4	ns
t _{TSU}	TPOS/TNEG to TxCLK falling set up time	3			ns
t _{THO}	TPOS/TNEG to TxCLK falling hold time	3			ns
t _{TDY}	TTIP/TRING to TxCLK rising propagation delay time		8		ns

FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle	45	50	55	%
	E3		34.368		MHz
	DS3		44.736		MHz
	STS-1		51.84		MHz
t_{RRX}	RxCLK rise time (10% to 90%)		2	4	ns
t_{FRX}	RxCLK falling time (10% to 90%)		2	4	ns
t_{CO}	RxCLK to RPOS/RNEG delay time			4	ns
t_{LCVO}	RxCLK to rising edge of LCV output delay		2.5		ns

FIGURE 6. TRANSMIT INTERFACE CIRCUIT FOR E3, DS3 AND STS-1 RATES



3.0 LINE SIDE CHARACTERISTICS:

3.1 E3 line side parameters:

The XRT75L04D line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mb/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mb/s is shown in Figure 7.

FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

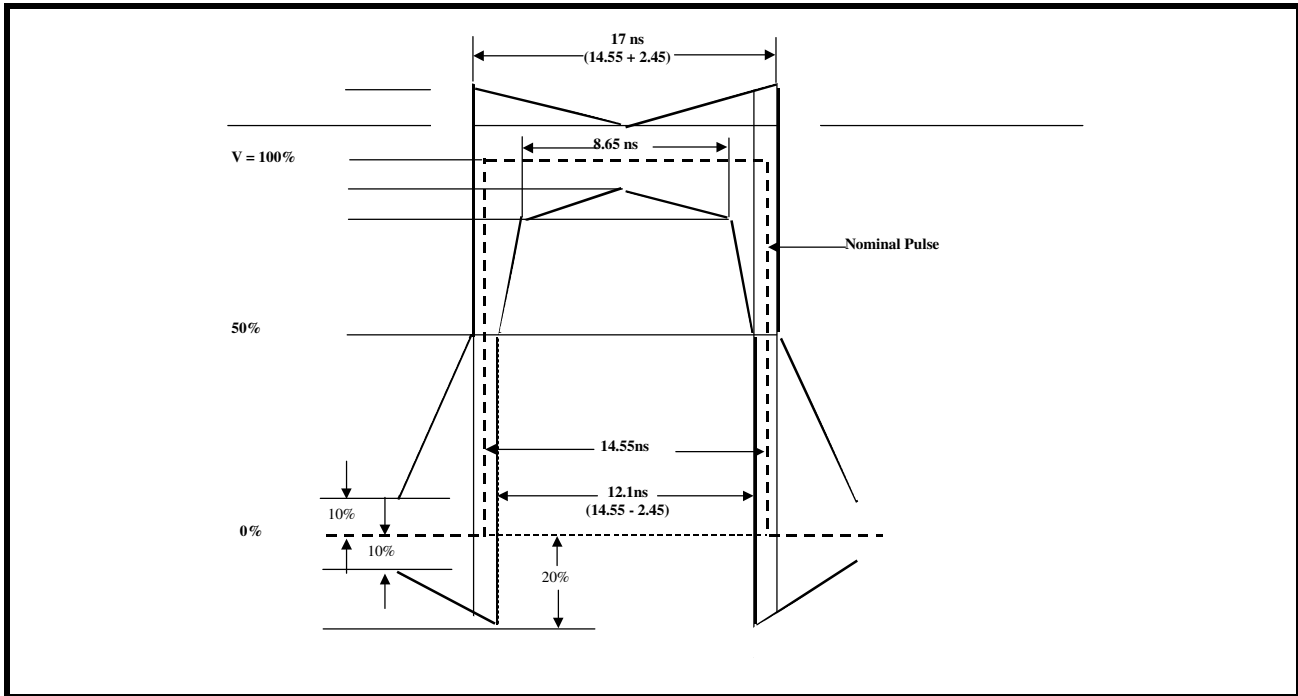


TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V _{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)		1200		feet
Interference Margin	-20	-16		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.30		UI _{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

NOTE: The above values are at

TA = 25°C and V_{DD} = 3.3 V ± 5%.

FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

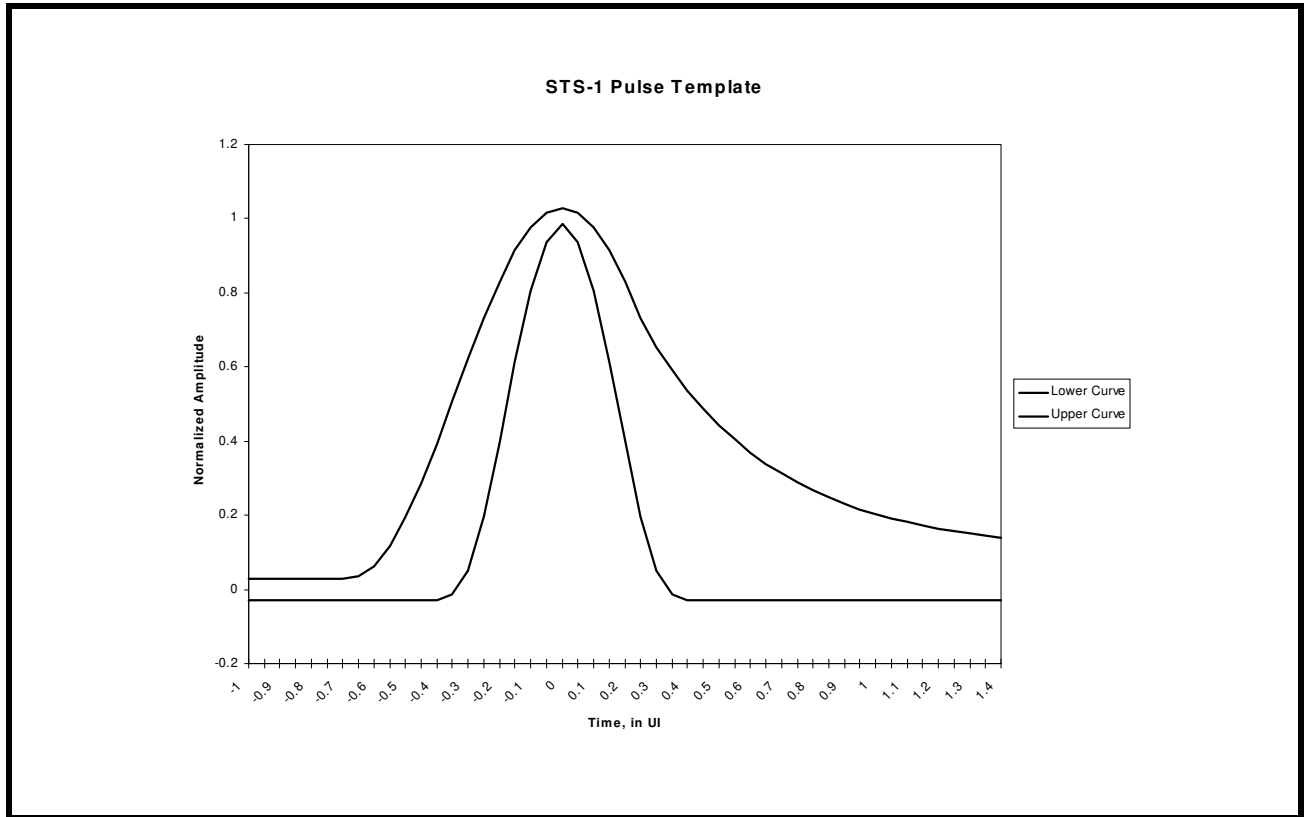


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5 \left[1 + \sin \frac{\pi}{2} \left(1 + \frac{T}{0.18} \right) \right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5 \left[1 + \sin \frac{\pi}{2} \left(1 + \frac{T}{0.34} \right) \right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \times e^{-2.4[T-0.26]}$