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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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GENERAL DESCRIPTION

The XRT75R12 is a twelve channel fully integrated Line Interface Unit (LIU) featuring EXAR's R^3 Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 12 independent Receivers, Transmitters and Jitter Attenuators in a single 420 Lead TBGA package.

Each channel of the XRT75R12 can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75R12's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75R12 incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

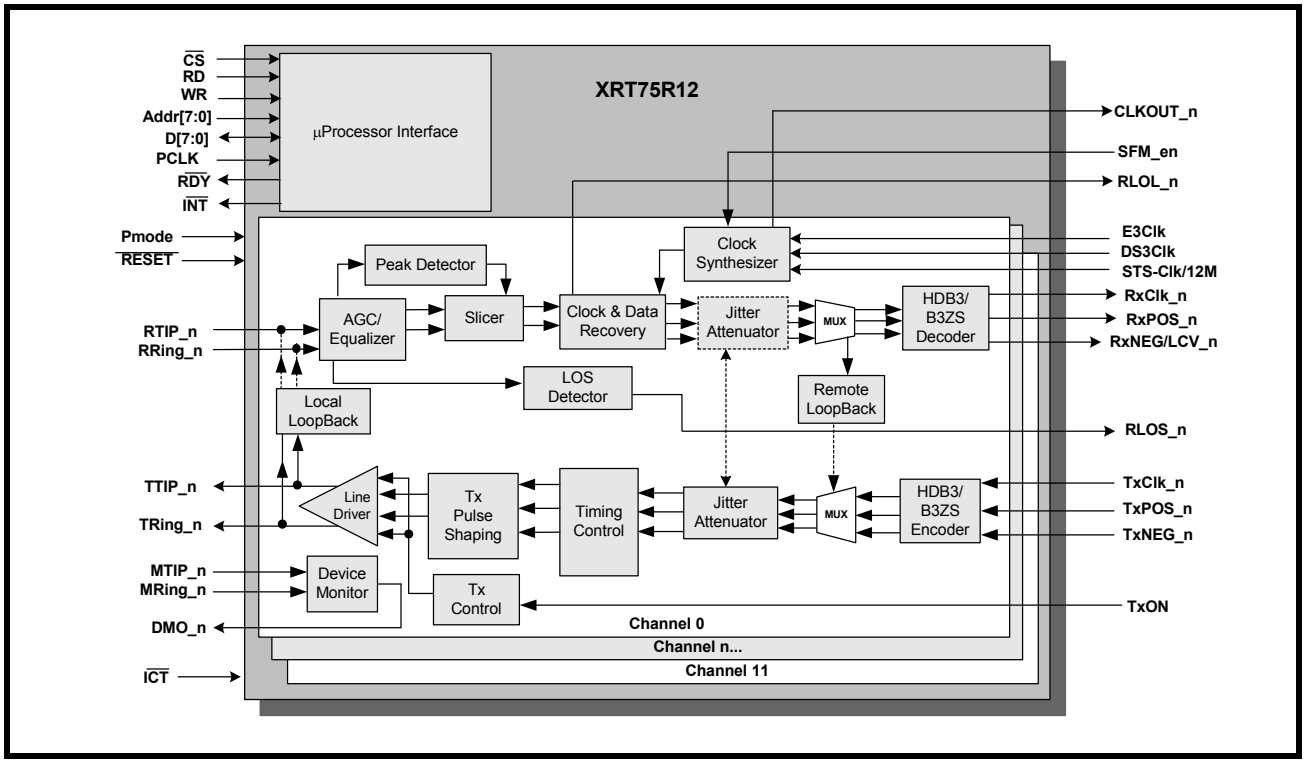
The XRT75R12 provides a Parallel Microprocessor Interface for programming and control.

The XRT75R12 supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

APPLICATIONS

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75R12



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75R12IB-L	420 Lead TBGA	-40°C to +85°C

FEATURES

RECEIVER

- R^3 Technology (Reconfigurable, Relayless Redundancy)
- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER

- R^3 Technology (Reconfigurable, Relayless Redundancy)
- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be independently turned on or off
- Transmitters provide Voltage Output Drive

JITTER ATTENUATOR

- On chip advanced crystal-less Jitter Attenuator for each channel
- Jitter Attenuator can be selected in Receive, Transmit path, or disabled
- Meets ETSI TBR 24 Jitter Transfer Requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- 16 or 32 bits selectable FIFO size

CONTROL AND DIAGNOSTICS

- Parallel Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring
- Each channel supports Analog, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant digital inputs
- Available in 420 pin TBGA Thermally enhanced Package
- - 40°C to 85°C Industrial Temperature Range

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Lock (LOL) Alarm
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

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PIN DESCRIPTIONS (BY FUNCTION)

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
P4	TxON	I	**Transmit On/Off Input** Upon power up, the transmitters are powered on. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 12 transmitters are powered off. ***NOTE:*** *TxON is ideal for redundancy applications. See the R^3 Technology section of this datasheet for more details. Internally pulled "High".*
F22 AA22 H22 Y23 G26 AA25 G1 AA2 H5 Y4 F5 AA5	TxCLK0 TxCLK1 TxCLK2 TxCLK3 TxCLK4 TxCLK5 TxCLK6 TxCLK7 TxCLK8 TxCLK9 TxCLK10 TxCLK11	I	**Transmit Clock Input** These input pins have three functions: • They function as the timing source for the Transmit Section of the corresponding channel within the XRT75R12. • They are used by the Transmit Section of the LIU IC to sample the corresponding TxPOS_n and TxNEG_n input pins. • They are used to clock the PRBS generator ***NOTE:*** *The user is expected to supply a 44.736MHz ± 20ppm clock signal (for DS3 applications), 34.368MHz ± 20 ppm clock signal (for E3 applications) or a 51.84MHz ± 4.6ppm clock signal (for STS-1, Stratum 3E or better applications).*
E23 AB24 J22 AA23 G25 AA26 G2 AA1 J5 AA4 E4 AB3	TxPOS0 TxPOS1 TxPOS2 TxPOS3 TxPOS4 TxPOS5 TxPOS6 TxPOS7 TxPOS8 TxPOS9 TxPOS10 TxPOS11	I	**Transmit Positive Data Input** The function of these digitial input pins depends upon whether the corresponding channel has been configured to operate in the Single-Rail or Dual-Rail Mode. **Single Rail Mode - Transmit Data Input** Operating in the Single-Rail Mode; all transmit input data will be serially applied to this input pin. This signal will be latched into the Transmit Section circuitry on the active edge of the TxCLK_n signal. The Transmit Section of the LIU IC will then encode this data into either the B3ZS line code (for DS3 and STS-1 applications) or the HDB3 line code (for E3 applications). **Dual Rail Mode - Transmit Positive Data Input** In the Dual-Rail Mode, the user should apply a pulse to this input pin when a positive-polarity pulse is to be transmitted onto the line. This signal will be latched into the Transmit Section circuitry upon the active edge of the TxCLK_n signal,. The Transmit Section of the LIU IC will NOT encode this data into either the B3ZS or HDB3 line codes. If the user configures the LIU IC to operate in the Dual-Rail Mode, B3ZS/HDB3 encoding must have already been done prior to this input.

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
C25 AB25 H23 W23 H24 Y26 H3 Y1 H4 W4 C2 AB2	TxNEG0 TxNEG1 TxNEG2 TxNEG3 TxNEG4 TxNEG5 TxNEG6 TxNEG7 TxNEG8 TxNEG9 TxNEG10 TxNEG11	I	**Transmit Negative Data Input** When a Channel has been configured to operate in the Dual-Rail Mode, the user should apply a pulse to this input pin anytime the Transmit Section of the LIU IC to generate a negative-polarity pulse onto the line. This signal will be latched into the Transmit Section circuitry upon the active edge of the TxCLK_n signal. ***NOTE:*** *In the Single-Rail Mode, this input pin has no function, and should be tied to GND.*
B24 AE24 C20 AD20 C16 AD16 C11 AD11 C7 AD7 C3 AD3	TTip0 TTip1 TTip2 TTip3 TTip4 TTip5 TTip6 TTip7 TTip8 TTip9 TTip10 TTip11	O	**Transmit TTIP Output - Positive Polarity Signal** These output pins along with the corresponding TRING_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel of the XRT75R12. Connect this signal and the corresponding TRING_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a high ervoltage than its corresponding TRING_n output pins. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a lower voltage than its corresponding TRING_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the TxON input pin or bit-field is set to "0".*
C24 AD24 B20 AE20 B16 AE16 B11 AE11 B7 AE7 B3 AE3	TRing0 TRing1 TRing2 TRing3 TRing4 TRing5 TRing6 TRing7 TRing8 TRing9 TRing10 TRing11	O	**Transmit Ring Output - Negative Polarity Signal** These output pins along with the corresponding TTIP_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel, within the XRT75R12. Connect this signal and the corresponding TTIP_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a lower voltage than its corresponding TTIP_n output pin. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a higher voltage than its corresponding TTIP_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the TxON input pin or bit-field is set to "0".*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
C23 AD23 D19 AC19 D15 AC15 E11 AB11 E8 AB8 C4 AD4	MTip0 MTip1 MTip2 MTip3 MTip4 MTip5 MTip6 MTip7 MTip8 MTip9 MTip10 MTip11	I	**Monitor Tip Input - Positive Polarity Signal** These input pins along with MRing_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. (1) To monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this pin MUST be connected to the corresponding TTIP_n output pin via a 270Ω series resistor. Similarly, the MRING_n input pin MUST also be connected to its corresponding TRING_n output pin via a 270Ω series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTE:*** *These input pins are inactive if the user chooses to internally monitor the Transmit Output line signal.*
D23 AC23 E19 AB19 E16 AB16 D10 AC10 D8 AC8 D4 AC4	MRing0 MRing1 MRing2 MRing3 MRing4 MRing5 MRing6 MRing7 MRing8 MRing9 MRing10 MRing11	I	**Monitor Ring Input** These input pins along with MTIP_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. (1) To monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this input pin MUST be connected to the corresponding TRING_n output pin via a 270Ω series resistor. Similarly, the MTIP_n input pin MUST be connected to its corresponding TTIP_n output pin via a 270Ω series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" to indicate a possible fault condition in the Transmit Output Line signal path. ***NOTE:*** *These input pins are inactive if the user chooses to internally monitor the Transmit Output line signal.*
N3 N4 N5 N1 M1 L2 M2 M3 M4 M5 K2 J1	DMO0 DMO1 DMO2 DMO3 DMO4 DMO5 DMO6 DMO7 DMO8 DMO9 DMO10 DMO11	O	**Drive Monitor Output** These output signals are used to indicate a fault condition within the Transmit Output signal path. This output pin will toggle "High" anytime the Transmit Drive Monitor circuitry either, via the corresponding MTIP and MRING input pins or internally, detects no bipolar pulses via the Transmit Output line signal (e.g., via the TTIP_m and TRING_m output pins) for 128 bit-periods. This output pin will be driven "Low" anytime the Transmit Drive Monitor circuitry has detected at least one bipolar pulse via the Transmit Output line signal within the last 128 bit periods.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
D25 AD25 G23 AA24 J24 U24 J3 U3 G4 AA3 D2 AD2	RLOS0 RLOS1 RLOS2 RLOS3 RLOS4 RLOS5 RLOS6 RLOS7 RLOS8 RLOS9 RLOS10 RLOS11	O	**Receive Loss of Signal Output Indicator** This output pin indicates Loss of Signal (LOS) Defect condition for the corresponding channel. "Low" - Indicates that the corresponding Channel is NOT currently declaring the LOS defect condition. "High" - Indicates that the corresponding Channel is currently declaring the LOS defect condition.
G22 AB26 K22 U22 L24 W25 L3 W2 K5 U5 G5 AB1	RLOL0 RLOL1 RLOL2 RLOL3 RLOL4 RLOL5 RLOL6 RLOL7 RLOL8 RLOL9 RLOL10 RLOL11	O	**Receive Loss of Lock Output Indicator** This output pin indicates Loss of Lock (LOL) condition for the corresponding channel. "Low" - Indicates that the corresponding Channel is NOT declaring the LOL condition. "High" - Indicates that the corresponding Channel is currently declaring the LOL condition. ***NOTE:*** *The Receive Section of a given channel will declare the LOL condition anytime the frequency of the Recovered Clock (RCLK) signal differs from that of the reference clock programmed for that channel by 0.5% or more.*
E25 AD26 G24 Y24 L22 T22 L5 T5 G3 Y3 E2 AD1	RxPOS0 RxPOS1 RxPOS2 RxPOS3 RxPOS4 RxPOS5 RxPOS6 RxPOS7 RxPOS8 RxPOS9 RxPOS10 RxPOS11	O	**Receive Positive Data Output** The function of these output pins depends upon whether the channel has been configured to operate in the Single-Rail or Dual-Rail Mode. **Dual-Rail Mode - Receive Positive Polarity Data Output** If the channel has been configured to operate in the Dual-Rail Mode, then all positive-polarity data will be output via this pin. The negative-polarity data will be output via the corresponding RxNEG_n pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a positive-polarity pulse via the RTIP/RRING input pins. The data output via this pin is updated upon the active edge of RxCLK_n output clock signal. **Single-Rail Mode - Receive Data Output** In the Single-Rail Mode, all Receive (or Recovered) data will be output via this pin. The data output via this pin is updated upon the active edge of RxCLK_n output clock signal.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
F23 AC26 F24 U23 L23 T24 L4 T3 F3 U4 F4 AC1	RxNEG/LCV0 RxNEG/LCV1 RxNEG/LCV2 RxNEG/LCV3 RxNEG/LCV4 RxNEG/LCV5 RxNEG/LCV6 RxNEG/LCV7 RxNEG/LCV8 RxNEG/LCV9 RxNEG/LCV10 RxNEG/LCV11	O	**Receive Negative Data Output/Line Code Violation** The function of these pins depends on whether the XRT75R12 is configured in Single Rail or Dual Rail mode. **Dual-Rail Mode - Receive Negative Polarity Data Output** In the Dual-Rail Mode, all negative-polarity data will be output via this pin. The positive-polarity data will be output via the corresponding RxPOS_n output pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RxCLK_n anytime it receives a negative-polarity pulse via the RTIP/RRING input pins. The data output via this pin is updated upon the active edge of the RCLK_n output clock signal. **Single-Rail Mode - Line Code Violation Indicator Output** In the Single-Rail Mode, this output pin will function as the Line Code Violation indicator output. In this configuration, the Receive Section of the Channel will pulse this output pin "High" for at least one RCLK period whenever it detects either an LCV (Line Code Violation) or an EXZ (Excessive Zero Event). The data that is output via this pin is updated upon the active edge of the RCLK_n output clock signal.
E24 AC25 J23 V23 K24 T23 K3 T4 J4 V4 E3 AC2	RxCLK0 RxCLK1 RxCLK2 RxCLK3 RxCLK4 RxCLK5 RxCLK6 RxCLK7 RxCLK8 RxCLK9 RxCLK10 RxCLK11	O	**Receive Clock Output** This output pin functions as the Receive or recovered clock signal. All Receive (or recovered) data will output via the RxPOS_n and RxNEG_n outputs upon the active edge of this clock signal. Additionally, if the device/channel has been configured to operate in the Single-Rail Mode, then the RNEG_n/LCV_n output pins will also be updated upon the active edge of this clock signal.

RECEIVE LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
B22 AE22 B18 AE18 A14 AF14 D13 AC13 B9 AE9 B5 AE5	RTip0 RTip1 RTip2 RTip3 RTip4 RTip5 RTip6 RTip7 RTip8 RTip9 RTip10 RTip11	I	**Receive TIP Input** These input pins along with the corresponding RRing_n input pin function as the Receive DS3/E3/STS-1 Line input signal for a given channel of the XRT75R12. Cconnect this signal and the corresponding RRING_n input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a higher voltage than its corresponding RRING_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a lower voltage than its corresponding RRING_n input pin.
C22 AD22 C18 AD18 B14 AE14 C13 AD13 C9 AD9 C5 AD5	RRing0 RRing1 RRing2 RRing3 RRing4 RRing5 RRing6 RRing7 RRing8 RRing9 RRing10 RRing11	I	**Receive Ring Input** These input pins along with the corresponding RTIP_n input pin function as the Receive DS3/E3/STS-1 Line input signal for a given channel of the XRT75R12. Connect this signal and the corresponding RTIP_n input signal to a 1:1 transformer. (See Figure 6) Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a lower voltage than its corresponding RTIP_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a higher voltage than its corresponding RTIP_n input pin.

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
R5	SFM_EN	I	**Single Frequency Mode Enable** This input pin is used to configure the XRT75R12 to operate in the SFM (Single Frequency Mode). When this feature is invoked, the SFM Synthesizer will become active. By applying a 12.288MHz clock signal to the STS-1Clk/12M pin, the XRT75R12 will generate all of the appropriate clock signals (e.g., 34.368MHz, 44.736MHz or 51.84). The XRT75R12 internal circuitry will route each of these synthesized clock signals to the appropriate nodes of the corresponding channels in the XRT75R12. "Low" - Disables the Single Frequency Mode. In this setting, the user is required to supply to the E3CLK, DS3CLK or STS-1CLK input pins all of the relevant clock signals that are to be used within the chip. "High" - Enables the Single-Frequency Mode. ***NOTE:*** *This input pin is internally pulled low.*
R1	E3Clk	I	**E3 Clock Input (34.368 MHz ± 20 ppm)** If any one of the channels is configured in E3 mode, a reference clock of 34.368 MHz ± 20 ppm is applied to this input pin. If the LIU is used in E3 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. ***NOTE:*** *SFM mode negates the need for this clock*
T1	DS3Clk	I	**DS3 Clock Input (44.736 MHz ± 20 ppm)** If any one of the channels is configured in DS3 mode, a reference clock of 44.736 MHz ± 20 ppm is applied to this input pin. ***NOTE:*** *SFM mode negates the need for this clock*
U1	STS-1Clk/12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm)** If any one of the channels is configured in STS-1 mode, a reference clock of 51.84MHz ± 20 ppm is applied to this input pin. If the LIU is used in STS-1 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. **Single Frequency Mode Clock Input (12.288MHz ± 20 ppm)** In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the rates (E3, DS3 or STS-1).
C26 W22 K23 W24 J25 V25 J2 V2 K4 W3 C1 W5	CLKOUT0 CLKOUT1 CLKOUT2 CLKOUT3 CLKOUT4 CLKOUT5 CLKOUT6 CLKOUT7 CLKOUT8 CLKOUT9 CLKOUT10 CLKOUT11	O	**Reference Clock Out** A reference clock pin is provided for each channel that will supply a precise data rate frequency derived from either the Clock input pin (E3Clk, DS3Clk, or STS-1Clk) or the 12.288MHz input in SFM mode. This frequency will be as stable as the original source. It is designed to provide the attached framer with its appropriate reference clock.

GENERAL CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
P3	TEST	****	**Factory Test Mode Input Pin** This pin must be connected to GND for normal operation. ***NOTE:*** *This input pin is internally pulled "Low".*
AE25	TRST	I	**Test Reset** Test Boundary Scan
AB23	TMS	I	**Test Mode Select** Test Boundary Scan
AB5	TCK	I	**Test Clock** Test Boundary Scan
AB4	TDI	I	**Test Data Input** Test Boundary Scan
AE2	TDO	O	**Test Data Output** Test Boundary Scan

MICROPROCESSOR PARALLEL INTERFACE -

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
J26	Pmode	I	**This pin controls the Microprocessor Parallel Interface mode.** "High" sets a Synchronous clocked interface mode with a clock from the Host. "Low" sets an Asynchronous mode where a clock internal to the XRT75R12 will time the operations.
P24	PCLK	I	High speed clock supplied by the Host to provide timing in the Synchronous Interface mode. This signal must be a square-wave.
N24	$\overline{CS}$	I	**Chip Select Input (active low)** Initiates a read or write operation. When "High", no parallel communication is active between the LIU and the Host.
N22	$\overline{WR}$	I	**Write Input (active low)** Enables the Host to write data D[7:0] into the LIU register space at address Addr[7:0].
N23	$\overline{RD}$	I	**Read Input (active low)** Commands the LIU to transfer the contents of a register specified by Addr[7:0] to the Host.
N25	$\overline{RDY}$	O	**Ready Line Output (active low)** Provides a handshake between the LIU and the Host that communicates when an operation has been completed. ***NOTE:*** *This pin must be pulled "High" with a 3kΩ ± 1% resistor.*

MICROPROCESSOR PARALLEL INTERFACE -

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
K25 M22 M23 M24 K26 L26 M26 N26	Addr0 Addr1 Addr2 Addr3 Addr4 Addr5 Addr6 Addr7	I	An eight bit direct address bus that specifies the source/destination register for a Read or Write operation.
P22 R26 T26 U26 R25 R24 R23 R22	D0 D1 D2 D3 D4 D5 D6 D7	I/O	An eight bit bi-directional data bus that provides the data into the LIU for a Write operation or the data out to the Host for a Read operation.
P26	$\overline{\text{INT}}$	O	**Interrupt Active Output (active low)** Normally, this output pin will be pulled "High". However, if the user enables interrupts within the LIU, and if those conditions occur, the XRT75R12 will signal an interrupt from the Microprocessor by pulling this output pin "Low". The Host Microprocessor must ascertain the source of the interrupt and service it. Reading the source of the interupt will clear the flag and the $\overline{\text{INT}}$ pin will go back high unless another interrupt has gone active. ***NOTES:*** *1. This pin will remain "Low" until the Interrupt has been serviced.* *2. This pin must be pulled "High" with a 3kΩ ± 1% resistor.*
N2	$\overline{\text{RESET}}$	I	**RESET Input** Pulsing this input "Low" causes the XRT75R12 to reset the contents of the on-chip Command Registers to their default values. As a consequence, the XRT75R12 will then also be operating in its default condition. For normal operation this input pin should be at a logic "High". ***NOTE:*** *This input pin is internally pulled high.*

POWER SUPPLY PINS

PIN NAME	PIN NUMBERS	DESCRIPTION
RVDD0 RVDD1 RVDD2 RVDD3 RVDD4 RVDD5 RVDD6 RVDD7 RVDD8 RVDD9 RVDD10 RVDD11	D22 AC22 D18 AC18 E15 AB15 E12 AB12 A9 AF9 D5 AC5	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
TVDD0 TVDD1 TVDD2 TVDD3 TVDD4 TVDD5 TVDD6 TVDD7 TVDD8 TVDD9 TVDD10 TVDD11	B23 AE23 B19 AE19 B15 AE15 B10 AE10 A6 AF6 B4 AE4	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
AVDD	M25, T25, AB21, AB18, AF13, AF12, AB9, AB6, R4, K1, E6, E9, A12, A13, E18, E21,	**Analog Power Supply (3.3V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
DVDD	D26, F25, H25, P25, W26, V24, Y22, AF21, AF20, AF17, AF16, AD14, AD12, AF11, AF8, AF7, AF24, AD6, AF3, Y5, V3, W1, P5, P2, H2, F2, D1, C6, A7, A3, A8, A11, C12, C14, A16, A17, A20, A21, A24	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

GROUND PINS

PIN NAME	PIN NUMBERS	DESCRIPTION
RGND0 RGND1 RGND2 RGND3 RGND4 RGND5 RGND6 RGND7 RGND8 RGND9 RGND10 RGND11	A22 AF22 A18 AF18 E14 AB14 E13 AB13 D9 AC9 A5 AF5	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9 TGND10 TGND11	A23 AF23 A19 AF19 A15 AF15 A10 AF10 B6 AE6 A4 AF4	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
AGND	A1, A2, A25, A26, B1, B2, B25, B26, C8, C10, C17, C19, C21, D17, D21, E5, E22, L25, U25, AB22, AB20, AB17, AB10, AB7, R3, L1, E7, E10, B12, B13, E17, E20, T2, U2, AC17, AC21, AD8, AD10, AD15, AD17, AD19, AD21, AE1, AE26, AE12, AE13, AF1, AF2, AF25, AF26, C15	**Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND	E26, F26, H26, P23, , V26, Y25, V22, AC24, AC20, AC16, AC14, AC12, AC11, AE8, AE17, AE21, AC7, AC6, AC3, V5, Y2, V1, R2, P1, H1, F1, E1, D3, D7, B8, D6, D11, D12, D14, D16, B17, D20, B21, D24	**Digital Ground** It's recommended that all ground pins of this device be tied together.

TABLE 1: PIN LIST BY PIN NUMBER

PIN	PIN NAME
A1	AGND
A2	AGND
A3	DVDD
A4	TGND10
A5	RGND10
A6	TVDD8
A7	DVDD
A8	DVDD
A9	RVDD8
A10	TGND6
A11	DVDD
A12	AVDD
A13	AVDD
A14	RTip4
A15	TGND4
A16	DVDD
A17	DVDD
A18	RGND2
A19	TGND2
A20	DVDD
A21	DVDD
A22	RGND0
A23	TGND0
A24	DVDD
A25	AGND
A26	AGND
B1	AGND
B2	AGND
B3	TRing10
B4	TVDD10
B5	RTip10
B6	TGND8
B7	TRing8
B8	DGND
B9	RTip8
B10	TVDD6
B11	TRing6
B12	AGND
B13	AGND
B14	RRing4
B15	TVDD4
B16	TRing4
B17	DGND
B18	RTip2
B19	TVDD2
B20	TRing2
B21	DGND
B22	RTip0
B23	TVDD0
B24	TTip0
B25	AGND
B26	AGND
C1	CLKOUT10
C2	TxNEG10
C3	TTip10
C4	MTip10
C5	RRing10
C6	DVDD
C7	TTip8
C8	AGND
C9	RRing8
C10	AGND
C11	TTip6
C12	DVDD
C13	RRing6
C14	DVDD
C15	AGND
C16	TTip4
C17	AGND
C18	RRing2
C19	AGND
C20	TTip2
C21	AGND
C22	RRing0
C23	MTip0
C24	TRing0
C25	TxNEG0
C26	CLKOUT0
D1	DVDD
D2	RLOS10
D3	DGND
D4	MRing10
D5	RVDD10
D6	DGND
D7	DGND
D8	MRing8
D9	RGND8
D10	MRing6
D11	DGND
D12	DGND
D13	RTip6
D14	DGND
D15	MTip4
D16	DGND
D17	AGND
D18	RVDD2
D19	MTip2
D20	DGND
D21	AGND
D22	RVDD0
D23	MRing0
D24	DGND
D25	RLOS0
D26	DVDD
E1	DGND
E2	RxPOS10
E3	RxCLK10
E4	TxPOS10
E5	AGND
E6	AVDD
E7	AGND
E8	MTip8
E9	AVDD
E10	AGND
E11	MTip6
E12	RVDD6
E13	RGND6
E14	RGND4
E15	RVDD4
E16	MRing4
E17	AGND
E18	AVDD
E19	MRing2
E20	AGND
E21	AVDD
E22	AGND
E23	TxPOS0
E24	RxCLK0
E25	RxPOS0
E26	DGND
F1	DGND
F2	DVDD
F3	RxNEG/LCV8
F4	RxNEG/LCV10

PIN	PIN NAME
F5	TxCLK10
F22	TxCLK0
F23	RxNEG/LCV0
F24	RxNEG/LCV2
F25	DVDD
F26	DGND
G1	TxCLK6
G2	TxPOS6
G3	RxPOS8
G4	RLOS8
G5	RLOL10
G22	RLOL0
G23	RLOS2
G24	RxPOS2
G25	TxPOS4
G26	TxCLK4
H1	DGND
H2	DVDD
H3	TxNEG6
H4	TxNEG8
H5	TxCLK8
H22	TxCLK2
H23	TxNEG2
H24	TxNEG4
H25	DVDD
H26	DGND
J1	DMO11
J2	CLKOUT6
J3	RLOS6
J4	RxCLK8
J5	TxPOS8
J22	TxPOS2
J23	RxCLK2
J24	RLOS4

PIN	PIN NAME
J25	CLKOUT4
J26	Pmode
K1	AVDD
K2	DMO10
K3	RxCLK6
K4	CLKOUT8
K5	RLOL8
K22	RLOL2
K23	CLKOUT2
K24	RxCLK4
K25	Addr0
K26	Addr4
L1	AGND
L2	DMO5
L3	RLOL6
L4	RxNEG/LCV6
L5	RxPOS6
L22	RxPOS4
L23	RxNEG/LCV4
L24	RLOL4
L25	AGND
L26	Addr5
M1	DMO4
M2	DMO6
M3	DMO7
M4	DMO8
M5	DMO9
M22	Addr1
M23	Addr2
M24	Addr3
M25	AVDD
M26	Addr6
N1	DMO3
N2	$\overline{\text{RESET}}$

PIN	PIN NAME
N3	DMO0
N4	DMO1
N5	DMO2
N22	$\overline{\text{WR}}$
N23	$\overline{\text{RD}}$
N24	$\overline{\text{CS}}$
N25	$\overline{\text{RDY}}$
N26	Addr7
P1	DGND
P2	DVDD
P3	TEST
P4	TxON
P5	DVDD
P22	D0
P23	DGND
P24	PCLK
P25	DVDD
P26	$\overline{\text{INT}}$
R1	E3Clk
R2	DGND
R3	AGND
R4	AVDD
R5	SFM_EN
R22	D7
R23	D6
R24	D5
R25	D4
R26	D1
T1	DS3Clk
T2	AGND
T3	RxNEG/LCV7
T4	RxCLK7
T5	RxPOS7
T22	RxPOS5

PIN	PIN NAME
T23	RxCLK5
T24	RxNEG/LCV5
T25	AVDD
T26	D2
U1	STS-1Clk/12M
U2	AGND
U3	RLOS7
U4	RxNEG/LCV9
U5	RLOL9
U22	RLOL3
U23	RxNEG/LCV3
U24	RLOS5
U25	AGND
U26	D3
V1	DGND
V2	CLKOUT7
V3	DVDD
V4	RxCLK9
V5	DGND
V22	DGND
V23	RxCLK3
V24	DVDD
V25	CLKOUT5
V26	DGND
W1	DVDD
W2	RLOL7
W3	CLKOUT9
W4	TxNEG9
W5	CLKOUT11
W22	CLKOUT1
W23	TxNEG3
W24	CLKOUT3
W25	RLOL5
W26	DVDD

PIN	PIN NAME
Y1	TxNEG7
Y2	DGND
Y3	RxPOS9
Y4	TxCLK9
Y5	DVDD
Y22	DVDD
Y23	TxCLK3
Y24	RxPOS3
Y25	DGND
Y26	TxNEG5
AA1	TxPOS7
AA2	TxCLK7
AA3	RLOS9
AA4	TxPOS9
AA5	TxCLK11
AA22	TxCLK1
AA23	TxPOS3
AA24	RLOS3
AA25	TxCLK5
AA26	TxPOS5
AB1	RLOL11
AB2	TxNEG11
AB3	TxPOS11
AB4	TDI
AB5	TCK
AB6	AVDD
AB7	AGND
AB8	MTip9
AB9	AVDD
AB10	AGND
AB11	MTip7
AB12	RVDD7
AB13	RGND7
AB14	RGND5

PIN	PIN NAME
AB15	RVDD5
AB16	MRing5
AB17	AGND
AB18	AVDD
AB19	MRing3
AB20	AGND
AB21	AVDD
AB22	AGND
AB23	TMS
AB24	TxPOS1
AB25	TxNEG1
AB26	RLOL1
AC1	RxNEG/LCV11
AC2	RxCLK11
AC3	DGND
AC4	MRing11
AC5	RVDD11
AC6	DGND
AC7	DGND
AC8	MRing9
AC9	RGND9
AC10	MRing7
AC11	DGND
AC12	DGND
AC13	RTip7
AC14	DGND
AC15	MTip5
AC16	DGND
AC17	AGND
AC18	RVDD3
AC19	MTip3
AC20	DGND
AC21	AGND
AC22	RVDD1

PIN	PIN NAME
AC23	MRing1
AC24	DGND
AC25	RxCLK1
AC26	RxNEG/LCV1
AD1	RxPOS11
AD2	RLOS11
AD3	TTip11
AD4	MTip11
AD5	RRing11
AD6	DVDD
AD7	TTip9
AD8	AGND
AD9	RRing9
AD10	AGND
AD11	TTip7
AD12	DVDD
AD13	RRing7
AD14	DVDD
AD15	AGND
AD16	TTip5
AD17	AGND
AD18	RRing3
AD19	AGND
AD20	TTip3
AD21	AGND
AD22	RRing1
AD23	MTip1
AD24	TRing1
AD25	RLOS1
AD26	RxPOS1
AE1	AGND
AE2	TDO
AE3	TRing11
AE4	TVDD11

PIN	PIN NAME
AE5	RTip11
AE6	TGND9
AE7	TRing9
AE8	DGND
AE9	RTip9
AE10	TVDD7
AE11	TRing7
AE12	AGND
AE13	AGND
AE14	RRing5
AE15	TVDD5
AE16	TRing5
AE17	DGND
AE18	RTip3
AE19	TVDD3
AE20	TRing3
AE21	DGND
AE22	RTip1
AE23	TVDD1
AE24	TTip1
AE25	TRST
AE26	AGND
AF1	AGND
AF2	AGND
AF3	DVDD
AF4	TGND11
AF5	RGND11
AF6	TVDD9
AF7	DVDD
AF8	DVDD
AF9	RVDD9
AF10	TGND7
AF11	DVDD
AF12	AVDD

PIN	PIN NAME
AF13	AVDD
AF14	RTip5
AF15	TGND5
AF16	DVDD
AF17	DVDD
AF18	RGND3
AF19	TGND3
AF20	DVDD
AF21	DVDD
AF22	RGND1
AF23	TGND1
AF24	DVDD
AF25	AGND
AF26	AGND

FUNCTIONAL DESCRIPTION

The XRT75R12 is a twelve channel fully integrated Line Interface Unit featuring EXAR's R^3 Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 12 independent Receivers, Transmitters and Jitter Attenuators in a single 420 Lead TBGA package. Each channel can be independently programmed to support E3, DS-3 or STS-1 line rates using one input clock reference of 12.288MHz in Single Frequency Mode (SFM). The LIU is responsible for providing the physical connection between a line interface and an aggregate mapper or framing device. Along with the analog-to-digital processing, the LIU offers monitoring and diagnostic features to help optimize network design implementation. A key characteristic within the network topology is Automatic Protection Switching (APS). EXAR's proven expertise in providing redundany solutions has paved the way for R^3 Technology.

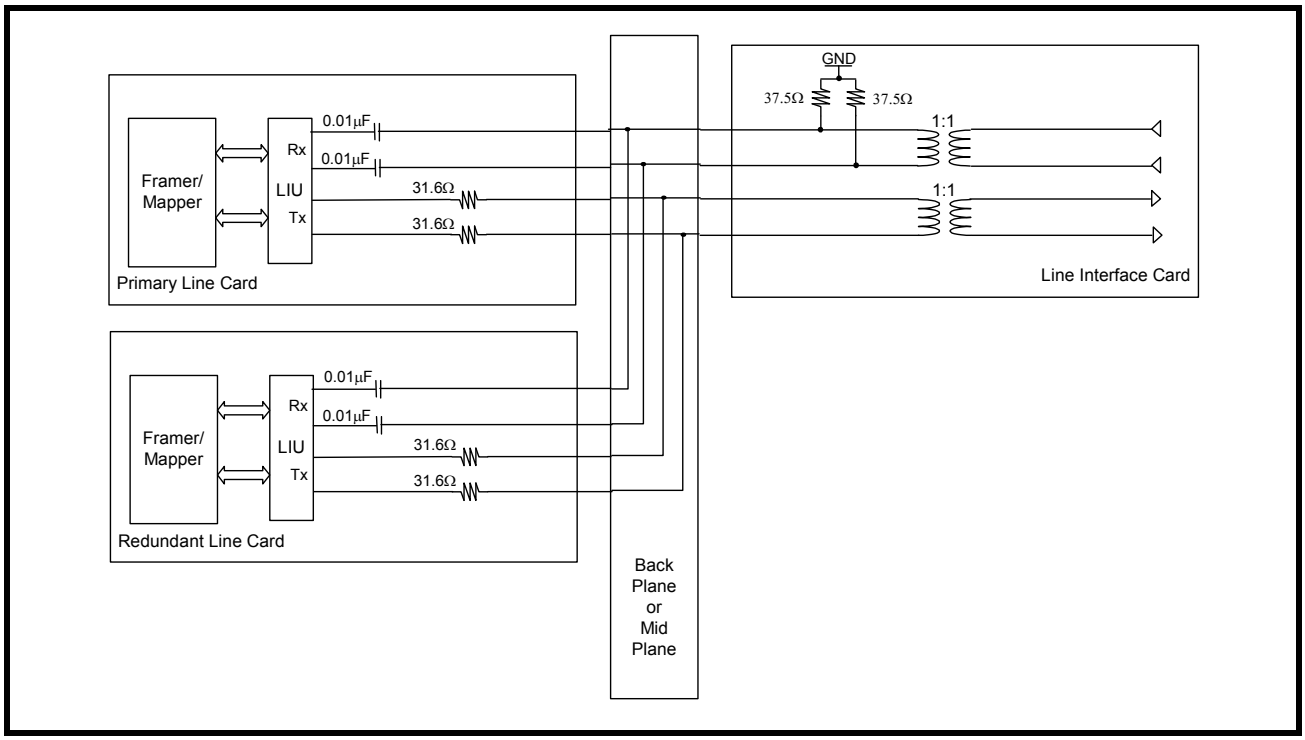
1.0 R^3 TECHNOLOGY (RECONFIGURABLE, RELAYLESS REDUNDANCY)

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. EXAR's R^3 technology has re-defined E3/DS-3/STS-1 LIU design for 1:1 and 1+1 redundancy applications. Without relays and one Bill of Materials, EXAR offers multi-port, integrated LIU solutions to assist high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R^3 Technology with EXAR's world leading line interface units.

1.1 Network Architecture

A common network design that supports 1:1 or 1+1 redundancy consists of N primary cards along with N backup cards that connect into a mid-plane or back-plane architecture without transformers installed on the network cards. In addition to the network cards, the design has a line interface card with one source of transformers, connectors, and protection components that are common to both network cards. With this design, the bill of materials is reduced to the fewest amount of components. See **Figure 2**. for a simplified block diagram of a typical redundancy design.

FIGURE 2. NETWORK REDUNDANCY ARCHITECTURE



2.0 CLOCK SYNTHESIZER

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS-3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS-3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS-3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS-3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 3. Reference clock performance specifications can be found on Table 2 below.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR

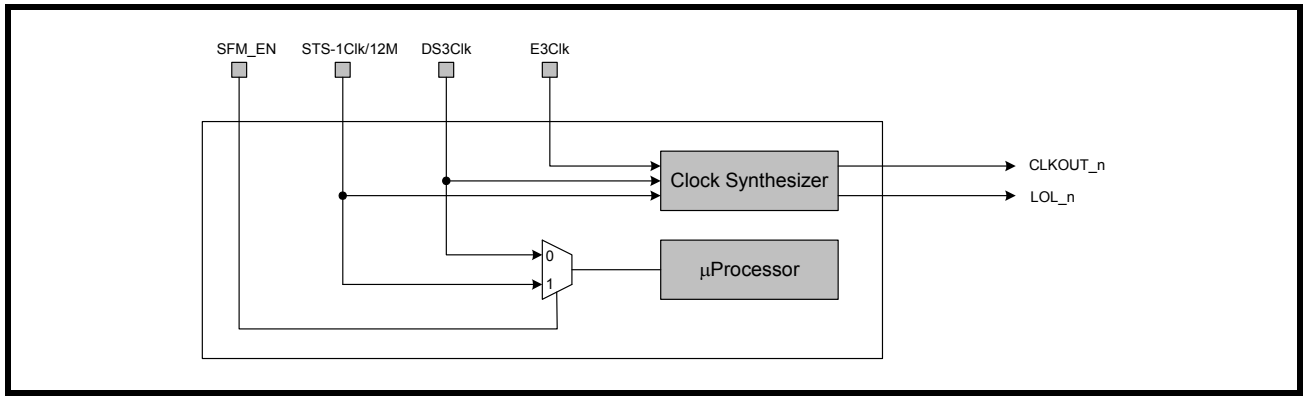


TABLE 2: REFERENCE CLOCK PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference Clock Duty Cycle	40		60	%
REF_{E3}	E3 Reference Clock Frequency Tolerance[1]	-20		+20	ppm
REF_{DS3}	DS3 Reference Clock Frequency Tolerance[1]	-20		+20	ppm
REF_{STS1}	STS-1 Reference Clock Frequency Tolerance[1]	-20		+20	ppm
REF_{SFM}	SFM Reference Clock Frequency Tolerance[1]	-20		+20	ppm
t_{RISE_REFCLK}	Reference Clock Rise Time (10% to 90%)			5	ns
t_{FALL_REFCLK}	Reference Clock Fall Time (90% to 10%)			5	ns
CLK_{JIT}	Reference Clock Jitter Stability[2]			0.005	UI_{p2p}

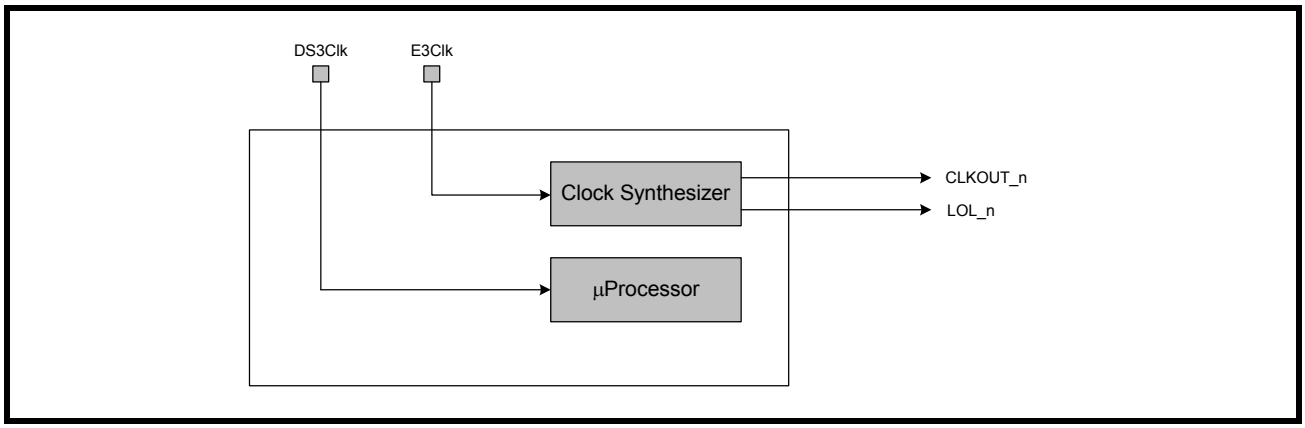
NOTES:

1. *Required to meet Bellcore GR-499 specification on frequency stability requirements. However, the LIU can functionally operate with ±100 ppm without meeting the required specifications.*
2. *Reference clock jitter limits are required for the transmit output to meet ITU-T and Bellcore system level jitter requirements.*

2.1 Clock Distribution

Network cards that are designed to support multiple line rates which are not configured for single frequency mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS-3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. If however, multiple line rates will not be supported, i.e. E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.

FIGURE 4. CLOCK DISTRIBUTION CONGIFURED IN E3 MODE WITHOUT USING SFM

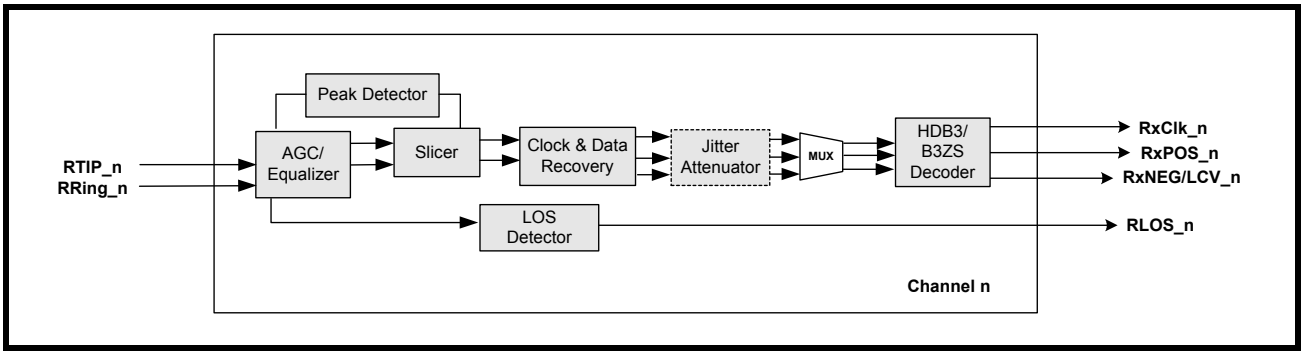


NOTE: *For one input clock reference, the single frequency mode should be used.*

3.0 THE RECEIVER SECTION

The receiver is designed so that the LIU can recover clock and data from an attenuated line signal caused by cable loss or flat loss according to industry specifications. Once data is recovered, it is processed and presented at the receiver outputs according to the format chosen to interface with a Framer/Mapper or ASIC. This section describes the detailed operation of various blocks within the receive path. A simplified block diagram of the receive path is shown in Figure 5.

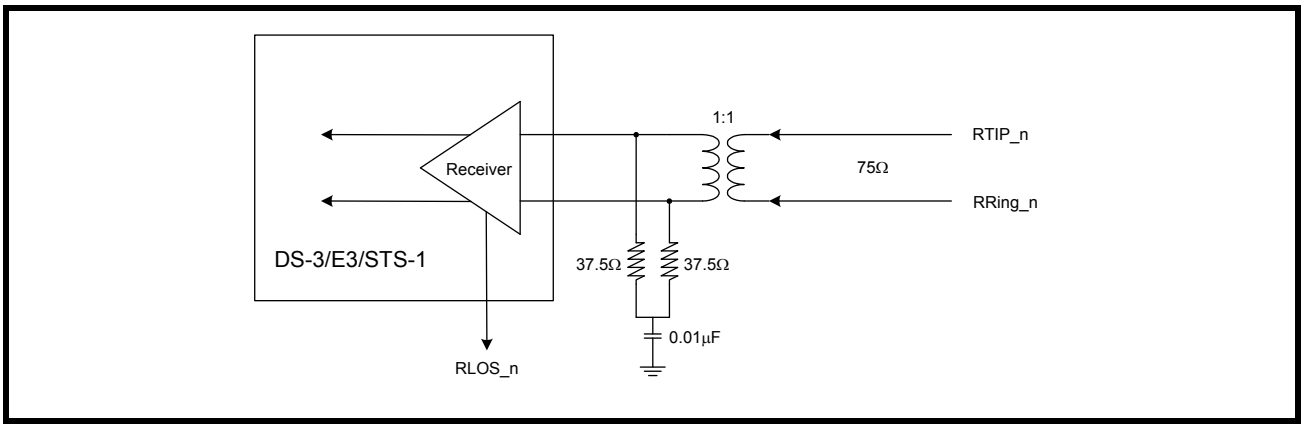
FIGURE 5. RECEIVE PATH BLOCK DIAGRAM



3.1 Receive Line Interface

Physical Layer devices are AC coupled to a line interface through a 1:1 transformer. The transformer provides isolation and a level shift by blocking the DC offset of the incoming data stream. The typical medium for the line interface is a 75Ω coxial cable. Whether using E3, DS-3 or STS-1, the LIU requires the same bill of materials, see Figure 6.

FIGURE 6. RECEIVE LINE INTERFACECONNECTION



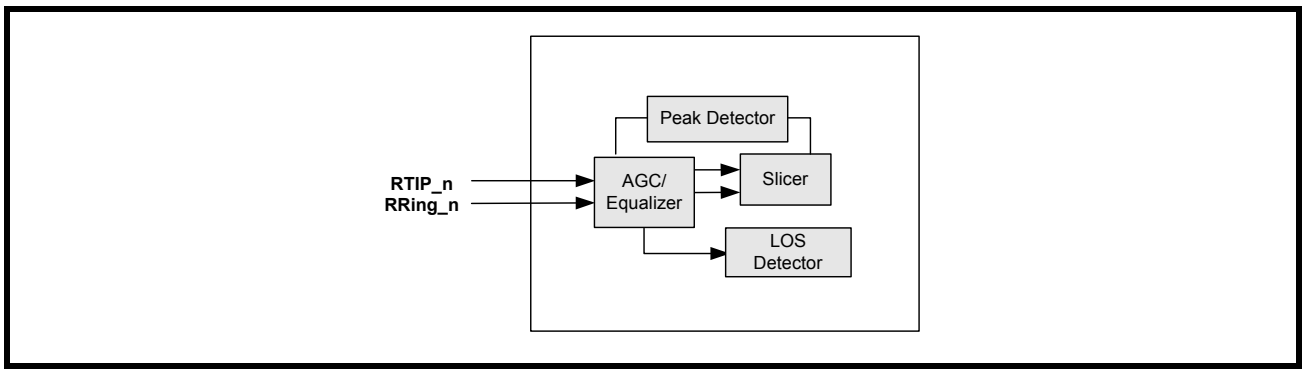
3.2 Adaptive Gain Control (AGC)

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB. The peak detector provides feedback to the equalizer before slicing occurs.

3.3 Receive Equalizer

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data. The equalizer can be disabled by programming the appropriate register.

FIGURE 7. ACG/EQUALIZER BLOCK DIAGRAM



3.3.1 Recommendations for Equalizer Settings

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be enabled. However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be disabled for cable length less than 300 feet. This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics. The Equalizer also contains an additional 20 dB gain stage to provide the line monitoring capability (Receive Monitor Mode) of the resistively attenuated signals which may have 20dB flat loss. The equalizer and the equalizer gain mode can be enabled by programming the appropriate register. However, enabling the equalizer gain mode (Receive Monitor Mode) suppresses the internal LOS circuitry and LOS will never assert nor LOS be declared when operating with Receive Monitor Mode enabled.

NOTE: The results of extensive testing indicate that even when the Equalizer was enabled, regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.

3.4 Clock and Data Recovery

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder. The Clock Recovery PLL can be in one of the following two modes:

3.4.1 Data/Clock Recovery Mode

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

3.4.2 Training Mode

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin “High” or setting the RLOL_n bit to “1” in the control register. Also, the clock output on the RxClk_n pins are the same as the reference channel clock.

3.5 LOS (Loss of Signal) Detector

3.5.1 DS3/STS-1 LOS Condition

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to “1” in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses. Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 3.The status of the ALOS condition is reflected in the ALOS_n status control register. RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled “High” and the RLOS_n bit is set to “1” in the status control register.