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GENERAL DESCRIPTION

The XRT75VL00 is a single-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/STS-1 applications. It incorporates an independent Receiver, Transmitter and Jitter Attenuator in a single 52 pin TQFP package.

The XRT75VL00 can be configured to operate in either E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) modes. The transmitter can be turned off (tri-stated) for redundancy support and for conserving power.

The XRT75VL00's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75VL00 incorporates an advanced crystal-less jitter attenuator that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

The XRT75VL00 provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75VL00 supports local, remote and digital loop-backs. The XRT75VL00 also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES

RECEIVER:

- On chip Clock and Data Recovery circuit for high input jitter tolerance.
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements.
- Detects and Clears LOS as per G.775.
- Meets Bellcore GR-499 CORE Jitter Transfer Requirements.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation.
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards.
- Meets ETSI TBR 24 Jitter Transfer Requirements.
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled.
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock.
- Provides low jitter output clock.

TRANSMITTER:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Transmitter can be turned on or off.

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator.
- Jitter Attenuator can be selected in Receive or Transmit paths.
- 16 or 32 bits selectable FIFO size.
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards.
- Jitter Attenuator can be disabled.

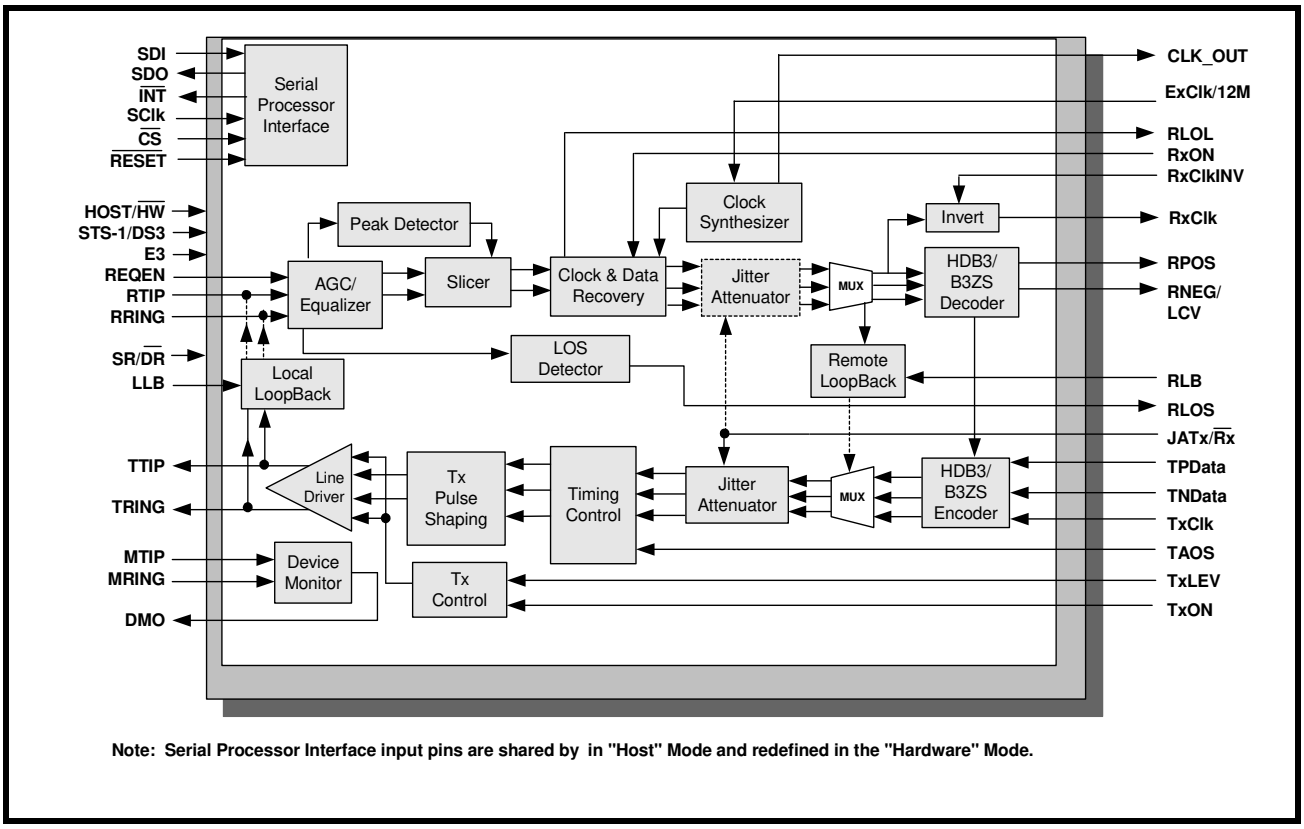
CONTROL AND DIAGNOSTICS:

- 5 wire Serial Microprocessor Interface for control and configuration.
- Supports optional internal Transmit Driver Monitoring.
- PRBS error counter register to accumulate errors.
- Hardware Mode for control and configuration.
- Supports Local, Remote and Digital Loop-backs.
- Single 3.3 V ± 5% power supply.
- 5 V Tolerant I/O.
- Available in 52 pin TQFP.
- -40℃ to 85℃ Industrial Temperature Range.

APPLICATIONS

- E3/DS3 Access Equipment.
- DSLAMs.
- Digital Cross Connect Systems.
- CSU/DSU Equipment.
- Routers.
- Fiber Optic Terminals.

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75VL00



Note: Serial Processor Interface input pins are shared by in "Host" Mode and redefined in the "Hardware" Mode.

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit.
- Built-in B3ZS/HDB3 Encoder (which can be disabled).
- Accepts Transmit Clock with duty cycle of 30%-70%.
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications.
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993.
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE.
- Transmitter can be turned off in order to support redundancy designs.

RECEIVE INTERFACE CHARACTERISTICS

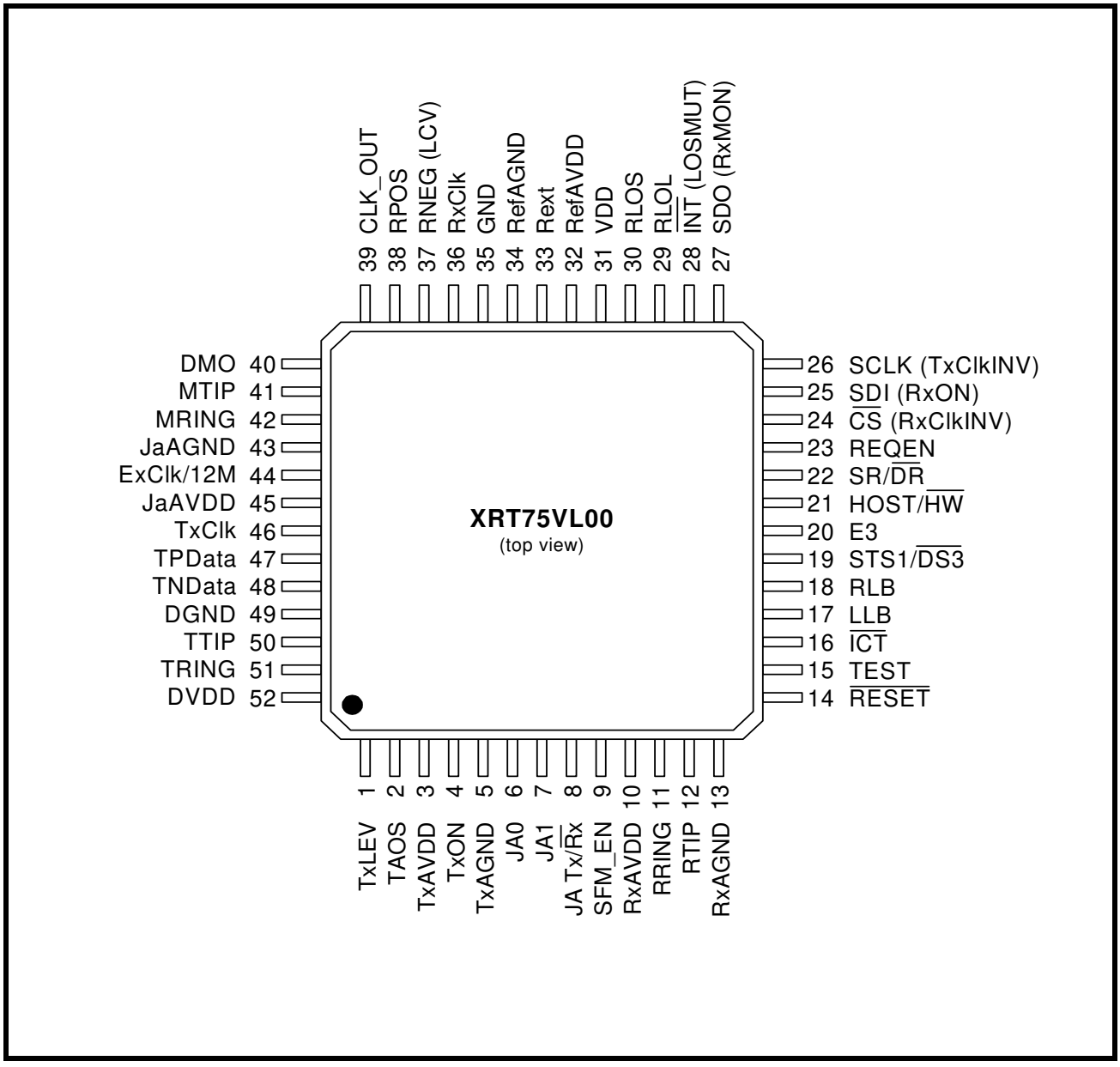
- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery.
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications.
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications.
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications.
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms.
- Built-in B3ZS/HDB3 Decoder (which can be disabled).
- Recovered Data can be muted while the LOS Condition is declared.

- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment.

JITTER ATTENUATORS

The XRT75VL00 includes a Jitter Attenuator that meets the Jitter requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards. In addition, the jitter attenuator also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards.

FIGURE 2. PIN OUT OF THE XRT75VL00



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75VL00IV	52 Pin TQFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
4	TxON	I	**Transmitter ON Input** Setting this input pin "High" turns on the Transmitter. ***NOTES:*** 1. *Even when the XRT75VL00 is configured in HOST mode, this pin still controls the TTIP and TRING outputs* 2. *When the Transmitter is turned off either in Host or Hardware mode,the TTIP and TRING outputs are Tri-stated.* 3. *This pin is internally pulled down*
46	TxClk	I	**Transmit Clock Input for TPData and TNData** The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%. The XRT75VL00 samples the TPData and TNData pins on the falling or rising edge of TxClk signal based on the status of TxClkINV pin (in Hardware mode) or the status of the bit in the Channel Register (in HOST mode).
26	TxClkINV/ SClk	I	**Transmit Clock Invert or Serial Clock Input:** Function of this depends on whether the XRT75VL00 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin “High” configures the Transmitter to sample the TPData and TNData data on the rising edge of the TxClk. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as SClk input pin (please refer to the pin description for Microprocessor interface).*
48	TNData	I	**Transmit Negative Data Input** If the XRT75VL00 is configured in Dual-rail mode, this pin is sampled on the falling or rising edge of TxClk based on the status of the TClkINV pin (in Hardware mode) or the status of the control bit in the Channel Register (in HOST mode). ***NOTES:*** 1. *This input pin is ignored and should be tied to GND if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.*
47	TPData	I	**Transmit Positive Data Input** The XRT75VL00 samples this pin on the falling or rising edge of TxClk based on the status of the TClkINV pin (in Hardware mode) or the status of the control bit in the Channel Register (in HOST mode).
50	TTIP	O	**Transmit TTIP Output** The XRT75VL00 uses this pin along with TRING to transmit a bipolar signal to the line using a 1:1 transformer.

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
51	TRING	O	**Transmit Ring Output** The XRT75VL00 uses this pin along with TTIP to transmit a bipolar signal to the line using a 1:1 transformer.
1	TxLEV	I	**Transmit Line Build-Out Enable/Disable Select** This input pin is used to enable or disable the Transmit Line Build-Out circuit. Setting this pin to "High" disables the Line Build-Out circuit. In this mode, partially-shaped pulses are output onto the line via the TTIP and TRING output pins. Setting this pin to "Low" enables the Line Build-Out circuit. In this mode, shaped pulses are output onto the line via the TTIPand TRING output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set this pin to "1" if the cable length between the Cross-Connect and the transmit output is greater than 225 feet. 2. Set this pin to "0" if the cable length between the Cross-Connect and the transmit output is less than 225 feet. This pin is active only if the following two conditions are true: a. The XRT75VL00 is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT75VL00 is configured to operate in the Hardware Mode. ***NOTES:*** *1. This pin is internally pulled down.* *2. If the XRT75VL00 is configured in HOST mode, this pin may be tied to GND.*

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
25	RxON/ SDI	I	**Receiver Turn ON Input or Serial Data Input:** Function of this pin depends on whether the XRT75VL00 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" turns on and enables the Receiver.. ***NOTES:*** *1. If the XRT75VL00 is configured in HOST mode, this pin functions as SDI input pin (please refer to the pin description for Microprocessor Interface)* *2. This pin is internally pulled down.*
23	REQEN	I	**Receive Equalization Enable Input** Setting this input pin "High" enables the Internal Receive Equalizer. Setting this pin "Low" disables the Internal Receive Equalizer. ***NOTES:*** *1. This input pin is ignored and may be connected to GND if the XRT75VL00 is operating in the HOST Mode* *2. This pin is internally pulled down.*
36	RxClk	O	**Receive Clock Output** The Recovered Clock signal from the incoming line signal is output through this pin.By default, the Receiver Section outputs data via RPOS and RNEG pins on the rising edge of this clock signal. Configure the Receiver Section to update data on the RPOS and RNEG pins on the falling edge of RxClk by doing the following: a) **Operating in Hardware mode**, pull the RxClkINV pin to "High". b) **Operating in Host mode**, write a "1" to RxClkINV bit field within the Receive Control Register.
24	RxClkINV/ $\overline{CS}$	I	**RxClk INVERT or Chip Select**: Function of this pin depends on whether the XRT75VL00 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" configures the Receiver Section to invert the RxClk output signals and outputs the recovered data via RPOS and RNEG on the falling edge of RxClk. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as CS input pin (please refer to the pin description for Microprocessor Interface).*
38	RPOS	O	**Receive Positive Data Output** This output pin pulses "High" whenever the XRT75VL00 has received a Positive Polarity pulse in the incoming line signal at the RTIP/RRing inputs.

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
37	RNEG/LCV	O	**Receive Negative Data Output/Line Code Violation Indicator** **Function of these pins depends on whether the XRT75VL00 is configured in Single Rail or Dual Rail mode.** If the XRT75VL00 is configured in Dual Rail mode, a negative pulse is output through RNEG. **In Hardware mode:** Tie the pin SR/$\overline{DR}$ (pin 22) "High" to configure the XRT75VL00 in Single Rail mode and tie "Low" to configure in Dual Rail mode. **In HOST mode:** XRT75VL00 can be configured in Single Rail or Dual Rail by setting or clearing the bit in the block control register. **Line Code Violation Indicator** If the XRT75VL00 is configured in Single Rail mode then: Whenever the Receiver Section detects a Line Code violation, it pulses this output pin "High". This output pin remains "Low" at all other times. It is advisable to sample this output pin using the RxClk output signal.
11	RRING	I	**Receive Ring Input** This input pin along with RTIP is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
12	RTIP	I	**Receive TIP Input** This input pin along with RRNG is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
27	RxMON/ SDO	I	**Receive Monitoring Mode or Serial Data Output:** In Hardware mode, when this pin is tied "High" XRT75VL00 configures into monitoring channel. In the monitoring mode, the Receiver is capable of monitoring the signals with 20 dB flat loss plus 6 dB cable attenuation. This allows to monitor very weak signal before declaring LOS. In HOST Mode, XRT75VL00 can be configured to be a monitoring channel by setting the bits in the receive control register. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as SDO pin (please refer to the pin description for the Microprocessor Interface).*

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
44	ExClk/12M	I	**Clock Input (34.368 MHz or 44.736 MHz or 51.84 MHz ± 20 ppm):** Based on the mode selected, provide the appropriate reference clock signal. If the XRT75VL00 is configured for Single Frequency Mode with the SFM_EN tied "High", then provide a 12.288 MHz ± 20 ppm clock and depending on the mode, the correct frequency is generated internally by the clock synthesizer..
9	SFM_EN	I	**Single Frequency Enable:** Tie this pin "High" to select the single frequency mode. When enabled, a single frequency clock, 12.288 MHz is input through the ExClk input pin and the internal clock synthesizer generates the appropriate clock frequency. ***NOTE:*** *This pin is internally pulled down.*
39	CLK_OUT	O	**Clock out put:** When the Single Frequency Mode is selected, a low jitter clock will be out put. The frequency of this clock depends on whether the XRT75VL00 is configured in E3 or DS3 or STS-1 mode.

OPERATING MODE SELECT

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
21	HOST/($\overline{HW}$)	I	**HOST/Hardware Mode Select:** Tie this pin "High" to configure the XRT75VL00 in HOST mode. Tie this "Low" to configure in Hardware mode. When the XRT75VL00 is configured in HOST mode, the states of many discrete input pins are ignored. ***NOTE:*** *This pin is internally pulled up.*
20	E3	I	**E3 Mode Select Input** A "High" on this pin configures to operate in the E3 mode. A "Low" on this pin configures to operate in either STS-1 or DS3 mode depending on the setting on pin 19. ***NOTES:*** 1. *This pin is internally pulled down* 2. *This pin is ignored and may be tied to GND if the XRT75VL00 is configured to operate in HOST mode.*
19	STS-1/$\overline{DS3}$	I	**STS-1/DS3 Select Input** A "High" on this pin configures to operate in STS-1 mode. A "Low" on this pin configures to operate in DS3 mode. This pin is ignored if the E3 pin is set to "High". ***NOTES:*** 1. *This pin is internally pulled down* 2. *This pin is ignored and may be tied to GND if the XRT75VL00 is configured to operate in HOST mode.*
22	SR/$\overline{DR}$	I	**Single-Rail/Dual-Rail Select:** Setting this "High" configures both the Transmitter and Receiver to operate in Single-rail mode and also enables the B3ZS/HDB3 Encoder and Decoder. In Single-rail mode, Transmit input at TNData should be grounded. Setting this "Low" configures both the Transmitter and Receiver to operate in Dual-rail mode and disables the B3ZS/HDB3 Encoder and Decoder. ***NOTE:*** *This pin is internally pulled down.*

CONTROL AND ALARM INTERFACE

42	MRING	I	**Monitor Ring Input** The bipolar line output signal from TRING is connected to this pin via a 270 Ω resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled down.*
41	MTIP	I	**Monitor Tip Input** The bipolar line output signal from TTIP is connected to this pin via a 270-ohm resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled down.*
40	DMO	O	**Drive Monitor Output** If MTIP and MRING has no transition pulse for 128 ± 32 TxClk cycles, DMO goes "High" to indictae the driver failure. DMO output stays "High" until the next AMI signal is detected.

CONTROL AND ALARM INTERFACE

30	RLOS	O	**Receive Loss of Signal Output Indicator** This output pin toggles "High" if Receiver has detected a Loss of Signal Condition in the incoming line signal. The criteria for declaring/clearing an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode and is described in Section 2.04.
29	RLOL	O	**Receive Loss of Lock Output Indicator:** This output pin toggles "High" if the XRT75VL00 has detected a Loss of Lock Condition. LOL (Loss of Lock) condition is declared if the recovered clock frequency deviates from the Reference Clock frequency (available at ExClk input pin) by more than 0.5%.
33	Rext	****	**External Bias control Resistor of 3.3 KΩ ±1%.** Should be connected to RefAGND via 3.3 KΩ resistor.
15	TEST	I	**Test Mode:** Connect this pin “High” to configure the XRT75VL00 in test mode. ***NOTE:*** *This pin is internally pulled Down.*
16	$\overline{ICT}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, set this pin "High". ***NOTE:*** *This pin is internally pulled “High".*
2	TAOS	I	**Transmit All Ones Select** A “High" on this pin causes the Transmitter Section to generate and transmit a continuous AMI all “1’s” pattern onto the line. The frequency of this “1’s” pattern is determined by TxClk. ***NOTES:*** 1. *This input pin is ignored if the XRT75VL00 is operating in the HOST Mode and should be tied to GND.* 2. *Analog Loopback and Remote Loopback have priority over request.* 3. *This pin is internally pulled down.*
28	LOSMUT/ $\overline{INT}$	I/O	**MUTE-upon-LOS Enable Input or Interrupt Ouput:** In Hardware Mode, setting this pin “High” configures the XRT75VL00 to Mute the recovered data on the RPOS and RNEG whenever an LOS condition is declared. RPOS and RNEG outputs are pulled “Low”. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as $\overline{INT}$ pin (please refer to the pin description for the Microprocessor Interface).*

CONTROL AND ALARM INTERFACE

17	LLB	I	**Local Loop-back** This input pin along with RLB configures different Loop-Back modes. **RLB / LLB / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Analog Local** **1 / 0 / Remote** **1 / 1 / Digital** ***NOTE:*** *This input pin is ignored and may be connected to GND if the XRT75VL00 is operating in the HOST Mode.*
18	RLB	I	**Remote Loop-back** This input pin along with LLB configures different Loop-Back modes. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT75VL00 is operating in the HOST Mode.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
24	$\overline{CS}$/RxClkINV	I	**Microprocessor Serial Interface - Chip Select** Tie this "Low" to enable the communication with Serial Microprocessor Interface. ***NOTE:*** *If the XRT75VL00 is configured in Hardware Mode,this pin functions as RxClkINV.*
26	SCLK/TxClkINV	I	**Serial Interface Clock Input** The data on the SDI pin is sampled on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. ***NOTE:*** *If the XRT75VL00 is configured in Hardware Mode, this pin functions as TxClkINV.*
25	SDI/RxON	I	**Serial Data Input:** Data is serially input through this pin. The input data is sampled on the rising edge of the SCLK pin (pin 26). ***NOTES:*** 1. *This pin is internally pulled down* 2. *If the XRT75VL00 is configured in Hardware Mode, this pin functions as RxON.*
27	SDO/RxMON	O	**Serial Data Output:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SCLK and this pin is tri-stated upon completion of data transfer. ***NOTE:*** *If the XRT75VL00 is configured in Hardware Mode, this pin functions as RxMON.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
14	$\overline{\text{RESET}}$	I	**Register Reset:** Setting this input pin "Low" causes the XRT75VL00 to reset the contents of the Command Registers to their default settings and default operating configuration ***NOTE:*** *This pin is internally pulled up.*
28	$\overline{\text{INT}}$/LOSMUT	I/O	**INTERRUPT Output:** This pin functions as Interrupt Output for Serial Interface. A transition to “Low” indicates that an interrupt has been generated by the Serial Interface. The interrupt function can be disabled by setting the interrupt enable bit to “0” in the Channel Control Register. ***NOTE:*** *If the XRT75VL00 is in Hardware mode, this pin functions as LOSMUT.*

JITTER ATTENUATOR INTERFACE

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>JA0</td><td>I</td><td>Disable Jitter Attenuator/FIFO Size Select::
In Hardware Mode, this pin along with JA1 pin provides the following functions in the table below.
<table><tr><th>JA0</th><th>JA1</th><th>Operation</th></tr><tr><td>0</td><td>0</td><td>16 bit FIFO</td></tr><tr><td>0</td><td>1</td><td>32 bit FIFO</td></tr><tr><td>1</td><td>0</td><td>Disable Jitter Attenuator</td></tr><tr><td>1</td><td>1</td><td>Disable Jitter Attenuator</td></tr></table>
NOTE: This pin is internally pulled down.</td></tr>
<tr><td>7</td><td>JA1</td><td>I</td><td>Disable Jitter Attenuator/FIFO Size Select:
In Hardware Mode, this pin along with JA0 pin provides the functions in the table above.
NOTE: This pin is internally pulled down.</td></tr>
<tr><td>8</td><td>JA Tx/$\overline{\text{Rx}}$</td><td>I</td><td>Jitter Attenuator Select:
In Hardware Mode setting this pin “High” selects the Jitter Attenuator in the Transmit path and setting “Low” selects in Receive path.
NOTE: This pin is internally pulled down.</td></tr>
</table>

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
3	TxAVDD	****	**Transmitter Analog VDD 3.3 V ± 5%**
10	RxAVDD	****	**Receiver Analog VDD 3.3 V ± 5%**
32	RefAVDD	****	**Reference Analog VDD 3.3 V ± 5%**
5	TxAGND	****	**Transmitter Analog GND**
13	RxAGND	****	**Receiver Analog GND**
34	RefAGND	****	**Reference Analog GND**
45	JaAVDD	****	**Jitter Attenuator Analog VDD 3.3 V ± 5%**
43	JaAGND	****	**Jitter Attenuator Analog GND**

DIGITAL POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
31	DVDD	****	**VDD 3.3 V ± 5% Receiver Digital**
35	DGND	****	**GND**
52	DVDD	****	**VDD 3.3 V ± 5% Transmitter Digital**
49	DGND	****	**GND**

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5+0.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^{0}C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^{0}C	linear airflow 0 ft./min
ThetaJA	Thermal Resistance		20	^{0}C/W	linear air flow 0ft/min
ThetaJC			6	^{0}C/W	
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating		2000	V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*

TABLE 2: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current (Measured while transmitting and receiving all 1's)	65	120	175	mA
P_{DD}	Power Dissipation	210	395	610	mW
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, I_{OUT} = - 4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs and outputs are TTL 5V compliant.*

2.0 TIMING CHARACTERISTICS

FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75VL00 (DUAL-RAIL DATA)

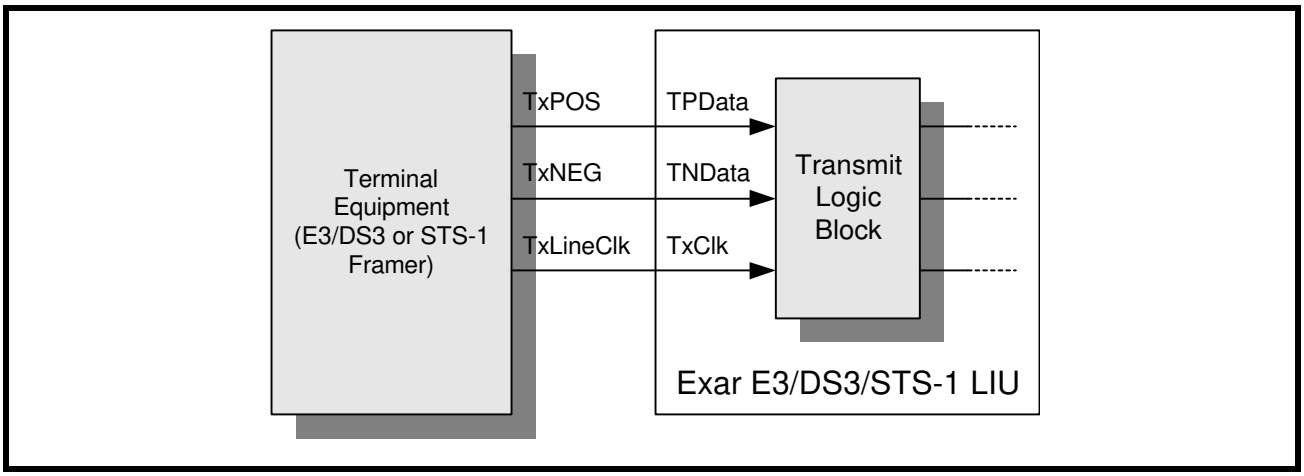
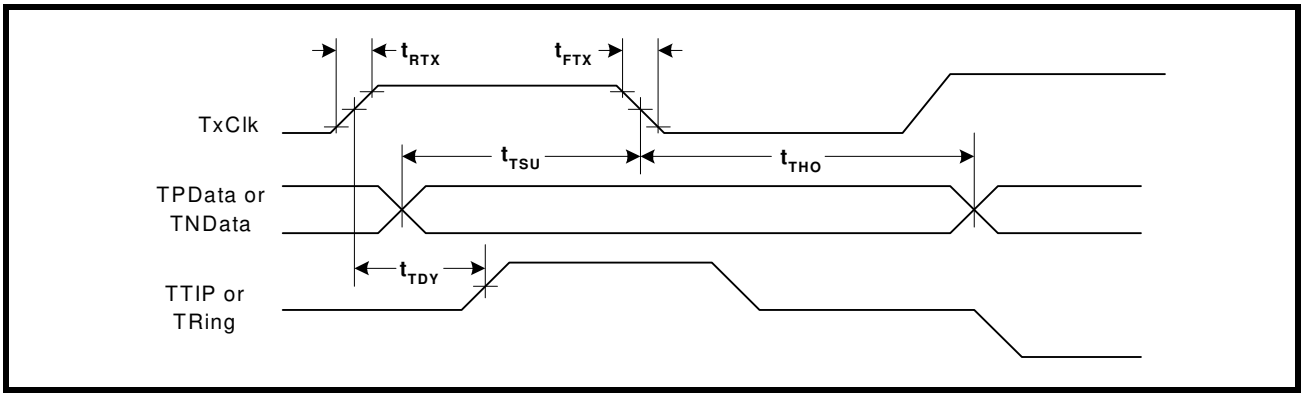
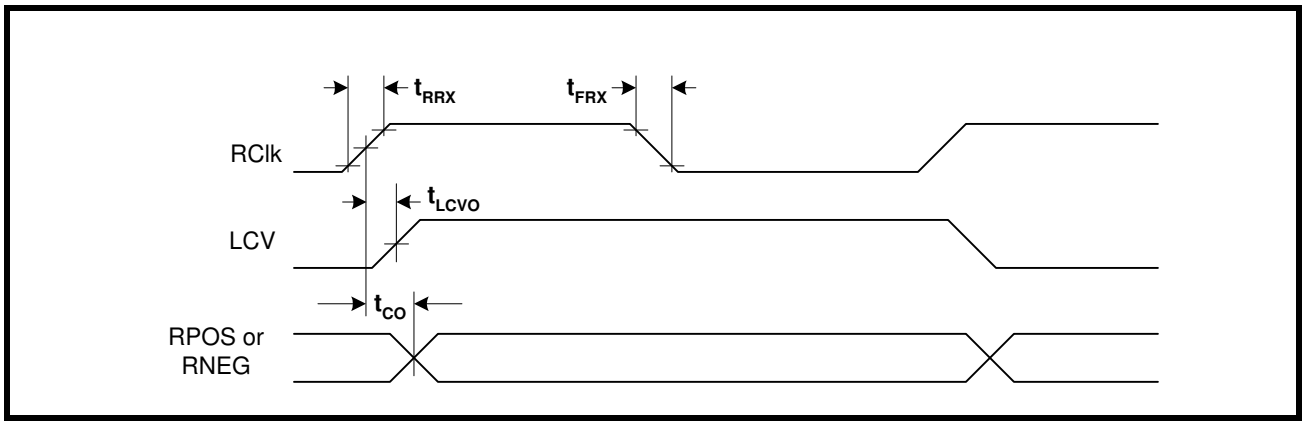


FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING



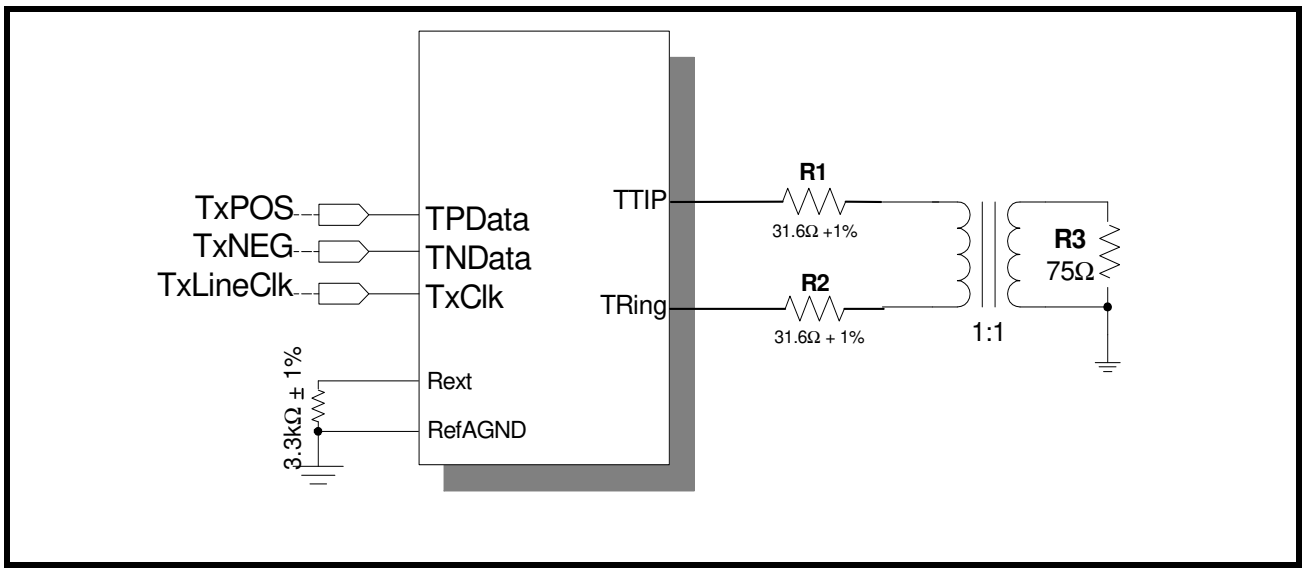
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle E3 DS3 STS-1	30	50 34.368 44.736 51.84	70	% MHz MHz MHz
t_{RTX}	TxClk Rise Time (10% to 90%)			4	ns
t_{FTX}	TxClk Fall Time (10% to 90%)			4	ns
t_{TSU}	TPData/TNData to TxClk falling set up time	3			ns
t_{THO}	TPData/TNData to TxClk falling hold time	3			ns
t_{TDY}	TTIP/TRing to TxClk rising propagation delay time		8		ns

FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle E3 DS3 STS-1	45	50 34.368 44.736 51.84	55	% MHz MHz MHz
t_{RRX}	RxClk rise time (10% o 90%)		2	4	ns
t_{FRX}	RxClk falling time (10% to 90%)		2	4	ns
t_{CO}	RxClk to RPOS/RNEG delay time			4	ns
t_{LCVO}	RxClk to rising edge of LCV output delay		2.5		ns

FIGURE 6. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES



3.0 LINE SIDE CHARACTERISTICS:

3.1 E3 line side parameters:

The XRT75VL00 meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation at the secondary of the transformer. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

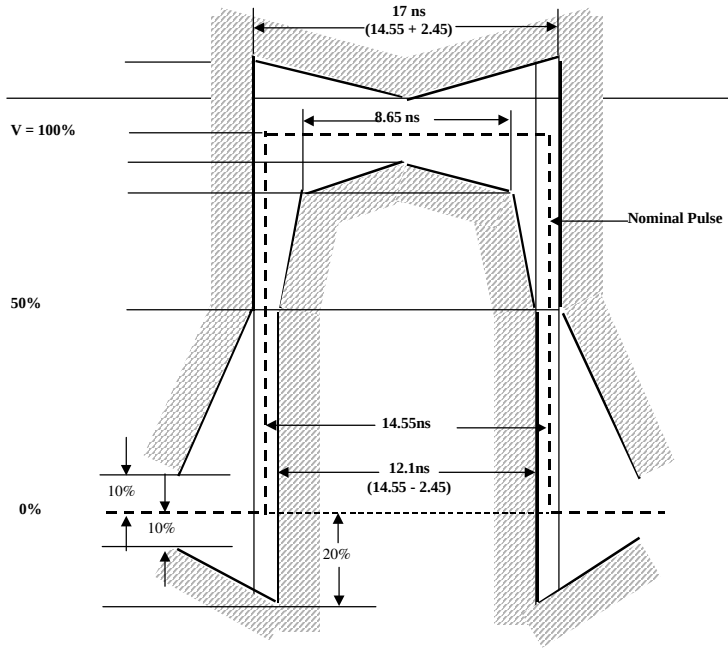


TABLE 3: E3 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS (T_A = 25^{0}C AND VDD = 3.3 V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Intrinsic Jitter		0.02	0.05	UI_{PP}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)		1200		feet
Interference Margin	-20	-15		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

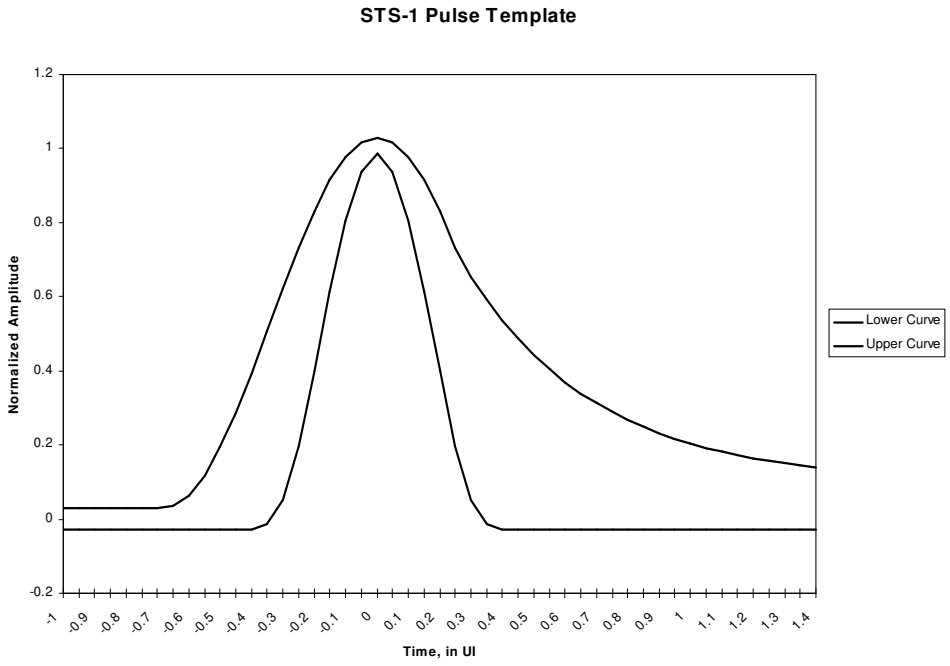


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \text{ x } e^{-2.4[T-0.26]}$

TABLE 5: STS-1 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS (TA = 25^{0}C AND VDD =3.3V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.90	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15	0.60		UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

FIGURE 9. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

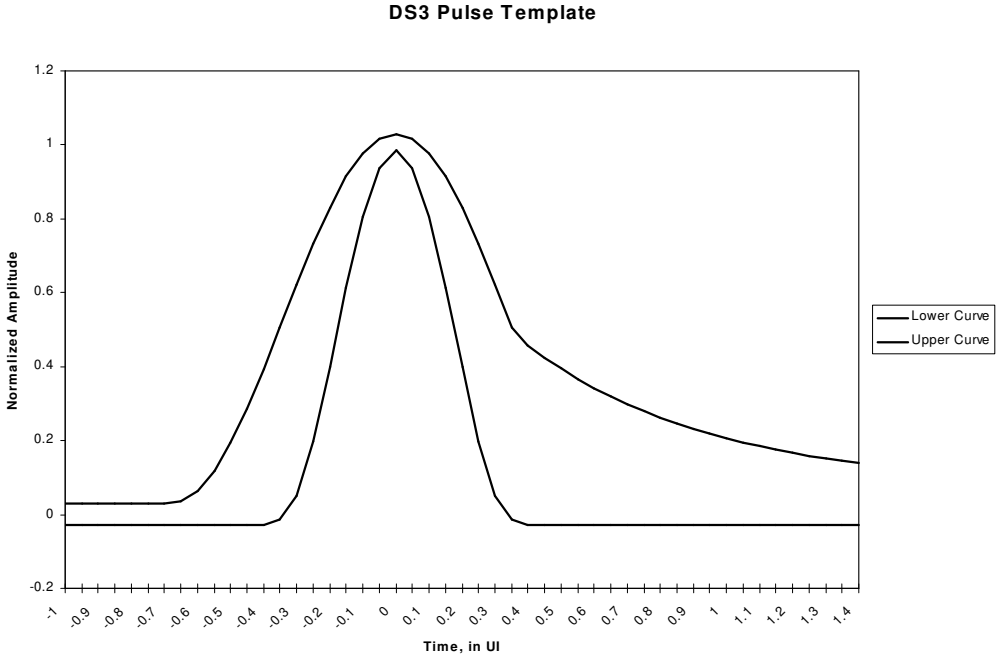


TABLE 6: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS ($T_A = 25^0C$ AND VDD = 3.3V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15	0.60		UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

FIGURE 10. MICROPROCESSOR SERIAL INTERFACE STRUCTURE

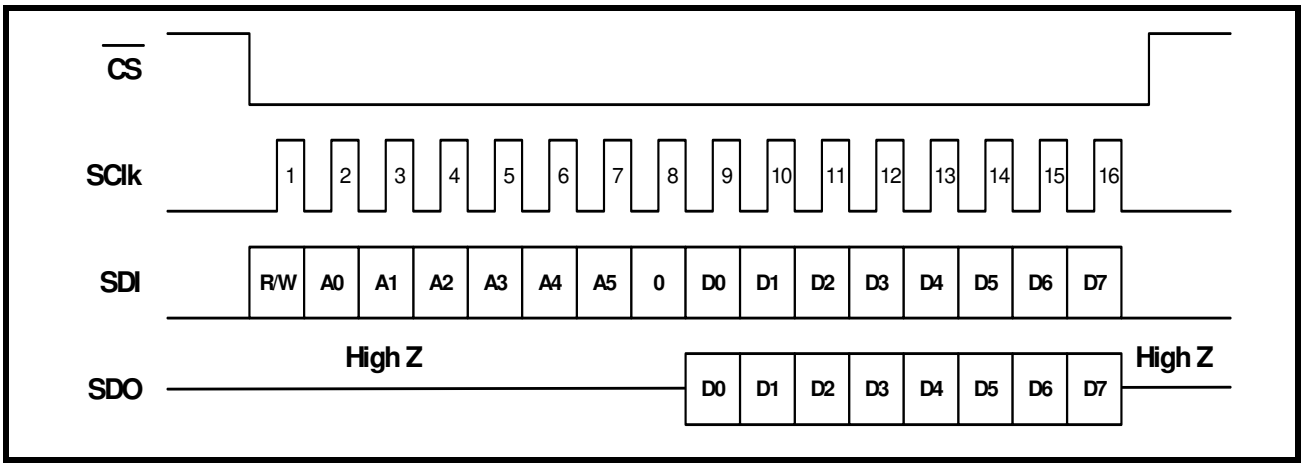


FIGURE 11. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

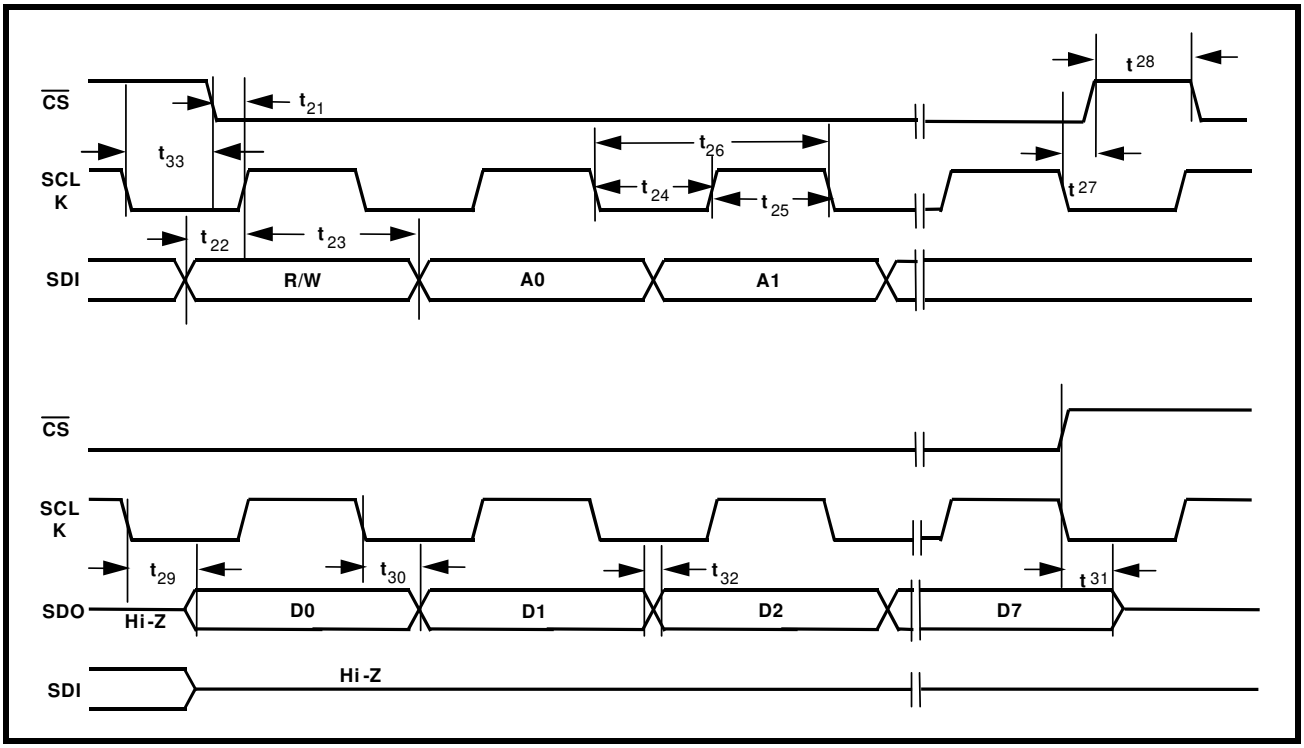


TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS (T_A = 25^{0}C, V_{DD}=3.3V± 5% AND LOAD = 10PF)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time		25		ns
t_{25}	SClk "High" Time		25		ns
t_{26}	SClk Period		50		ns
t_{27}	Falling Edge of SClk to rising edge of $\overline{CS}$	0			ns
t_{28}	$\overline{CS}$ "Inactive" Time	50			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			20	ns
t_{30}	Falling Edge of SClk to SDO Invalid Time			10	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z		10		ns
t_{32}	Rise/Fall time of SDO Output			5	ns
t_{33}	SCLK Falling Edge to $\overline{CS}$ Low Assertion Time	5			ns