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GENERAL DESCRIPTION

The XRT79L71 is a single channel, integrated DS3/E3 framing controller and Line Interface Unit with Jitter Attenuator that is designed to support Frame processing. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT79L71 includes DS3/E3 Framing, Line Interface Unit with Jitter Attenuator that supports mapping of HDLC framed data. A flexible parallel microprocessor interface is provided for configuration and control.

GENERAL FEATURES:

- Integrated T3/E3 Line Interface Unit
- Integrated Jitter Attenuator that can be selected either in Receive or Transmit path
- HDLC Controller that provides the mapping/extraction of either bit or byte mapped encapsulated packet from DS3/E3 Frame.
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing.
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola, PowerPC, and Mips µPs
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 208 STBGA Package
- JTAG Interface

LINE INTERFACE UNIT

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3 Jitter Tolerance Requirements
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets ETSI TBR 24 and GR-499 Jitter Transfer Requirements
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- On chip advanced crystal-less Jitter Attenuator
- Jitter Attenuator can be selected in Receive or Transmit paths
- 16 or 32 bits selectable FIFO size
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards
- Jitter Attenuator can be disabled
- Typical power consumption 1.3W

DS3/E3 FRAMER

- DS3 framer supports both M13 and C-bit parity.
- DS3 framer meets ANSI T1.107 and T1.404 standards.
- Detects OOF,LOF,AIS,RDI/FERF alarms.
- Generation and Insertion of FEBE on received parity errors supported.
- Automatic insertion of RDI/FERF on alarm status.
- E3 framer meets G.832,G.751 standards.
- Framers can be bypassed.
- Maps HDLC data stream directly into DS3 or E3 frame
- Extracts in-band messaging packets
- Supports CRC-16/32, HDLC flag and Idle sequence generation

RECEIVE PACKET PROCESSING

- Extracts HDLC data stream from DS3 or E3 frame
- Inserts in-band messaging packets
- Detects and removes HDLC flags

SERIAL INTERFACE

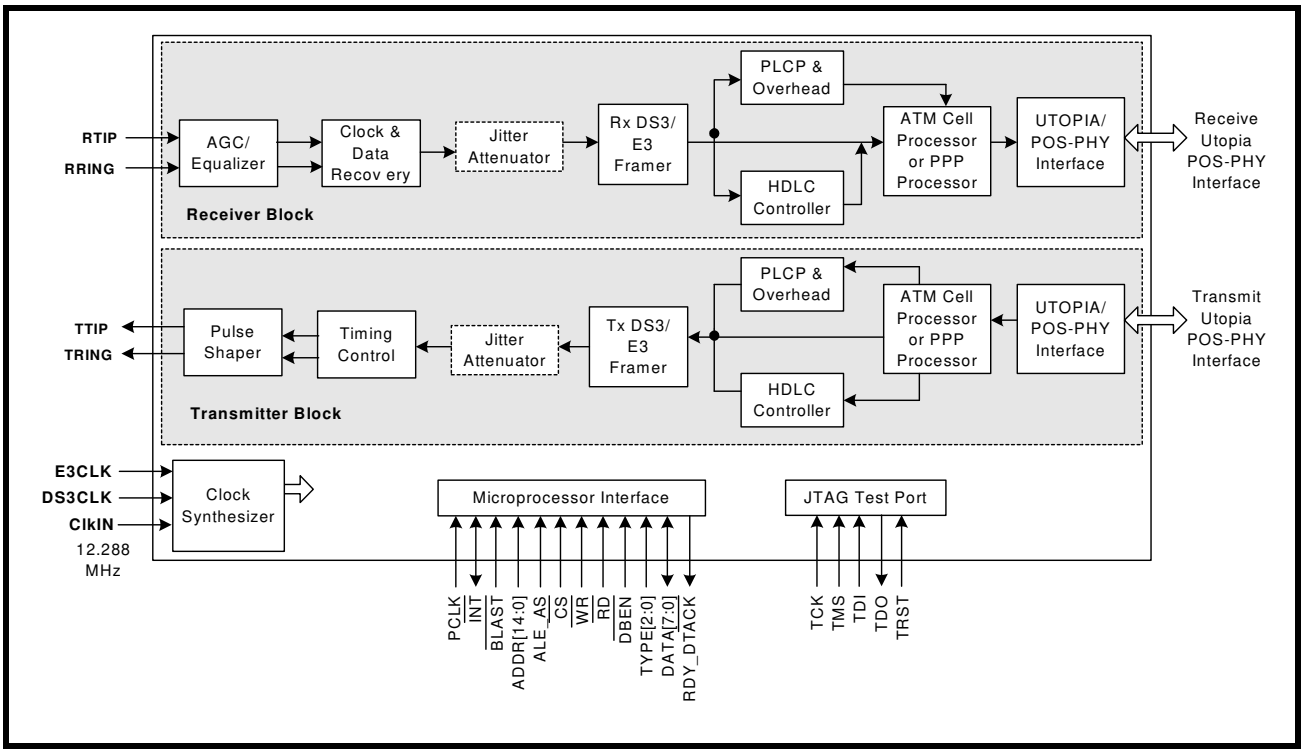
- Serial clock and data interface for accessing DS3/E3 framer

- Serial clock and data interface for accessing cell/packet processor

APPLICATIONS

- Digital Access and Cross Connect Systems
- 3G Base Stations
- DSLAMs

FIGURE 1. BLOCK DIAGRAM OF THE XRT79L71



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L71IB	17X17 mm 208 Ball Shrink Thin Ball Grid Array	-40°C to +85°C

TABLE 1: PIN OUT OF THE XRT79L71 (TOP VIEW)

	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	TXUADDR_1	TXUADDR_3	TXUCLKO	TXPEOP	TXUCLK	RXMOD	RXUADDR_4	RXUADDR_0	RXUCLAV	RXUADDR_1	RXUDATA_2	RXUDATA_5	RXUDATA_9	RXUDATA_13	RXGFCMSB	RXGFCCLK
2	TXUADDR_0	TXUADDR_2	TXUADDR_4	RXPDVAL	TXPER	RXPERR	RXUCLKO	RXUADDR_1	RXUSOC	RXUADDR_0	RXUDATA_4	RXUDATA_8	RXUDATA_12	TXGFCCLK	RXPRED	RXPLOF
3	TXUDATA_0	TXUPRTY	TXUSOC	TXUCLAV	TXMOD	RXUCLK	RXPEOP	RXUADDR_2	RXUPRTY	RXUDATA_3	RXUDATA_7	RXUDATA_11	RXUDATA_15	RXGFC	TXPOHCLK	TXPOHFRAME
4	TXUDAT_3	TXUDATA_2	TXUDATA_1	TXUDATA_10	TXUEN_L	TSX_TSOF	RSX_RSOF	RXUADDR_3	RXUEN_L	RXUDATA_6	RXUDATA_10	RXUDATA_14	RXGP	RXPOHFRAME	RXNIB_3	RXNIB_2
5	TXUDATA_7	TXUDATA_6	TXUDATA_5	TXUDATA_4									RXPOOF	RXNIB_0	RXOUTCLK	RXSER
6	TXUDATA_12	TXUDATA_11	TXUDATA_9	TXUDATA_8									RXNIB_1	RXOHIND	RXFRAME	RXCLK
7	GPIO_0	TXUDATA_15	TXUDATA_14	TXUDATA_13									RXLOS	RXOH	RXOHENABLE	RXOHCLK
8	DMO_0	GPIO_3	GPIO_2	GPIO_1									TXNIB_1	TXNOB_2	TXNOB_3	RXOHFRAME
9	TCK	TMS	TDI	TDO									TXNIBCLK	TXSER	TXOHIND	TXNIB_0
10	TRING	TRST	MTIP	TXDGND									TXOHINS	TXINCLK	TXFRAME	TXNIBFRAME
11	TTIP	NC	MRING	TXDVDD									PDATA	TXOH	TXOHFRAME	TXFRAMEREF
12	TXAVDD	REFAVDD	REFAGND	TXAGND									PDATA_4	PDATA_1	TXOHCLK	TXOHENABLE
13	RXAVDD	RRING	ANAIO1	OVDD	OGND	GPI_2	GPO_2	PDBEN_L	DA_SEL	DPADDR_7	DPADDR_3	PADDR_6	PINT_L	PDATA_5	PDATA_2	TXAISEN
14	RXAGND	RTIP	ANAIO2	VDD	RESET_L	GPI_1	GPO_1	PTYPE_2	VDD	DPADDR_6	DPADDR_2	PADDR_5	PCS_L	PRDY_L	PDATA_6	PDATA_3
15	JAGND	TXON	ICTB	GND	TESTMODE	GPI_0	GPO_0	PTYPE_1	GND	DPADDR_5	DPADDR_1	PADDR_4	PADDR_1	PRD_L	PBLAST_L	PDATA_7
16	JAAVDD	CLKVDD	DS3CLK	CLKGND	E3CLK	NIBBLEINTF	CLKOUT	PTYPE_0	PCLK	DPADDR_4	DPADDR_0	PADDR_3	PADDR_2	PADDR_0	PWR_L	PAS_L

VDD	GND	GND	VDD	G
VDD	GND	GND	VDD	G
VDD	GND	GND	VDD	G
VDD	GND	GND	VDD	G

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1.0 BRIEF XRT79L71 ARCHITECTURE DESCRIPTION

The XRT79L71 can be configured to operate in any of the following modes.

- The Clear-Channel DS3/E3 Framer Mode
- The High-Speed HDLC Controller over DS3/E3 Mode
- The ATM UNI over DS3/E3 Mode
- The PPP over DS3/E3 Mode

The detailed functional description of the XRT79L71, that covers these four modes of operation, can be found in various documents as presented below in Table 2.

TABLE 2: LISTING OF ARCHITECTURAL/FUNCTIONAL DESCRIPTION DOCUMENTS FOR THE XRT79L71

MODE OF OPERATION	ARCHITECTURAL/FUNCTIONAL DESCRIPTION DOCUMENT
DS3/E3 Clear-Channel Framer Mode	**79L71_Arch_Descr_CC.pdf** Architectural/Functional Description of the XRT79L71, 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel with LIU, IC - Clear-Channel Framer Applications
DS3/E3 High-Speed HDLC Controller Mode	**79L71_Arch_Descr_HDLC.pdf -** Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel with LIU IC - High-Speed HDLC Controller Mode Applications
DS3/E3 ATM UNI Mode	**79L71_Arch_Descr_ATM.pdf** Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel Framer with LIU IC - ATM UNI Mode Applications
DS3/E3 PPP Mode	**79L71_Arch_Descr_PPP.pdf** Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel Framer with LIU IC - PPP Mode Applications

If the XRT79L71 is to be operated in a particular mode, obtain the appropriate document, which is presented in Table 2. However, a brief functional/architectural description of the XRT79L71, when it is configured to operate in any of these modes will be presented below.

1.1 BRIEF FUNCTIONAL ARCHITECTURE DESCRIPTION OF THE XRT79L71 - CLEAR-CHANNEL DS3/E3 FRAMER MODE

If the XRT79L71 has been configured to operate in the Clear-Channel DS3/E3 Framer Mode, then it will have the Functional Architecture as is presented below in Figure 2.

FIGURE 2. THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT79L71 WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE CLEAR-CHANNEL DS3/E3 FRAMER MODE

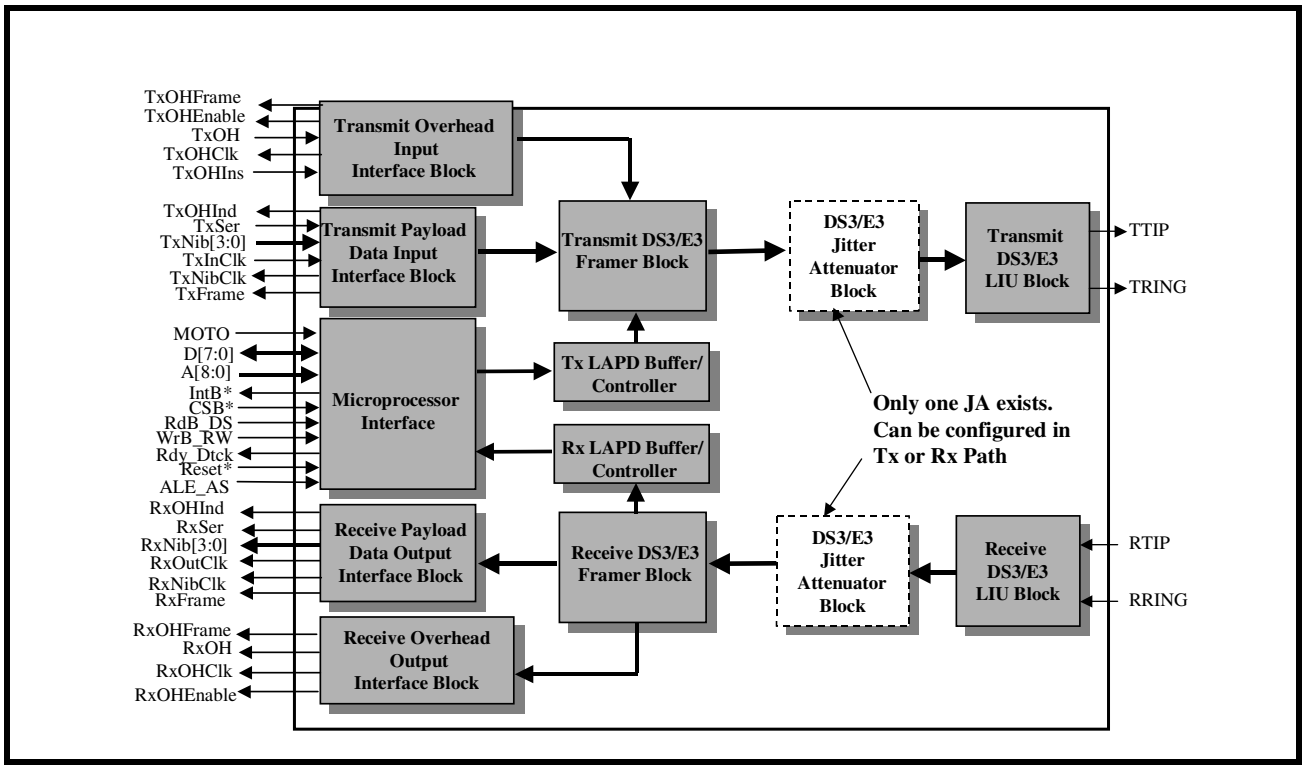

Figure 2 indicates that the XRT79L71 consists of the following functional blocks.

- The Transmit Payload Data Input Interface Block
- The Transmit Overhead Data Input Interface Block
- The Transmit LAPD Controller Block
- The Transmit FEAC Controller Block (DS3, C-bit Parity Applications Only)
- The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)
- The Transmit SSM Controller Block (E3, ITU-T G.832 Applications Only)
- The Transmit DS3/E3 Framer Block
- The Transmit DS3/E3 LIU Block
- The Receive DS3/E3 LIU Block
- The Receive DS3/E3 Framer Block
- The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)
- The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)
- The Receive FEAC Controller Block (DS3, C-bit Parity Applications Only)
- The Receive LAPD Controller Block
- The Receive Payload Data Output Interface Block
- The Receive Overhead Data Output Interface Block

Each of these functional blocks is briefly discussed below. These functional blocks will be discussed in considerable detail throughout this data sheet.

1.1.1 The Transmit Payload Data Input Interface Block

The purpose of the Transmit Payload Data Input Interface block is to accept outbound payload data either via a Serial or Nibble-Parallel interface, and to route this data to the Transmit DS3/E3 Framer block (where this data will ultimately be mapped into the payload bit-positions within each outbound DS3/E3 frame).

1.1.2 The Transmit Overhead Data Input Interface Block

The purpose of the Transmit Overhead Data Input Interface block is to permit the user to externally insert the users own value for overhead bits into the outbound DS3/E3 data-stream.

NOTE: *This particular feature is very valuable in those applications in which the XRT79L71 is processing a Channelized DS3 signal that is of the M23-framing format (where it is imperative to preserve the contents of the C-bits within the DS3 data-stream).*

1.1.3 The Transmit LAPD Controller Block

The purpose of the Transmit LAPD Controller block is to permit the user to transmit LAPD/PMDL (Path Maintenance Data Link) Messages to the remote terminal equipment. The Transmit LAPD Controller block comes with a LAPD Controller/Transmitter and 90 bytes of on-chip RAM (for storage of outbound PMDL Messages), prior to transmission.

1.1.4 The Transmit FEAC Controller Block (for DS3, C-Bit Parity Applications only)

The purpose of the Transmit FEAC Controller block is to permit the user to transmit FEAC (Far-End Alarm & Control) Messages to the remote terminal equipment.

NOTE: *The Transmit FEAC Controller Block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.*

1.1.5 The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)

The purpose of the Transmit Trail-Trace Message Controller block is to permit a given terminal equipment to repeatedly transmit a "Trail-Trace" Message to the remote terminal equipment, via the TR bytes within each outbound E3, ITU-T G.832 frame

1.1.6 The Transmit SSM Controller Block (E3, ITU-T G.832 Applications Only)

The purpose of the Transmit SSM Controller block is to permit a given terminal equipment to repeatedly transmit the "Synchronization Status Message" to the remote terminal equipment, via the MA byte, within each outbound E3, ITU-T G.832 frame.

1.1.7 The Transmit DS3/E3 Framer Block

The purpose of the Transmit DS3/E3 Framer block is to accept data from the Transmit Payload Data Input Interface block, and Transmit Overhead Data Input Interface, the Transmit LAPD Controller and the Transmit FEAC Controller block and to construct a DS3/E3 data-stream for transmission to the remote terminal equipment. Additionally, the Transmit DS3/E3 Framer block can be configured to do all of the following.

- To transmit the AIS Indicator (upon Software Control)
- To automatically transmit the FERF/RDI Indicator (in response to the Receive DS3/E3 Framer block declare the LOS, LOF/OOF or AIS defect condition).
- To transmit the FERF/RDI indicator (upon Software Control)
- To automatically transmit the FEBE/REI Indicator (in response to the Receive DS3/E3 Framer block detecting Framing bit or CP-bit errors - DS3, C-bit Parity Applications).
- To automatically transmit the FEBE/REI Indicator (in response to the Receive DS3/E3 Framer block detecting BIP-8 Error - E3, ITU-T G.832 Applications).
- To transmit the FEBE/REI indicator (upon Software Control).

1.1.8 The Transmit DS3/E3 LIU Block

The purpose of the Transmit DS3/E3 LIU Block is to accept the outbound DS3/E3 data-stream from the Transmit DS3/E3 Framer block, and to perform all of the following operations on this signal.

- To encode into the B3ZS Line Code (for DS3 Applications) or the HDB3 Line Code (for E3 Applications)
- To convert this outbound DS3 or E3 data into a DS3/E3 line signal and transmit this signal to the remote terminal equipment.
- To generate and transmit DS3 pulses that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE
- To generate and transmit E3 pulses that complies with the ITU-T G.703 Pulse Template requirements for E3 applications.

1.1.9 The Receive DS3/E3 LIU Block

The purpose of the Receive DS3/E3 LIU Block is to receive a DS3/E3 line signal from the remote terminal equipment, and to perform the following operations

- To decode this incoming signal from the B3ZS Line Code (for DS3 Applications) or the HDB3 Line Code (for E3 Applications) into a binary data-stream
- To route this binary data-stream to the Receive DS3/E3 Framer block for further processing
- To detect and flag the occurrence of LCVs (Line Code Violations) and EXZs (Excessive Zeros)
- To insure that the XRT79L71 meets all of the following Receive requirements.
  - **a.** The Receive Sensitivity requirements for DS3 Applications (e.g., able to receive a DSX-3 type of signal through at least 450 feet of cable loss)
  - **b.** The Receive Sensitivity requirements for E3 Applications (e.g., able to receive an E3 signal over 12dB of cable loss)
  - **c.** To comply with the Category I and II Jitter Tolerance Requirements per Bellcore GR-499-CORE (for DS3 Applications)
  - **d.** To comply with the Jitter Tolerance Requirements per ITU-T G.832 (for E3 Applications)
  - **e.** To comply with the Interference Margin Requirements of 20dB, per ITU-T G.703 (for E3 Applications)

1.1.10 The Receive DS3/E3 Framer Block

The purpose of the Receive DS3/E3 Framer block is to acquire and maintain Frame Synchronization with the incoming DS3/E3 data-stream that is receives from the Receive DS3/E3 LIU Block. As the Receive DS3/E3 Framer block performs this task, it will also do the following.

- It will declare and clear the LOS defect condition
- It will declare and clear the LOF/OOF defect condition
- It will declare and clear the AIS defect condition
- It will declare and clear the FERF/RDI defect condition
- It will detect and flag the occurrences of P-bit, CP-bit and Framing bit errors (DS3 Applications)
- It will detect and flag the occurrence of BIP-8 Errors (E3, ITU-T G.832 Applications)
- It will detect and flag the occurrence of BIP-4 Errors (E3, ITU-T G.751 Applications)
- It will detect and flag the occurrence of FEBE/REI Events
- It will route all PMDL data to the Receive LAPD Controller block for further processing
- It will route all Overhead bits/bytes to the Receive Overhead Data Output Interface block for further processing
- It will route all DS3/E3 data to the Receive Payload Data Output Interface block.

1.1.11 The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)

The purpose of the Receive SSM Controller Block is to permit a given terminal equipment to receive (and extract out) the SSM (Synchronization Status Message) from the remote terminal equipment, via the MA byte, within each inbound E3, ITU-T G.832 frame.

1.1.12 The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)

The purpose of the Receive Trail-Trace Message Controller block is to permit a given terminal equipment to receive (and extract out) the Trail-Trace Message from the remote terminal equipment, via the TR byte, within each inbound E3, ITU-T G.832 frame.

1.1.13 The Receive FEAC Controller Block (DS3 Applications Only)

The purpose of the Receive FEAC Controller block is to permit the user to receive FEAC (Far-End Alarm & Control) Messages from the remote terminal equipment.

NOTE: *The Receive FEAC Controller Block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.*

1.1.14 The Receive LAPD Controller Block

The purpose of the Receive LAPD Controller block is to permit the user to receive LAPD/PMDL (Path Maintenance Data Link) Messages from the remote terminal equipment. The Receive LAPD Controller block comes with a Receive LAPD Controller and 90 bytes of on-chip RAM (for storage of inbound PMDL Messages) after reception.

1.1.15 The Receive Payload Data Output Interface Block

The purpose of the Receive Payload Data Output Interface block is to output payload data (within the incoming DS3 or E3 data-stream) via either a Serial or Nibble-Parallel interface, and to route this data to the off-chip System-Side Terminal Equipment.

1.1.16 The Receive Overhead Data Output Interface Block

The purpose of the Receive Overhead Data Output Interface block is to permit the user to extract out the overhead bits (within the incoming DS3/E3 data-stream) and to route this data to some off-chip System-Side Terminal Equipment circuitry.

1.1.17 A more detailed Functional/Architectural Description of the XRT79L71 when configured to operate in the Clear Channel Controller Mode, is in this document (*79L71_Arch_Descr_CC.pdf*).

(Section 7.0- Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel Framer with LIU IC - Clear Channel Applications).

1.2 BRIEF FUNCTIONAL ARCHITECTURE DESCRIPTION OF THE XRT79L71 - HIGH-SPEED HDLC CONTROLLER OVER DS3/E3 MODE

If the XRT79L71 has been configured to operate in the High-Speed HDLC Controller over DS3/E3 Mode, then it will have the Functional Architecture as is presented below in **Figure 3**.

FIGURE 3. THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT79L71 WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE HIGH-SPEED HDLC CONTROLLER OVER DS3/E3 MODE

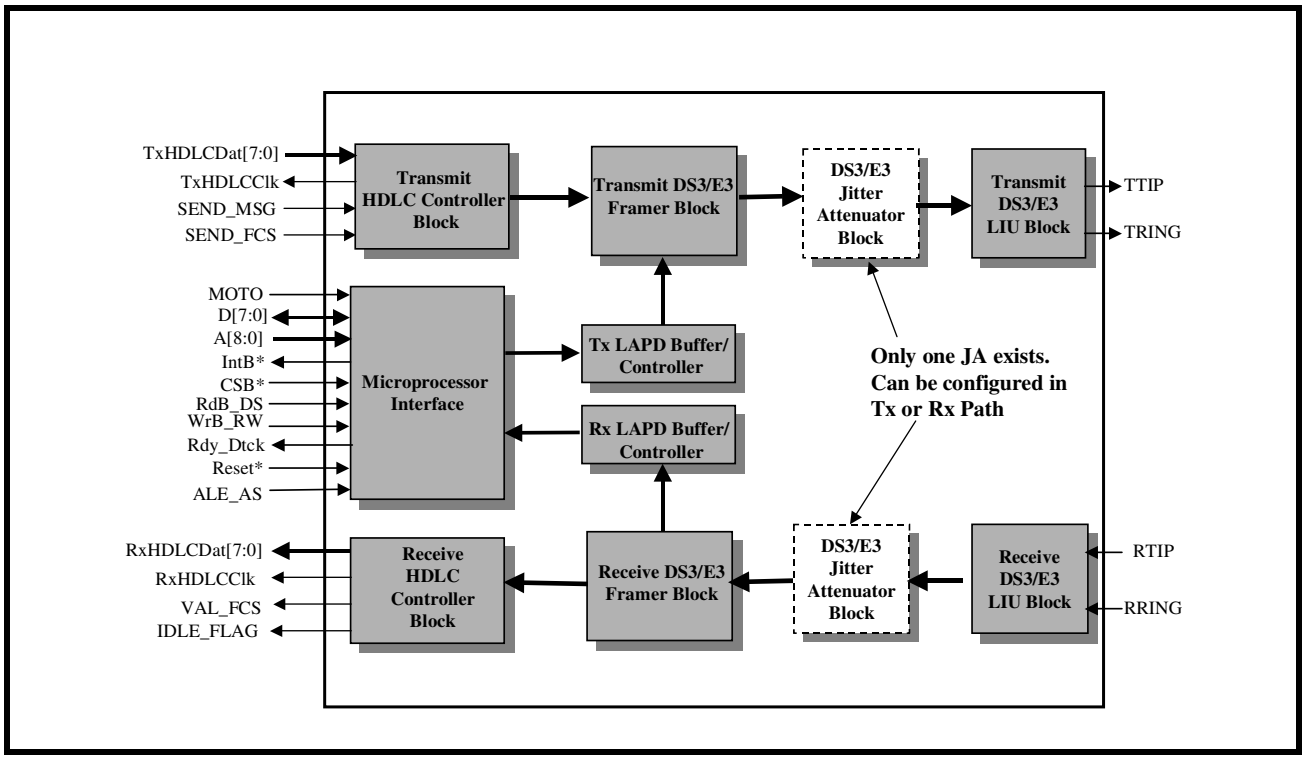

Figure 3 indicates that the XRT79L71 consists of the following functional blocks.

- The Transmit High-Speed HDLC Controller Block
- The Transmit LAPD Controller Block
- The Transmit FEAC Controller Block (DS3 Applications only)
- The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications only)
- The Transmit SSM Controller Block (E3, ITU-T G.832 Applications only)
- The Transmit DS3/E3 Framer Block
- The Transmit DS3/E3 LIU Block
- The Receive DS3/E3 LIU Block
- The Receive DS3/E3 Framer Block
- The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications only)
- The Receive SSM Controller Block (E3, ITU-T G.832 Applications only)
- The Receive FEAC Controller Block (DS3 Applications only)
- The Receive LAPD Controller Block
- The Receive High-Speed HDLC Controller Block

Each of these functional blocks is briefly discussed below. These functional blocks will also be discussed in considerable detail throughout this data sheet.

1.2.1 The Transmit High-Speed HDLC Controller Block

The purpose of the Transmit High-Speed HDLC Controller block is to perform the following tasks.