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XRT8001

WAN Clock for T1 and E1 Systems

October 2001-1

GENERAL DESCRIPTION

The XRT8001 WAN Clock is a dual-phase-locked loop chip that generates two very low jitter output clock signals that can be used for synchronization clocks in wide area networking systems. The XRT8001 has pre-programmed multipliers and dividers that are selected via the serial port. It generates two integer multiples of 8kHz, 56kHz, and 64kHz while locked onto an incoming reference of 1.54MHz (T1), 2.048MHz (E1), 8kHz, 56kHz, or 64kHz

The XRT8001 WAN Clock can be configured to operate in one of six modes:

1. The Forward/Master Mode
2. The Reverse/Master Mode
3. The “Fractional T1/E1" Reverse/Master Mode
4. The “E1 to T1 - Forward/Master" Mode
5. The “High Speed - Reverse" Mode
6. The “Slave” Mode

FEATURES

- Dual Phased Locked Loops with Pre-Programmed Multipliers and Dividers
- Pre-Programmed with Popular Frequency Conversions for Communications Systems
- Generates Output Clock Frequencies Ranging From 8kHz up to 16.384MHz
- Serial Port Control for Optimal Performance
- Sync Output: 8kHz or 64kHz
- Low Jitter
- Cascadable (Master / Slave Modes)
- No External Components Needed
- Pin Compatible with the XRT8000
- Low Power (3.3V or 5V): 40 - 100mW
- - 40°C to +85°C Temperature Range
- 18-Lead PDIP or SOIC Packages

APPLICATIONS

- T1/E1 Access Equipment (DSU/CSU)
- Frame Relay Access Devices (FRAD)
- Basic Rate and Primary Rate ISDN Equipment
  - ISDN Routers
  - Terminals
- Remote Access Servers
- T1/E1 Concentrators
- T1/E1 Multiplexers
- T1/E1 Clock Rate Converters
- Internal Timing Generators
- System Synchronizers

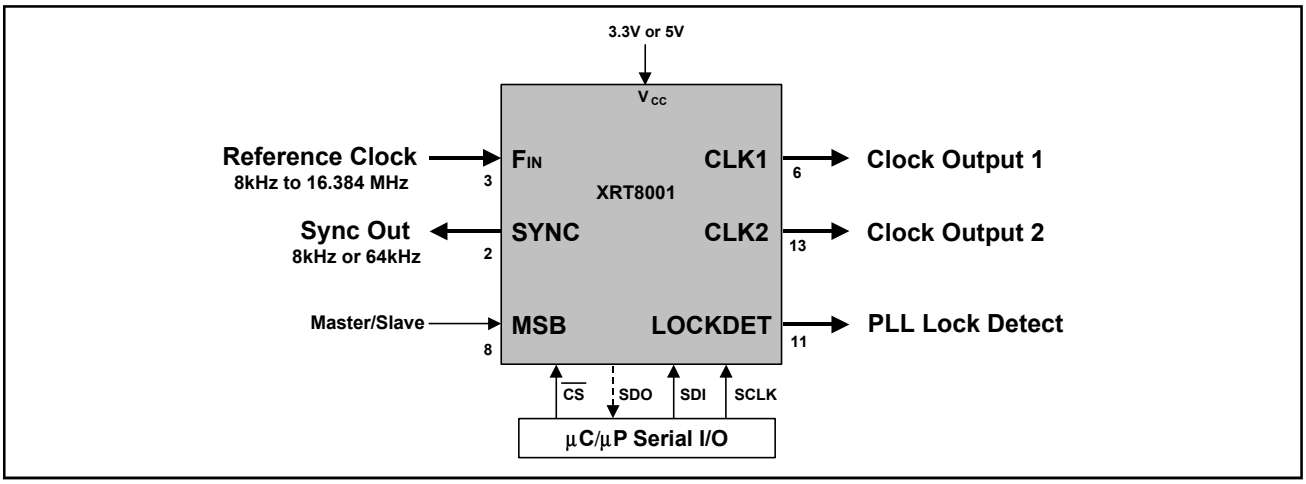


Figure 1. System Diagram

ORDERING INFORMATION

Part Number	Package	Operating Temperature Range
XRT8001IP	18-Lead 300 Mil PDIP	-40°C to +85°C
XRT8001ID	18-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 • (510) 668-7000 • FAX (510) 668-7017 • www.exar.com

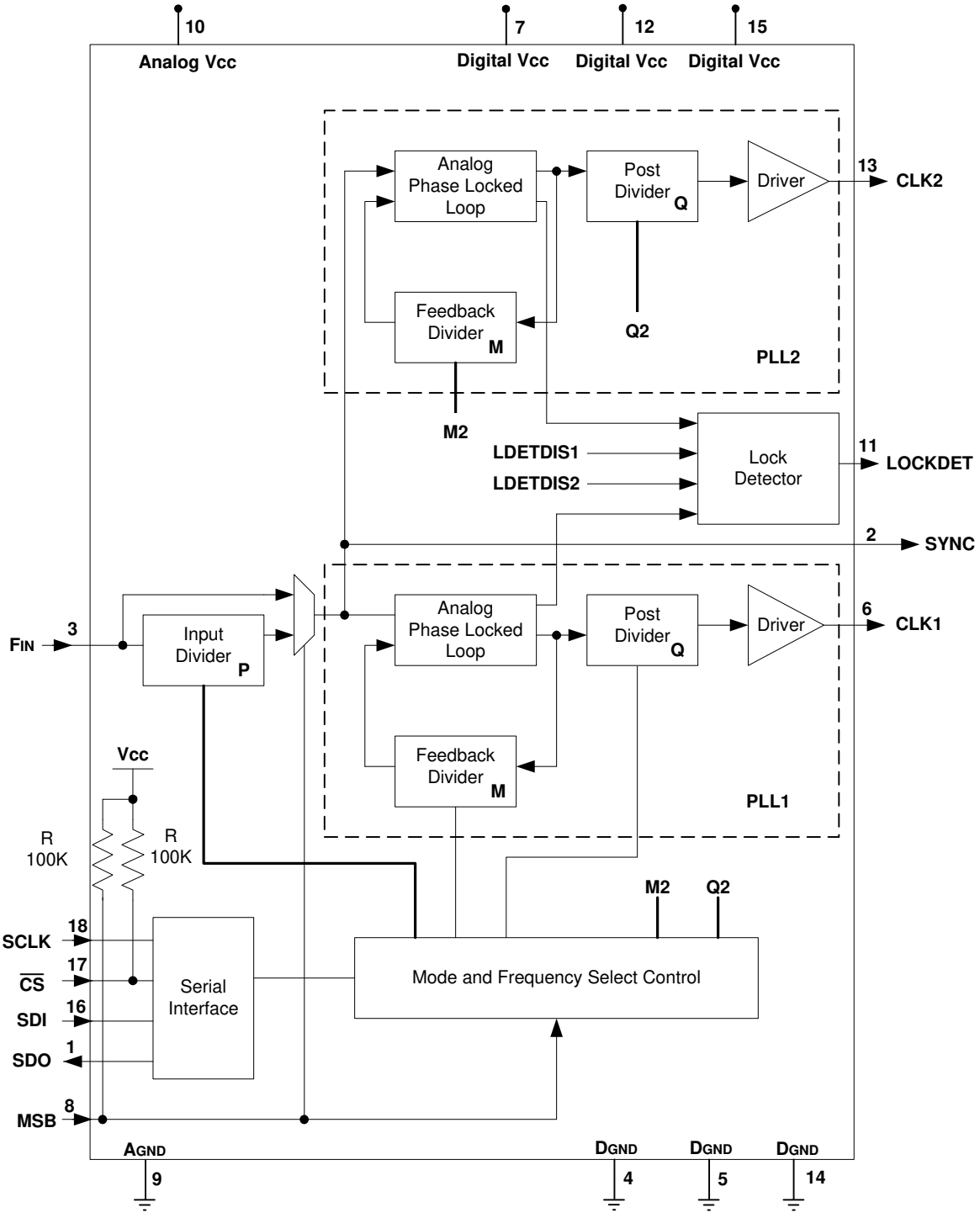


Figure 2. XRT8001 Block Diagram

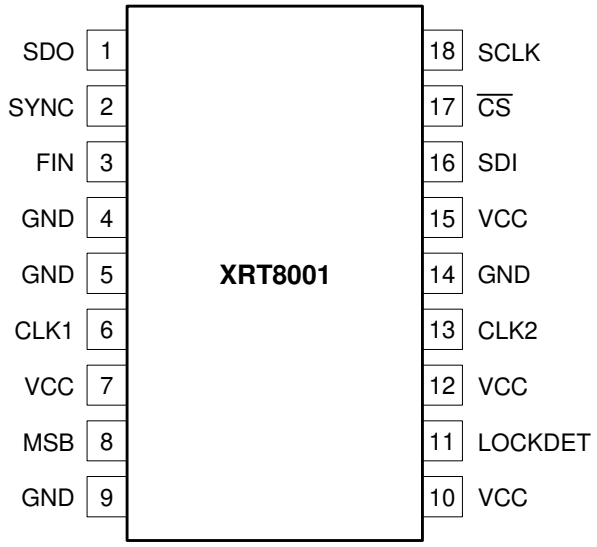


Figure 3. XRT8001 PIN OUT

PIN DESCRIPTION

Pin #	Name	Type	Description
1	SDO	O	**Serial Data Output from the Microprocessor Serial Interface** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SCLK input signal. This pin will be tri-stated upon completion of data transfer.
2	SYNC	O	**Sync Output -** The XRT8001 will typically output an 8kHz clock signal via this output pin. However, when the XRT8001 is operating in the "High Speed - Reverse" Mode, then this device will simply output a 64kHz clock signal.
3	FIN	I	**Reference Clock Input -** The Reference Timing signal (from which the CLK1 and CLK2 output signals are derived) is to be input via this pin.
4	GND	-	**Digital Ground**
5	GND	-	**Digital Ground**
6	CLK1	O	**Clock Output 1 -** The XRT8001 will drive the desired "synthesized" signal via this output pin. This output signal will have a 50±5% duty cycle. ***Note:*** *This output pin is tri-stated unless the "CLK1EN" bit-field (within Command Register CR4) has been set to "1".*
7	V_{CC}	-	**Digital Power Supply**

PIN DESCRIPTION (CONT'D)

Pin #	Name	Type	Description
8	MSB	I	**Master/Slave Mode Select Input -** Setting this input pin "HIGH" configures the XRT8001 to operate in the "MASTER" Mode. Conversely, setting this input pin "LOW" configures the XRT8001 to operate in the "SLAVE" Mode.
9	GND	-	**Analog Ground**
10	VCC	-	**Analog Power Supply**
11	LOCKDET	O	**Lock Detect Output -** This output indicates whether or not the "selected" internal PLL(s) are "in-lock" or are "out-of-lock". By default, this output pin is "high" when both PLLs are in-lock" and will go toggle "low" if either one of the PLLs is "out-of-lock". However, the XRT8001 also permits the user to configure this output pin to reflect the state of any one of the PLLs within the chip. (See Table 3.)
12	VCC	-	**Digital Power Supply**
13	CLK2	O	**Clock Output 2 -** The XRT8001 will drive the desired "synthesized" signal via this output pin. This output signal will have a 50±5% duty cycle. ***Note:*** *This output pin is tri-stated unless the "CLK1EN" bit-field (within Command Register CR4) has been set to "1".*
14	GND	-	**Digital Ground**
15	VCC	-	**Digital Power Supply**
16	SDI	I	**Microprocessor Serial Interface – Serial Data Input** Whenever, the user wishes to read or write data into the Command Registers, over the Microprocessor Serial Interface, the user is expected to apply the "Read/Write" bit, the Address Values (of the Command Registers) and Data Value to be written (during "Write" Operations) to this pin. This input will be sampled on the rising edge of the SCLK pin (pin 18).
17	$\overline{CS}$	I	**Microprocessor Serial Interface – Chip Select Input:** The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT8001 via the Microprocessor Serial Interface. ***Note:*** *This pin is internally pulled "high".*
18	SCLK	I	**Microprocessor Serial Interface-Clock Signal** This signal will be used to sample the data, on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal.

ABSOLUTE MAXIMUM RATINGS

Supply Range 7V
Voltage at any Pin ..... GND -0.3V to Vcc+0.3V
Operating Temperature..... - 40°C to +85°C
Storage Temperature ..... - 40°C to +85°C
Package Dissipation 500mW

DC ELECTRICAL CHARACTERISTICS (Except Microprocessor Serial Interface)[1]

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
V_{IL}	Input Low Level			0.8	V	
V_{IH}	Input High Level	2.0			V	
V_{OL}	Output Low Level (CLK1, CLK2)			0.4	V	I_{OL} = -6.0mA
V_{OH}	Output High Level (CLK1, CLK2)	2.4			V	I_{OL} = 6.0mA
V_{OL}	Output Low Level (LOCKDET, SYNC)			0.4	V	I_{OL} = -3.0mA
V_{OH}	Output High Level (LOCKDET, SYNC)	2.4			V	I_{OL} = 3.0mA
I_{IL}	Input Low Current (CSB, MSB)			-150	mA	
I_{IH}	Input High Current (CSB, MSB)			10	mA	$V_{IN} = V_{CC}$
I_{IL}	Input Low Current (except CSB, MSB)	-10			mA	
I_{IH}	Input High Current (except CSB, MSB)			10	mA	$V_{IN} = V_{CC}$
I_{CC}	Operating Current		11 20	30 35	mA mA	3.3V, No Load, CLk1, CLK2 = 8 x 2.048MHz 5V, No Load, CLk1, CLK2 = 8 x 2.048MHz
R_{IN}	Internal Pull-up Resistance (CSB, MSB)	50	100	150	kW	

Note:
1. 5V tolerant input considerations when operating from 3.3V:

When the XRT8001 is powered at 3.3V, it can tolerate 5V-level signals via its inputs. However, the user should be aware the XRT8001 contains a "Factory-Test" Mode. This mode is enabled whenever the MSB (Master-Slave select) input pin is pulled to about 2V above VDD.

Therefore, if the user is powering the XRT8001 at 3.3V but is applying a 5.25V signal to the MSB input pin, then it is possible that the XRT8001 could be configured to operate in this "Factory-Test" Mode. Since all "Factory-Test" Mode registers are reset to "0", upon chip power, this should not be a problem for the user.

However, if the user performs write operations to "non-defined" address locations within the XRT8001, then the user may observe strange operation from the XRT8001. The user must make sure that when the Microcontroller performs WRITE operations to the XRT8001, it is only performing these WRITE operations to the Address Locations defined in the XRT8001 Data Sheet.

AC ELECTRICAL CHARACTERISTICS (See Figure 4.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t1	Input Frequency	0.008 0.008		32.7 32.7	MHz MHz	3.3V 5V
t2	Minimum Input Signal "High" to "Low" Duration	12			ns	
t3	Output Frequency	56		16,384	kHz	
t6[1]	Duty Cycle	47.5	50	52.5	%	VCC/2 switch point, 30pF Load
t7[4]	Jitter Added 8kHz – 40kHz		0.01 0.01	0.02 0.02	UI UI	3.3V, Output = 1.544MHz (0.025 UI)[3] 5V, Output = 1.544MHz (0.025 UI)[3]
t7[4]	Jitter Added 10Hz – 40kHz		0.03 0.03	 –	UI UI	3.3V, Output = 1.544MHz (0.025 UI)[3] 5V, Output = 1.544MHz (0.025 UI)[3]
t7[4]	Broadband Jitter		0.03 0.035	0.05 0.05	UI UI	3.3V, Output = 1.544MHz (0.05 UI)[3] 5V, Output = 1.544MHz (0.05 UI)[3]
t7[4]	Jitter Added 20Hz – 100kHz		 0.01	0.07 0.07	UI UI	3.3V, Output = 2.048MHz (1.5 UI)[3] 5V, Output = 2.048MHz (1.5 UI)[3]
t7[4]	Jitter Added 18kHz – 100kHz		 0.007	0.03 0.03	UI UI	3.3V, Output = 2.048MHz (0.2 UI)[3] 5V, Output = 2.048MHz (0.2 UI)[3]
t8	Capture Time			40 40	ms ms	3.3V 5V
t9	Clock Output Rise Time			10ns	ns	30pF load measured at 20/80%
t10	Clock Output Fall Time			10ns	ns	30pF load measured at 20/80%
t11[2]	SYNC Output Signal Duty Cycle	40		60	%	VCC/2 switch point
t12	SYNC Ouput Signal + ½ Cycle					
t13	SYNC Output Signal – ½ Cycle					
t14	Delay Time between the rising edge of of SYNC and the Rising edge of CLK1 and CLK2	t-20		t+20	ns	See Table 8 for values of "t"
t21	CSB Low to Rising Edge of SCLK Setup Time	50			ns	
t22	CSB High to Rising Edge of SCLK Hold Time	20			ns	
t23	SDI to Rising Edge of SCLK Setup Time	50			ns	
t24	SDI to Rising Edge of SCLK Hold Time	50			ns	
t25	SCLK "Low" Time	240			ns	
t26	SCLK "High" Time	240			ns	
t27	SCLK Period	500			ns	
t28	CSB Low to Rising Edge of SCLK Hold Time	50			ns	
t29	CSB "Inactive" Time	250			ns	
t30	Falling Edge of SCLK to SDO Valid Time			200	ns	
t31	Falling Edge of SCLK to SDO Invalid Time			100	ns	
t32	Falling Edge of SCLK, or rising edge of CSB to High Z		100		ns	
t33	Rise/Fall time of SDO Output			40	ns	
PW_{MIN}	F_{IN} Duty Cycle	12			ns	

Notes:

[1] $t6 = \frac{t4}{(t4 + t5)}$

[2] $t11 = \frac{t12}{(t12 + t13)}$

[3] *Specifications from AT&T Publication 62411 and ITU-T Recommendations G-823 (for 1.544MHz and (2.048MHz).*

[4] *t7 is guaranteed by characterization, not tested.*

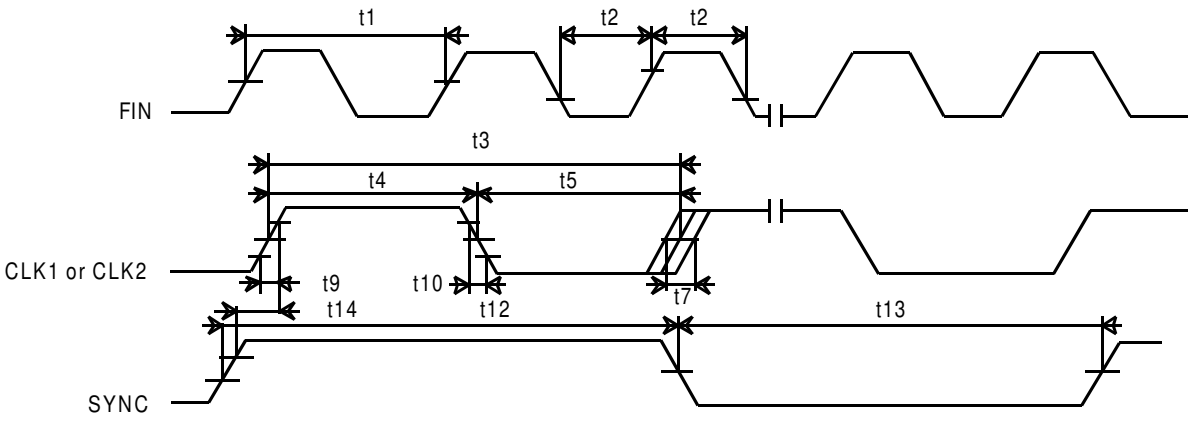


Figure 4. Timing Diagram for Clocks

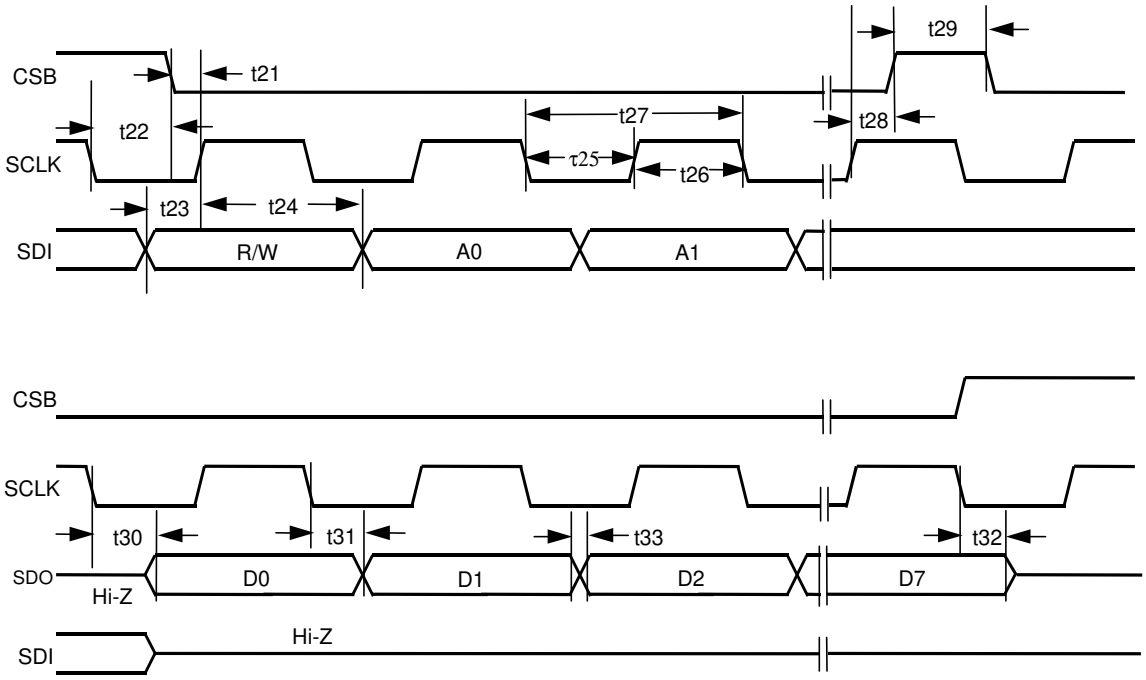


Figure 5. Timing Diagram for the Microprocessor Serial Interface

1.0 Operating the Microprocessor Serial Interface

The XRT8001 Serial Interface is a simple four-wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

CSB - Chip Select (Active Low)
SCLK - Serial Clock
SDI - Serial Data Input
SDO - Serial Data Output

Using the Microprocessor Serial Interface

The following instructions, for using the Microprocessor Serial Interface, are best understood by referring to the diagram in Figure 19.

In order to use the Microprocessor Serial Interface the user must first provide a clock signal to the SCLK input pin. Afterwards, the user will initiate a "Read" or "Write" operation by asserting the "active-low" Chip Select input pin (CSB). It is important to assert the CSB pin (e.g., toggle it "low") at least 50ns prior to the very first rising edge of the clock signal.

Once the CSB input pin has been asserted, the type of operation and the target register address must now be specified by the user. The user provides this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input. Note: each of these bits will be "clocked" into the SDI input on the rising edge of SCLK. These eight bits are identified and described below.

Bit 1 - "R/W" (Read/Write) Bit

This bit will be clocked into the SDI input on the first rising edge of SCLK (after CSB has been asserted). This bit indicates whether the current operation is a "Read" or "Write" operation. A "1" in this bit specifies a "Read" operation; whereas, a "0" in this bit specifies a "Write" operation.

Bits 2 Through 5: The Four (4) Bit Address Values (Labeled A0, A1, A2 and A3)

The next four rising edges of the SCLK signal will clock in the 4-bit address value for this particular Read (or Write) operation. The address selects the Command Register, within the XRT8001, that the user will either be reading data from, or writing data to. The user must supply the address bits to the SDI input pin in ascending order with the LSB (least significant bit) first.

Bits 6 and 7:

The next two bits, A4 and A5, must be set to "0", as shown in Figure 19.

Bit 8 - A6

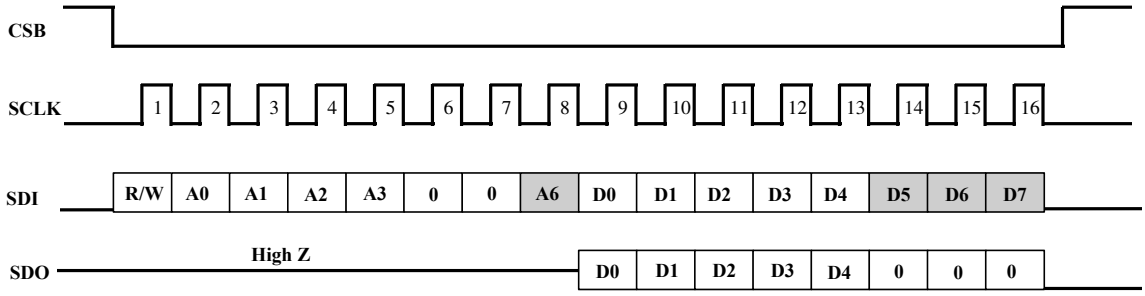
The value of "A6" is a "don't care". Once these first eight bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a "Read" or "Write" operation.

Read Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Read" operation will proceed through an idle period, lasting three SCLK periods. On the falling edge of SCLK Cycle #8 (see Figure 19) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A3, A2, A1, A0]) via the SDO output pin. The Microprocessor Serial Interface will output this 5-bit data word (D0 through D4) in ascending order (with the LSB first), on the falling edges of the SCLK pin. As a consequence, the data (on the SDO output pin) will be sufficiently stable for reading (by the Microprocessor), on the very next rising edge of the SCLK pin.

Write Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Write" operation will proceed through an idle period, lasting three SCLK periods. Prior to the rising edge of SCLK Cycle # 9 (see Figure 6) the user must begin to apply the 8-bit data word, that he/she wishes to write to the Microprocessor Serial Interface, onto the SDI input pin. The Microprocessor Serial Interface will latch the value on the SDI input pin, on the rising edge of SCLK. The user must apply this word (D0 through D7) serially, in ascending order with the LSB first.



Notes:

A4 and A5 are always "0".

R/W = "1" for "Read" Operations

R/W = "0" for "Write" Operations

- Denotes a "don't care" value

Figure 6. Microprocessor Serial Interface Data Structure

Simplified Interface Option

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this "combined" signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal will be tri-stated.

2.1 The Forward/Master Mode

In the Forward/Master Mode, the XRT8001 will accept either an "N x 1.544MHz" or an "N x 2.048MHz" clock signal via the FIN input pin (where: $1 \leq N \leq 16$). From this "reference signal" the XRT8001 will generate either a "K x 56kHz" or a "K x 64kHz" clock signal (where: $1 \leq K \leq 32$).

Figure 7, presents a simple illustration of the XRT8001 WAN Clock operating in the "Forward Master/Mode."

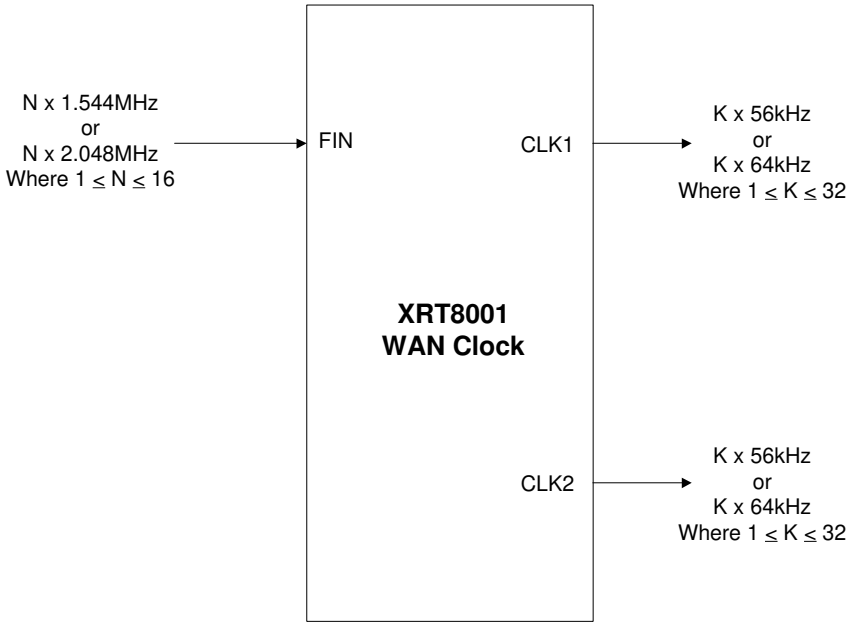


Figure 7. Illustration of the XRT8001 WAN Clock Operating in the Forward/Master Mode

2.2 The Reverse/Master Mode

In the Reverse/Master Mode, the XRT8001 will accept either a 56kHz or a 64kHz clock signal via the FIN input pin, and will generate either a 1.544MHz or a 2.048MHz clock signal via the Clock Output signals.

Figure 8, presents a simple illustration of the XRT8001 WAN Clock operating in the "Reverse/Master Mode."

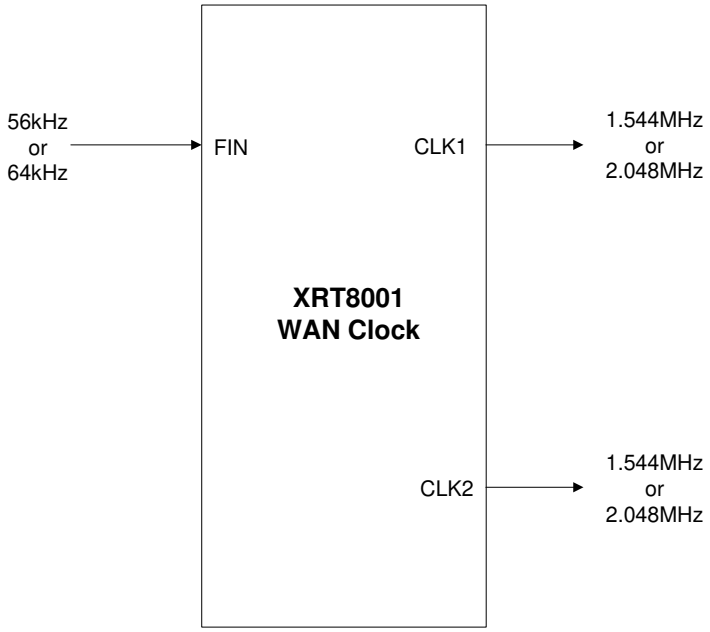


Figure 8. Illustration of the XRT8001 WAN Clock Operating in the Reverse/Master Mode

2.3 The Fractional T1/E1 Reverse/Master Mode

In the Fractional T1/E1 Reverse/Master Mode, the XRT8001 will accept either a “P x 56kHz” or a “P x 64kHz” clock signal via the FIN input pin (where: $1 \leq P \leq 32$). From this “reference signal” the XRT8001 will generate either a 1.544MHz or a 2.048MHz clock signal.

Figure 9, presents a simple illustration of the XRT8001 WAN Clock operating in the “Fractional T1/E1 Reverse/Master" Mode.

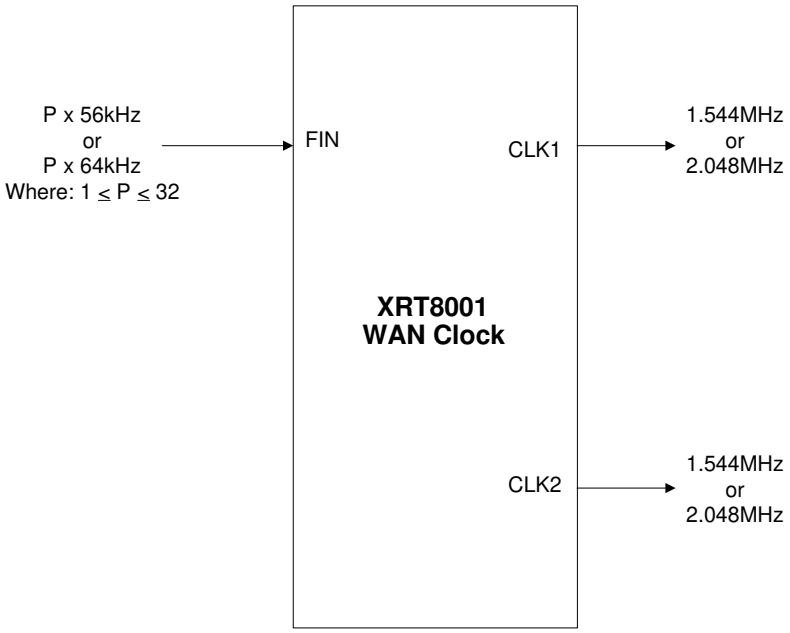


Figure 9. Illustration of the XRT8001 WAN Clock Operating in the “Fractional T1/E1 Reverse/Master” Mode

2.4 The "E1 to T1 Forward/Master" Mode

In the "E1 to T1 Forward/Master" Mode, the XRT8001 will accept a "Q x 2.048MHz" clock signal via the "Reference Clock Input" (FIN), and will output a "1.544MHz" clock signal via the CLK1 and/or CLK2 output pins.

Note: *The value of "Q" can range between 1 and 16.*

Figure 10, presents a simple illustration of the XRT8001 WAN Clock operating in the "E1 to T1 Forward/Master" Mode.

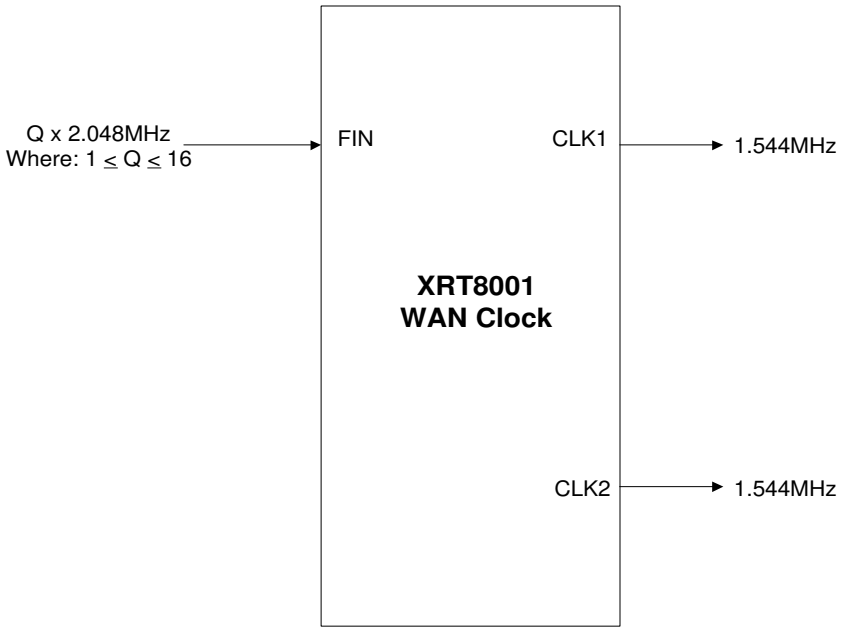


Figure 10. Illustration of the XRT8001 WAN Clock Operating in the "E1 to T1 Forward/Master" Mode

2.5 The "High Speed – Reverse" Mode

In the "High Speed - Reverse" Mode, the XRT8001 will accept a 64kHz clock signal via the "Reference Clock Input" (FIN), and will output a "M x 2.048MHz" clock signal (where M can be equal to 1, 2, 4 or 8) via the CLK1 and/or CLK2 output pins.

Note: The XRT8001 will accept and sythesze these clock frequencies independent of whether it has been configured to operate in the "Master" or "Slave" Modes.

Figure 11, presents a simple illustration of the XRT8001 WAN Clock operating in the "High Speed - Reverse" Mode.

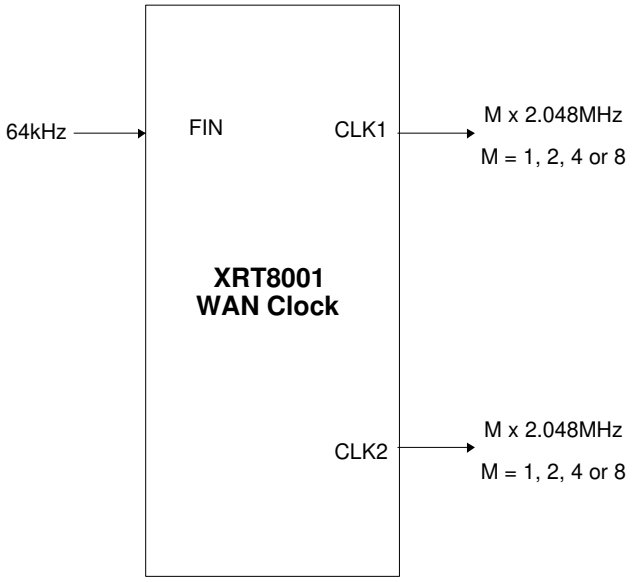


Figure 11. Illustration of the XRT8001 WAN Clock Operating in the "High Speed – Reverse" Mode

2.6 The "Forward/Slave" Mode

In the "Forward/Slave" Mode, the XRT8001 will accept an 8kHz clock signal via the Reference Clock Input (FIN), and will output a "L x 64kHz or L x 56kHz" clock signal (where L can range from 1 to 32) via the CLK1 and CLK2 output pins.

Figure 12 presents a simple illustration of the XRT8001 WAN Clock operating in the "Forward/Slave" Mode.

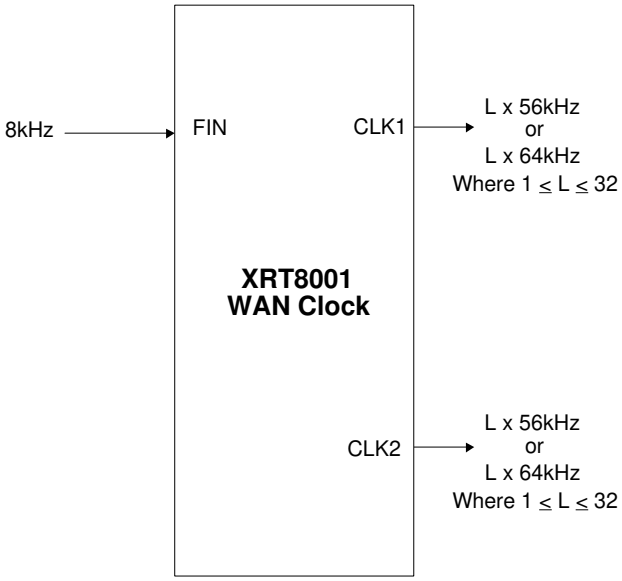


Figure 12. Illustration of the XRT8001 WAN Clock Operating in the "Forward/Slave" Mode

3.0 Description of the Command Registers

3.1 Address Map of the "On-Chip" Command Registers

			Register Bit-Format				
Address	**Command Register**	**Type**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	R/W	IOC4	IOC3	IOC2	IOC1	PL1EN
0x01	CR1	R/W	M4	M3	M2	M1	PL2EN
0x02	CR2	R/W	SEL14	SEL13	SEL12	SEL11	SEL10
0x03	CR3	R/W	SEL24	SEL23	SEL22	SEL21	SEL20
0x04	CR4	R/W	SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

3.2 Command Register Description

3.2.1 Command Register CR0 (Address = 0x00)

D4 – D1 (Configuration Mode Select Bits)

These four-bit fields permit the user to select which mode the XRT8001 will operate in. Specifically, these four bit-fields make the following configuration selections:

1. Whether the XRT8001 will be operating in the “Forward/Master”, “Reverse/Master”, “Fractional T1/E1 Reverse/Master”, "E1 to T1 - Forward/Master" and “High Speed - Reverse” odes.
2. What kind of input signals are to be applied to the Reference Clock Input (FIN).
3. What kind of signals will be output via the CLK1 and CLK2 output pins.

Table 2A relates the value of these four bit-fields to the four Master Modes and Table 2B relates to the three Slave Modes of the XRT8001.

D[4:1]	Mode	Input Frequency (at the FIN input)	CLK1 Output Signal	CLK2 Output Signal
0000	Forward/Master	N x 1.544MHz	K x 56kHz	K x 56kHz
0001	Forward/Master	N x 1.544MHz	K x 56kHz	K x 64kHz
0010	Forward/Master	N x 1.544MHz	K x 64kHz	K x 64kHz
0011	Reverse/Master	56kHz	1.544MHz	2.048MHz
0100	Forward/Master	N x 2.048MHz	K x 56kHz	K x 56kHz
0101	Forward/Master	N x 2.048MHz	K x 56kHz	K x 64kHz
0110	Forward/Master	N x 2.048MHz	K x 64kHz	K x 64kHz
0111	Reverse/Master	64kHz	1.544MHz	2.048MHz
1000	E1 to T1 – Forward/Master	Q x 2.048MHz	1.544MHz	1.544MHz
1001	Fract. T1/E1 Reverse/Master	P x 56kHz	1.544MHz	2.048MHz
1010	Fract. T1/E1 Reverse/Master	P x 56kHz	1.544MHz	1.544MHz
1011	Fract. T1/E1 Reverse/Master	P x 64kHz	2.048MHz	1.544MHz
1100	Fract. T1/E1 Reverse/Master	P x 64kHz	2.048MHz	2.048MHz
1101	High Speed - Reverse	64 kHz	M x 2.048MHz	M x 2.048MHz
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

Table 1. Relationship between the value of "D4 – D1 (within Command Register CR0) and the Operating Modes of the XRT8001 WAN Clock - Master Modes

D[4:1]	Mode	Input Frequency (at the FIN input)	CLK1 Output Signal	CLK2 Output Signal
0000	Forward/Slave	8kHz	K x 56kHz	K x 56kHz
0001	Forward/Slave	8kHz	K x 56kHz	K x 64kHz
0010	Forward/Slave	8kHz	K x 64kHz	K x 64kHz
0011	Reverse/Slave	8kHz	1.544MHz	2.048MHz
0100	Forward/Slave	8kHz	K x 56kHz	K x 56kHz
0101	Forward/Slave	8kHz	K x 56kHz	K x 64kHz
0110	Forward/Slave	8kHz	K x 64kHz	K x 64kHz
0111	Reverse/Slave	8kHz	1.544MHz	2.048MHz
1000	Reverse/Slave	8kHz	K x 56KHz	K x 64KHz
1001	Reverse/Slave	8kHz	1.544MHz	2.048MHz
1010	Reverse/Slave	8kHz	1.544MHz	1.554MHz
1011	Reverse/Slave	8kHz	2.048MHz	1.544MHz
1100	Reverse/Slave	8kHz	2.048MHz	2.048MHz
1101	High Speed – Reverse	64kHz	M x 2.048MHz	M x 2.048MHz
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

Table 2. Relationship between the value of "D4 – D1" (within Command Register CR0) and the Operating Modes of the XRT8001 WAN Clock – Slave Modes

D0 – PL1EN (PLL # 1 Enable Select)

This bit-field permits the user to enable or disable PLL # 1, within the XRT8001 WAN Clock. Setting this bit-field to "1" enables PLL # 1 for Frequency Synthesis. Conversely, setting this bit-field to "0" disables PLL # 1 for Frequency Synthesis.

3.2.2 Command Register CR1 (Address = 0x01)

D4 – D1: (M4 – M1)

These bit-fields are used to support configuration implementation for both the "Forward/Master" and "E1 to T1 - Forward/Master" Modes. In both the "Forward/Master" and "E1 to T1 - Forward/Master" Modes, the XRT8001 WAN Clock will be receiving either a "N x 1.544MHz" or a "N x 2.048MHz" clock signal. The M4 through M1 bit-fields, within this register, permit the user to specify the value of "N". As a consequence, the XRT8001 can be configured to accept a maximum frequency of "16 x 1.544MHz" or "16 x 2.048MHz".

D0 – PL2EN (PLL # 2 Enable Select)

This bit-field permits the user to enable or disable PLL # 2, within the XRT8001 WAN Clock. Setting this bit-field to "1" enables PLL # 2 for Frequency Synthesis. Conversely, setting this bit-field to "0" disables PLL # 2 for Frequency Synthesis.

3.2.3 Command Register CR2 (Address = 0x02)

D4 – D0 (SEL1[4:0])

These bit-fields are used to support configuration implementation for both the "Forward/Master", "Fractional T1/E1 Reverse/Master" and "High Speed – Reverse" Modes.

In the Forward/Master Mode

In the "Forward/Master" Mode, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal via the CLK1 output pin. These five (5) bit-fields within Command Register CR2 are used to define the value of "K" for the CLK1 Output. As a consequence, the XRT8001 can be configured to generate a maximum frequency of "32 x 56kHz" or "32 x 64kHz" via the CLK1 output pin.

In the "Fractional T1/E1 Reverse/Master" Mode

In the "Fractional T1/E1 Reverse/Master" Mode, the XRT8001 WAN Clock will be receiving either a "P x 56kHz" or a "P x 64kHz" clock signal via the "FIN" input pin. The XRT8001 WAN Clock will, in response, generate either a 1.544MHz or a 2.048MHz clock signal via the CLK1 and/or CLK2 output pins. These five (5) bit-fields are used to define the value of "P". As a consequence, the XRT8001 can be configured to accept a maximum frequency of "32 x 56kHz" or "32 x 64kHz".

In the "High Speed – Reverse" Mode

In the "High Speed – Reverse" Mode, the XRT8001 WAN Clock will be receiving a 64kHz clock signal via the "FIN" input pin. The XRT8001 WAN Clock will, in response, generate an "M x 2.048MHz" clock via the CLK1 and CLK2 output pins. These five (5) bit-fields within Command Register CR2 are used to define the value "M" for the CLK1 output.

Note: *The only acceptable values for "M" are 1, 2, 4, or 8.*

3.2.4 Command Register CR3 (Address = 0x03)

D4 – D0 (SEL2[4:0])

These bit-fields are used to support configuration implementation for the "Forward/Master" and the "High Speed – Reverse" Modes of operation.

In the "Forward/Master" Mode

In the "Forward/Master" Mode, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal via the CLK2 output pin. These five (5) bit-fields within Command Register CR3 are used to define the value of "K" for the CLK2 Output. As a consequence, the XRT8001 can be configured to generate a maximum frequency of "32 x 56kHz" or "32 x 64kHz" via the CLK2 output pin.

In the "High Speed – Reverse" Mode

In the "High Speed – Reverse" Mode, the XRT8001 WAN Clock will be receiving a 64kHz clock signal via the "FIN" input pin. The XRT8001 WAN Clock will, in response, generate an "M x 2.048MHz" clock via the CLK1 and CLK2 output pins. These five (5) bit-fields within Command Register CR3 are used to define the value "M" for the CLK2 output.

Note: *The only acceptable values for "M" are 1, 2, 4, or 8.*

3.2.5 Command Register CR4 (Address = 0x04)

D4 – SYNCEN (SYNC Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the SYNC output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D3 – CLK1EN (CLK1 Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the CLK1 output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D2 – CLK2EN (CLK2 Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the CLK2 output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D1, D0 – LDETDIS[2:1] – Lock Detector Output Control

The combination of these two bit-fields permit the user to specify the signal that will be output via the LOCKDET output pin. The user's options are shown in Table 3.

LDETDIS[2:1]	Signal output via the LOCKDET Signal
00	**The LOCK Condition of PLL1 AND PLL2** With this selection, the LOCKDET output pin will be "high" if either one of the following conditions are true. a. If both PLL1 and PLL2 are in the "LOCK" condition, (**applies if both PLL1 and PLL2 are enabled**) or b. If the only enabled PLL is in the "LOCK" condition (**applies only if one of the PLLs are enabled**).
01	**The LOCK Condition of PLL2 Only** With this selection, only the "LOCK" state of PLL2 will be reflected in the LOCKDET output pin. LOCKDET = "high" if PLL2 is in "LOCK". LOCKDET = "low" if PLL2 is out of "LOCK".
10	**The LOCK Condition of PLL1 Only** With this selection, only the "LOCK" state of PLL1 will be reflected in the LOCKDET output pin. LOCKDET = "high" if PLL1 is in "LOCK". LOCKDET = "low" if PLL1 is out of "LOCK".
11	LOCKDET will be unconditionally pulled to "LOW"

Table 3. Relationship Between the Values of the LDETDIS[2:1] Bit-Fields and the Meaning of the LOCKDET Output Signal

4.0 Instructions for Configuring the XRT8001 WAN Clock

As mentioned earlier, the XRT8001 WAN Clock can be configured to operate in the following modes:

- The "Forward/Master" Mode
- The "Reverse/Master" Mode
- The "Fractional T1/E1 Reverse/Master" Mode
- The "E1 to T1 – Forward/Master" Mode
- The "High Speed – Reverse" Mode
- The "Forward/Slave" Mode

A detailed description of the operation and the configuration steps for each of these configurations follows.

4.1 The "Forward/Master" Mode.

When the XRT8001 WAN Clock has been configured to operate in the "Forward/Master" Mode, then it will accept an "N x 1.544MHz" or an "N x 2.048MHz" clock signal via the "Reference Clock" input at FIN (pin 3); where "N" can range anywhere between 1 and 16. In response to this clock signal, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal, via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock, operating in the "Forward/Master" Mode is shown in figure 13.

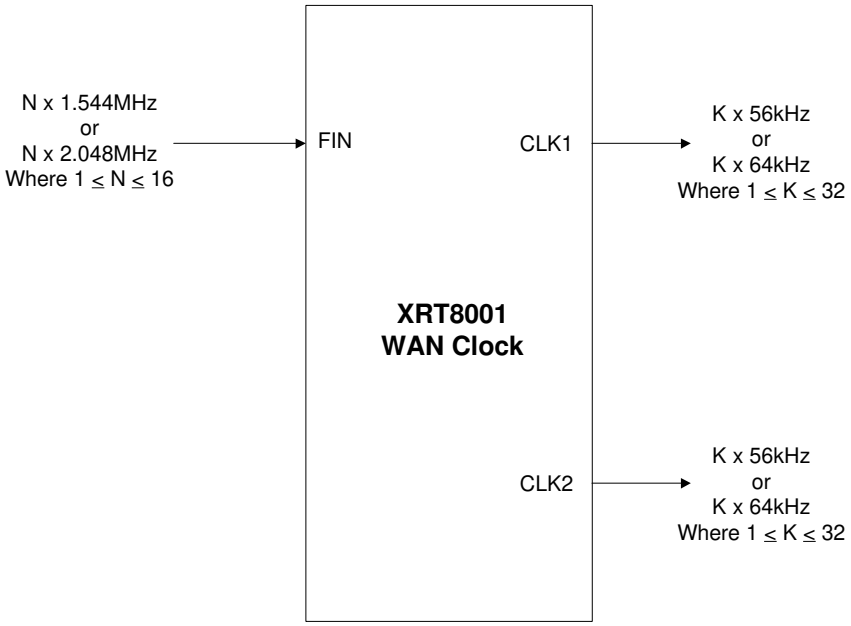


Figure 13. Illustration of the XRT8001 WAN Clock Device Operating in the "Forward/Master" Mode

5.0 Configuring the XRT8001 WAN Clock into the "Forward/Master" Mode

The user can configure the XRT8001 WAN Clock to operate in the "Forward/Master" Mode, by executing the following steps:

Step 1 *– Configure the XRT8001 to operate in the "MASTER" Mode, by pulling the MSB pin (pin 8) to VDD.*

Step 2 *– Review Table 4, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.*

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4-D1 in CR0
N x 1.544MHz	K x 56kHz	K x 56kHz	0000
N x 1.544MHz	K x 56kHz	K x 64kHz	0001
N x 1.544MHz	K x 64kHz	K x 64kHz	0010
N x 2.048MHz	K x 56kHz	K x 56kHz	0100
N x 2.048MHz	K x 56kHz	K x 64kHz	0101
N x 2.048MHz	K x 64kHz	K x 64kHz	0110

Table 4. Listing of "Input Frequency and "Output Frequency" Cases for "Forward/Master" Mode Operation

Step 3 *– Upon reviewing Table 4, write the listed value (under the "Value to Write to D4 – D1 in CR0" Register Column) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below.*

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 to operate in the "Forward/Master" Mode.

Step 4 *– Next, you need to specify the value for "N" (e.g., as in the "N x 1.544MHz" or "N x 2.048MHz" clock signal which is to be applied to the "FIN" input pin.)*

In order to specify the value for "N", one needs to write the value of "N - 1" (in binary format) into the "D4 through D1" bits within Command Register CR1, as illustrated below.

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Value of "N - 1" (in Binary Format)				X

For example, if the user wishes to configure the XRT8001 to accept a 1.544MHz clock signal, via the "FIN" input pin (e.g., N = 1), then the user should write in the value "0", into Command Register CR1.

Note: *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

Step 5 *– Specify the value of "K" (e.g., as in the "K x 56kHz" or "K x 64kHz" clock signal which is to be output via the CLK1 output signal).*

In order to specify the value for "K", one needs to write the value of "K - 1" (in binary format) into Command Register CR2, as illustrated below.

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
Value of "K - 1" (in Binary Format).				

For example, if one wishes to configure the XRT8001 to output a clock signal of either "56kHz" or "64kHz" (e.g., where "K" = 1) via the CLK1 output pin, then he/she should write the value "0", into Command Register CR2.

Step 6 *– Specify the value of "K" (e.g., as in the "K x 56kHz" or "K x 64kHz" clock signal which is to be output via the CLK2 output signal).*

In order to specify the value for "K", one needs to write the value of "K - 1" (binary format) into Command Register CR3, as illustrated below.

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
Value of "K - 1" (in Binary Format).				

For example, if one wishes to configure the XRT8001 to output a clock signal of either "1.792MHz" or "2.048MHz" (e.g., where "K" = 32) via the CLK2 output pin, then he/she should write the value "31" (or "1 1 1 1 1" in binary format) into Command Register CR3.

Step 7 *– Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below.

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

Note: *For information on the "LDETDIS1" and "LDETDIS2" bit-fields, please see Table 3.*

6.0 The "Reverse/Master" Mode

When the XRT8001 WAN Clock has been configured to operate in the "Reverse/Master" Mode, then it will accept either a "56kHz" or a "64kHz" clock signal via the "Reference Clock" input at FIN (pin 3). In response to this clock signal, the XRT8001 WAN Clock will output either a "1.544MHz" or a "2.048MHz" clock signal, via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock, operating in the "Reverse/Master" Mode is presented in Figure 14.

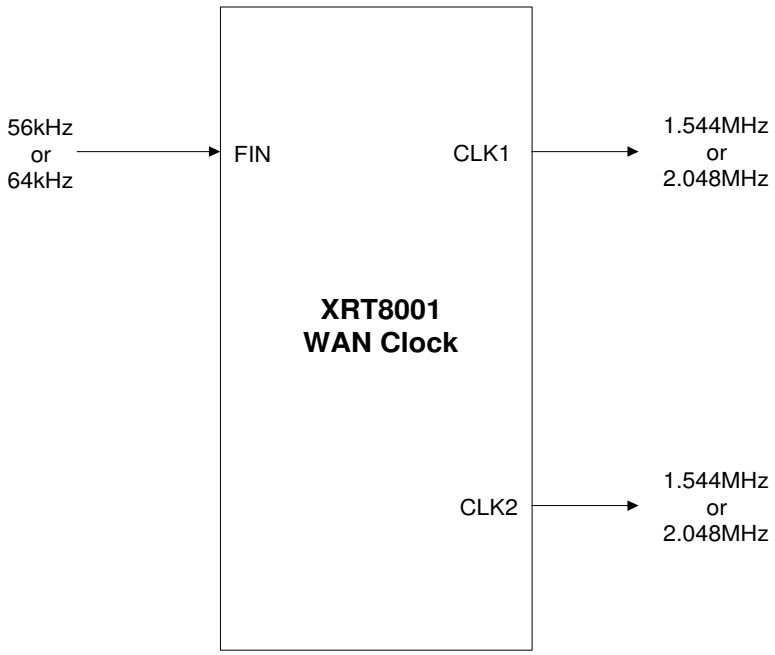


Figure 14. Illustration of the XRT8001 WAN Clock Operating in the "Reverse/Master" Mode

6.1 Configuring the XRT8001 WAN Clock Device into the "Reverse/Master" Mode

The user can configure the XRT8001 WAN Clock to operate in the "Reverse/Master" Mode, by executing the following steps:

Step 1 *– Configure the XRT8001 to operate in the "MASTER" Mode by pulling the "MSB" pin (pin 8) to VDD.*

Step 2 *– Review Table 5, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.*

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4 – D1 in CR0
56kHz	1.544MHz	2.048MHz	0011
64kHz	1.544MHz	2.048MHz	0111

Table 5. Listing of "Input Frequency" and "Output Frequency" Cases for "Reverse/Master" Mode Operation

Step 3 *– Upon reviewing Table 5, write the listed value (under the "Value to Write to D4 – D1 in CR0" register) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below:*

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 to operate in the "Reverse/Master" Mode.

Step 4 *– Write a "1" into the "PL2EN" bit-field within Command Register CR1 (if you wish to output a clock signal via the "CLK2" output pin), as illustrated below:*

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Don't Care				1

Notes:

1. *The value of the "D4 through D1" bit-fields within Command Register, CR1 are "Don't Care".*
2. *The contents of Command Registers CR2 and CR3 are "Don't Care".*

Step 5 *– Enable any of the following output signals as appropriate: SYNC", CLK1, CLK2 and LOCKDET.*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below:

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

Note: *For information on the "LDETDIS1" and "LDETDIS2" bit-fields, please see Table 3.*

6.2 The "Fractional T1/E1 Reverse/Master" Mode

When the XRT8001 WAN Clock has been configured to operate in the "Fractional T1/E1 Reverse/Master" Mode, then it will accept either a "P x 56kHz" or a "P x 64kHz" clock signal via the "FIN" input pin (pin 3). In response, the XRT8001 will output either a 1.544MHz or a 2.048MHz clock signal via the CLK1 and/or CLK2 outputs.

A simple illustration of the XRT8001 WAN Clock, operating in the "Fractional T1/E1 Reverse/Master" Mode is presented in Figure 15.

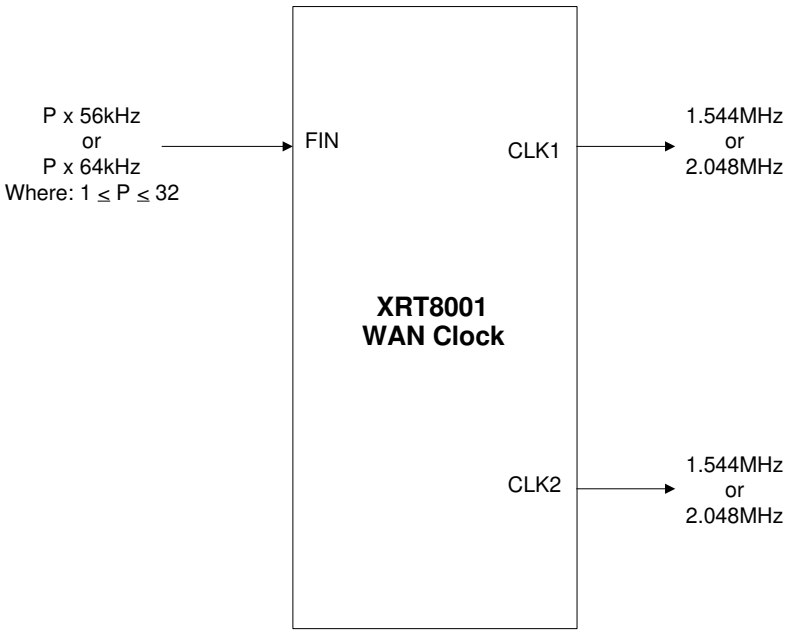


Figure 15. Illustration of the XRT8001 WAN Clock Operating in the "Fractional T1/E1 Reverse/Master" Mode

6.3 Configuring the XRT8001 WAN Clock into the "Fractional T1/E1 Reverse/Master" Mode

The user can configure the XRT8001 WAN Clock to operate in the "Fractional T1/E1 Reverse/Master" Mode by executing the following steps.

Step 1 *– Configure the XRT8001 to operate in the "MASTER" Mode, by pulling the "MSB" input pin (pin 8) to VDD.*

Step 2 *– Review Table 6, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.*

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4 – D1 in CR0
P x 56kHz	1.544MHz	2.048MHz	1001
P x 56kHz	1.544MHz	1.544MHz	1010
P x 64kHz	2.048MHz	1.544MHz	1011
P x 64kHz	2.048MHz	2.048MHz	1100

Table 6. Listing of "Input Frequency" and "Output Frequency" Cases for "Fractional T1/E1 Reverse/Master" Mode Operation