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GENERAL DESCRIPTION

The XRT83L30 is a fully integrated single-channel long-haul and short-haul line interface unit for T1(1.544Mbps) 100Ω, E1(2.048Mbps) 75Ω or 120Ω and J1 110Ω applications.

In long-haul applications the XRT83L30 accepts signals that have passed through cables from 0 feet to over 6000 feet in length and have been attenuated by 0 to 45dB at 772kHz in T1 mode or 0 to 43dB at 1024kHz in E1 mode. In T1 applications, the XRT83L30 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB, -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generator that can be used for arbitrary output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83L30 provides both Serial Host microprocessor interface and Hardware Mode for programming and control. Both B8ZS and HDB3 encoding and decoding functions are included and can be disabled as required. On-chip crystal-less jitter attenuator with a 32 or 64 bit FIFO can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L30 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. For the receiver this is accomplished by internal resistors or through the combination of one single fixed value external resistor and programmable internal resistors. In the absence of the power supply, the transmit output and receive input are tri-stated allowing for redundancy applications. The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

FEATURES

(See Page 2)

FIGURE 1. BLOCK DIAGRAM OF THE XRT83L30 T1/E1/J1 LIU (HOST MODE)

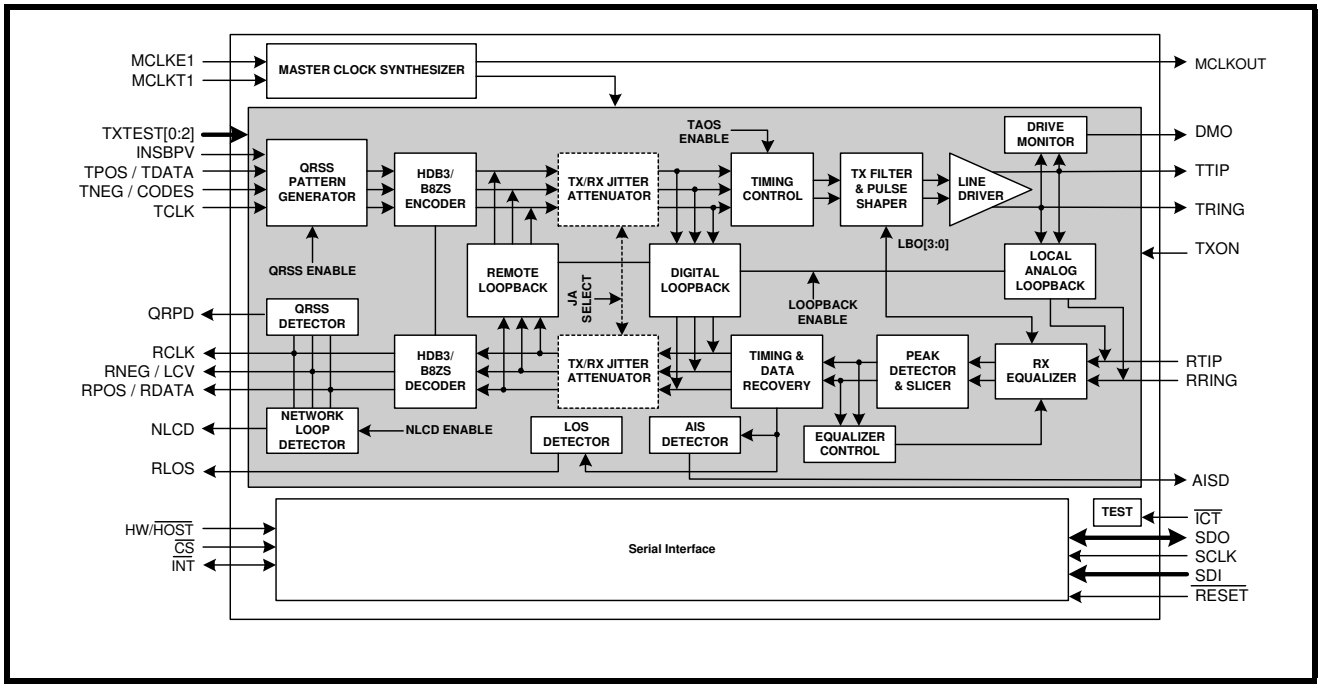
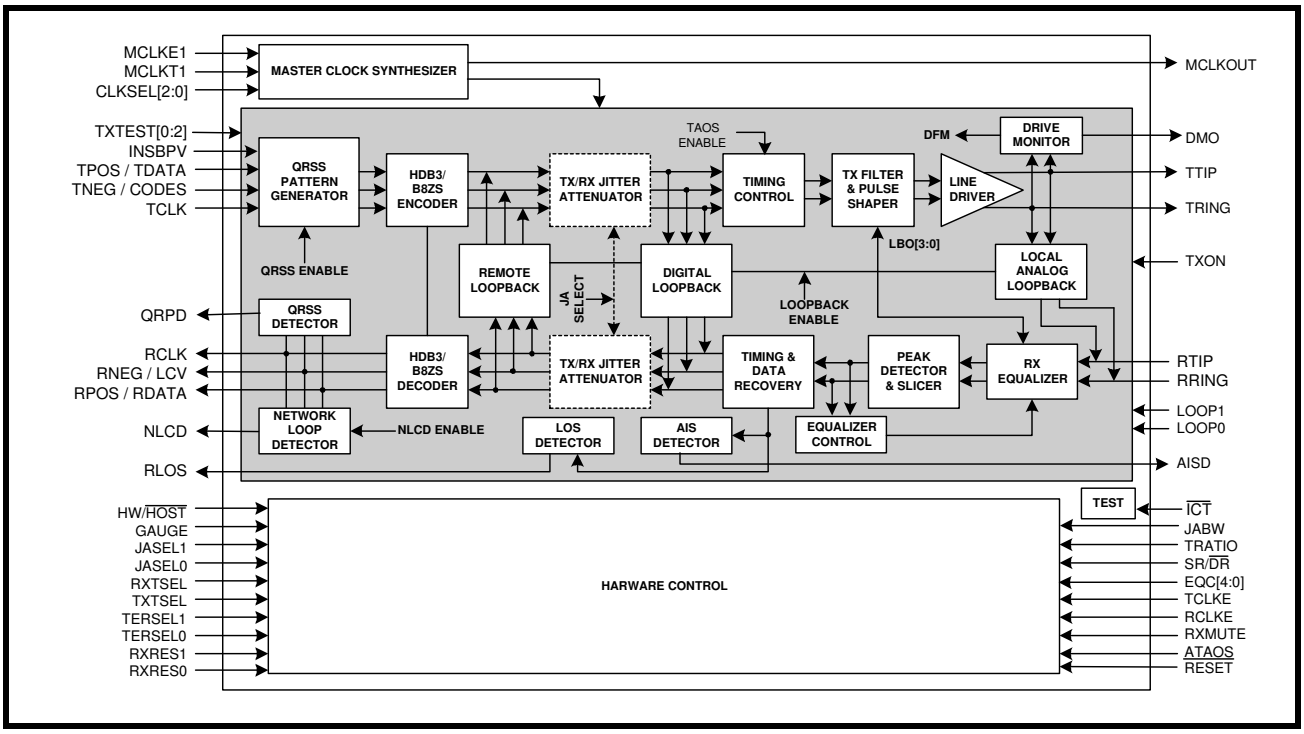


FIGURE 2. BLOCK DIAGRAM OF THE XRT83L30 T1/E1/J1 LIU (HARDWARE MODE)



FEATURES

- Fully integrated single-channel long-haul and short-haul transceiver for E1,T1 or J1 applications.
- Adaptive Receive Equalizer for cable attenuation of up to 45dB for T1 and 43dB for E1.
- Programmable Transmit Pulse Shaper for E1,T1 or J1 short-haul interfaces.
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping.
- Programmable Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps.
- Tri-State transmit output and receive input capability for redundancy applications
- Selectable receiver sensitivity from 0 to 36dB or 0 to 45dB cable loss for T1 @772kHz and 0 to 43dB for E1 @1024kHz.
- High receiver interference immunity
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for both T1 and E1 modes.
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications.
- Internal and external impedance matching for 75Ω,100Ω, 110Ω and 120Ω.
- Transmit return loss meets or exceeds ETSI 300 166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO Selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)

- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder
- QRSS pattern generation and detection for testing and monitoring
- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both Hardware and serial Microprocessor interface for programming
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Single +3.3V Supply Operation
- 64 pin TQFP package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L30IV	64 Lead TQFP (10 x 10 x 1.4mm)	-40°C to +85°C

FIGURE 3. PIN OUT OF THE XRT83L30

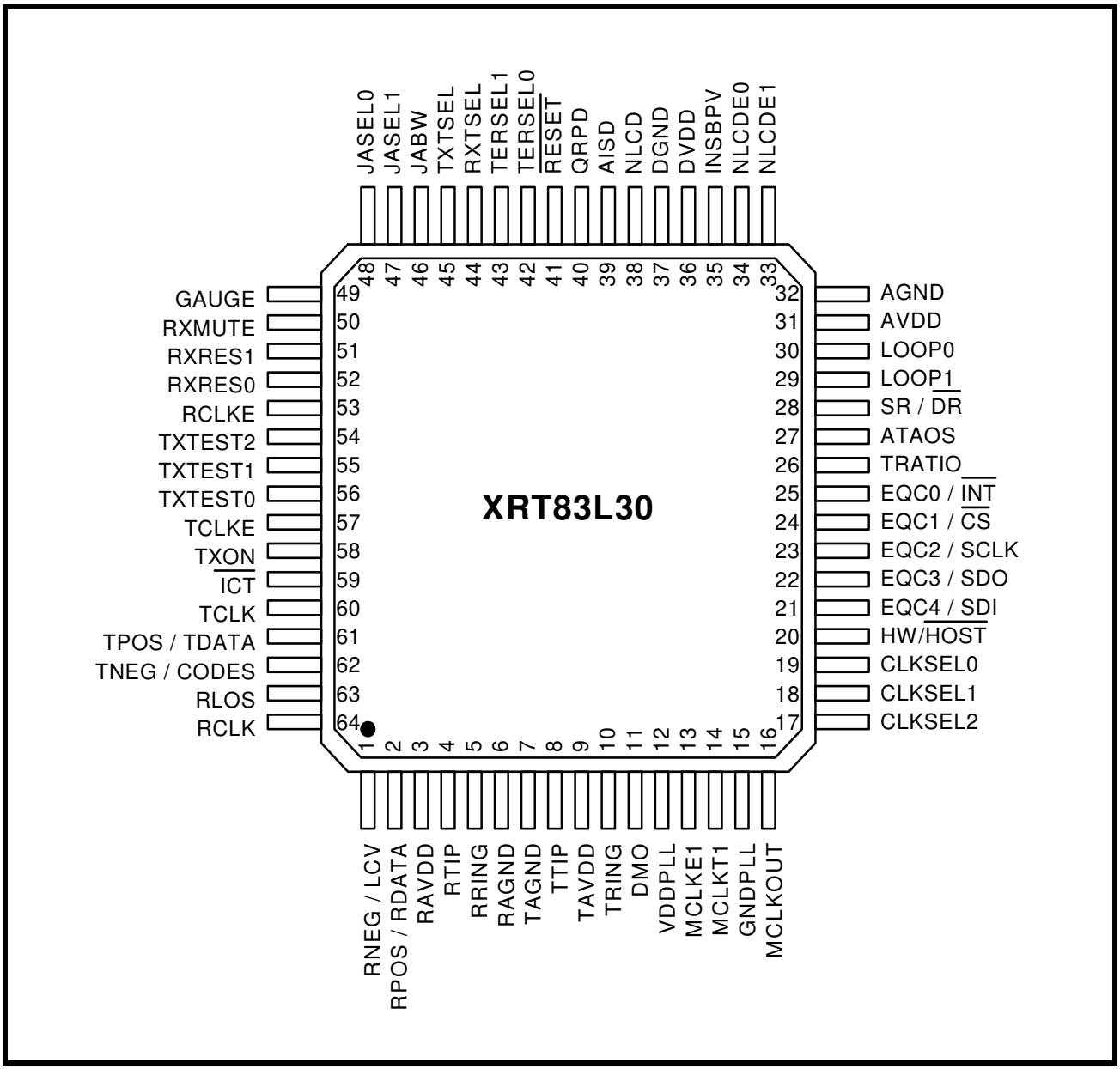


TABLE OF CONTENTS

PIN DESCRIPTIONS BY FUNCTION

SERIAL INTERFACE

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
HW/$\overline{\text{HOST}}$	20	**I**	**Mode Control Input** This pin is used for selecting **Hardware** or **Host** mode to control the device. Leave this pin unconnected or tie "High" to select **Hardware** mode. For **Host** mode, this pin must be tied "Low". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
SDI	21	**I**	**Serial Data Input** In **Host** mode, this pin is the data input for the Serial Interface.
EQC4			**Equalizer Control Input 4** **Hardware** mode, **SEE"CONTROL FUNCTION" ON PAGE 13.**
SDO	22	**O**	**Serial Data Output** In **Host** mode, this pin is the output "Read" data for the serial interface.
EQC3		**I**	**Equalizer Control Input 3** **Hardware** mode, **SEE"CONTROL FUNCTION" ON PAGE 13.**
SCLK	23	**I**	**Serial Interface Clock Input** In **Host** mode, this clock signal is used to control data "Read" or "Write" operation for the Serial Interface. Maximum clock frequency is 20MHz.
EQC2			**Equalizer Control Input 2** **Hardware** mode, **SEE"CONTROL FUNCTION" ON PAGE 13.**
$\overline{\text{CS}}$	24	**I**	**Chip Select Input** In **Host** mode, tie this pin "Low" to enable communication with the device via the Serial Interface.
EQC1			**Equalizer Control Input 1** **Hardware** mode, **SEE"CONTROL FUNCTION" ON PAGE 13.**
$\overline{\text{INT}}$	25	**O**	**Interrupt Output (active "Low")** In **Host** mode, this pin goes "Low" to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to "0" in the command control register.
EQC0		**I**	**Equalizer Control Input 0** **Hardware** mode, **SEE"CONTROL FUNCTION" ON PAGE 13.** ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*

RECEIVER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RLOS	63	**O**	**Receiver Loss of Signal** This signal is asserted 'High' for at least one RCLK cycle to indicate loss of signal at the receive input.
RCLK	64	**O**	**Receiver Clock Output**
RNEG **LCV**	1	**O**	**Receiver Negative Data Output** In dual-rail mode, this signal is the receiver negative-rail output data. **Line Code Violation Output** In single-rail mode, this signal goes 'High' for one RCLK cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go "High".
RPOS **RDATA**	2	**O**	**Receiver Positive Data Output** In dual-rail mode, this signal is the receive positive-rail output data sent to the Framer. **Receiver NRZ Data Output** In single-rail mode, this signal is the receive NRZ format output data sent to the Framer.
RTIP	4	**I**	**Receiver Differential Tip Positive Input** Positive differential receive input from the line.
RRING	5	**I**	**Receiver Differential Ring Negative Input** Negative differential receive input from the line.
RXMUTE	50	**I**	**Receive Muting** In **Hardware** mode, connect this pin 'High' to mute RPOS and RNEG outputs to a "Low" state upon receipt of LOS condition to prevent data chattering. Connect this pin to 'Low' to disable muting function. ***NOTE:*** *Internally pulled "Low" with 50kΩ resistor.*
RCLKE	53	**I**	**Receive Clock Edge** In **Hardware** mode, with this pin set to 'High' the output receive data is updated on the falling edge of RCLK. With this pin tied 'Low', output data is updated on the rising edge of RCLK. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

TRANSMITTER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TTIP	8	**O**	**Transmitter Tip Output** Positive differential transmit output to the line.
TRING	10	**O**	**Transmitter Ring Output** Negative differential transmit output to the line.
TPOS	61	**I**	**Transmitter Positive Data Input** In dual-rail mode, this signal is the positive-rail input data for the transmitter.
TDATA			**Transmitter Data Input** In single-rail mode, this pin is used as the NRZ input data for the transmitter. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TNEG	62	**I**	**Transmitter Negative NRZ Data Input** In dual-rail mode, this signal is the negative-rail input data for the transmitter. In single-rail mode, this pin can be left unconnected.
CODES			**Coding Select** In **Hardware** mode and with single-rail mode selected, connecting this pin "Low" enables HDB3 in E1 or B8ZS in T1 encoding and decoding. Connecting this pin "High" selects AMI data format. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TCLK	60	**I**	**Transmitter Clock Input** E1 rate at 2.048MHz ± 50ppm T1 rate at 1.544MHz ± 32ppm During normal operation, both in **Host** mode and **Hardware** mode, TCLK is used for sampling input data at TPOS/TDATA and TNEG/CODES while MCLK is used as the timing reference for the transmit pulse shaping circuit.
TCLKE	57	**I**	**Transmit Clock Edge** In **Hardware** mode, with this pin set to a "High", transmit input data is sampled at the rising edge of TCLK. With this pin tied "Low", input data are sampled at the falling edge of TCLK. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TXON	58	**I**	**Transmitter Turn On** In **Hardware** mode, setting this pin "High" turns on the Transmit Section. In this mode, when TXON = "0", TTIP and TRING driver outputs will be tri-stated. ***NOTES:*** 1. *Internally pulled "Low" with a 50kΩ resistor.* 2. *In **Hardware** mode only, the receiver is turned on at power-up.*

TRANSMITTER

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>TXTEST2
TXTEST1
TXTEST0</td><td>54
55
56</td><td>I</td><td>Transmit Test Pattern pin 2
Transmit Test Pattern pin 1
Transmit Test Pattern pin 0
TXTEST[2:0] pins are used to generate and transmit test patterns according to the following table:
<table>
<tr><th>TXTEST2</th><th>TXTEST1</th><th>TXTEST0</th><th>Test Pattern</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Transmit Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>TAOS</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>TLUC</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>TLDC</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>TDQRSS</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>TDQRSS & INVQRSS</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>TDQRSS & INSBER</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>TDQRSS & INVQRSS & INS</td></tr>
</table>
TAOS (Transmit All Ones): Activating this condition enables the transmission of an All Ones Pattern.TCLK must not be tied "Low".

TLUC (Transmit Network Loop-Up Code): Activating this condition enables the Network Loop-Up Code of "00001" to be transmitted to the line. When Network Loop-Up code is being transmitted, the XRT83L30 will ignore the Automatic Loop-Code detection and Remote Loop-back activation (NLCDE1=”1”, NLCDE0=”1”, if activated) in order to avoid activating Remote Digital Loop-back automatically when the remote terminal responds to the Loop-back request.

TLDC (Transmit Network Loop-Down Code): Activating this condition enables the network Loop-Down Code of "001" to be transmitted to the line.

TDQRSS (Transmit/Detect Quasi-Random Signal): Setting TXTEST2=”1”, regardless of the state of TXTEST1 and TXTEST0, enables Quasi-Random Signal Source generation and detection. In a T1 system QRSS pattern is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. In a E1 system, QRSS is a 2^{15}-1 PRBS pattern.

When TXTEST2 is “1” and TDQRSS is active, setting TXTEST0 to “1” inverts the polarity of transmitted QRSS pattern. Resetting to "0" sends the QRSS pattern with no inversion.

When TXTEST2 is “1” and TDQRSS is active, transitions of TXTEST1 from "0" to "1" results in a bit error to be inserted in the transmitted QRSS pattern. The state of this pin is sampled on the rising edge of TCLK. To ensure the insertion of a bit error, this pin should be reset to a "0" before setting to a "1".

When TXTEST2 is “1”, TXTEST1 and TXTEST0 affect the transmitted QRSS bit pattern independently.</td></tr>
</table>

JITTER ATTENUATOR

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
JABW	46	I	**Jitter Attenuator Bandwidth** In **Hardware** and E1 mode, when JABW="0" the jitter attenuator bandwidth is 10Hz (normal mode). Setting JABW to "1" selects a 1.5Hz Bandwidth for the Jitter Attenuator and the FIFO length will be automatically set to 64 bits. In T1 mode the Jitter Attenuator Bandwidth is always set to 3Hz, and the state of this pin has no effect on the Bandwidth. See table under JASEL1 pin, below. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
JASEL1 **JASEL0**	47 48	I	**Jitter Attenuator select pin 1** **Jitter Attenuator select pin 0** In **Hardware** mode, JASEL0, JASEL1 and JABW pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it and set the jitter attenuator bandwidth and FIFO size per the following table.

JABW	JASEL1	JASEL0	JA Path	JA BW (Hz)		FIFO Size T1/E1
				T1	E1	
0	0	0	Disabled	------	------	------
0	0	1	Transmit	3	10	32/32
0	1	0	Receive	3	10	32/32
0	1	1	Receive	3	10	64/64
1	0	0	Disabled	------	------	--------
1	0	1	Transmit	3	1.5	32/64
1	1	0	Receive	3	1.5	32/64
1	1	1	Receive	3	1.5	64/64

NOTE: *These pins are internally pulled "Low" with 50kΩ resistors.*

CLOCK SYNTHESIZER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
MCLKE1	13	I	**E1 Master Clock Input** This input signal is an independent 2.048MHz clock for E1 system with required accuracy of better than ±50ppm and a duty cycle of 40% to 60%. MCLKE1 is used in the E1 mode. Its function is to provide internal timing for the PLL clock recovery circuit, transmit pulse shaping, jitter attenuator block, reference clock during transmit all ones data and timing reference for the microprocessor in **Host** mode operation. MCLKE1 is also input to a programmable frequency synthesizer that under the control of the CLKSEL[2:0] inputs can be used to generate a master clock from an accurate external source. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. ***NOTES:*** 1. *See pin descriptions for pins CLKSEL[2:0].* 2. *Internally pulled "Low" with a 50kΩ resistor.*

CLOCK SYNTHESIZER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
MCLKT1	14	**I**	**T1 Master Clock Input** This signal is an independent 1.544MHz clock for T1 systems with required accuracy of better than ±50ppm and duty cycle of 40% to 60%. MCLKT1 input is used in the T1 mode. ***NOTES:*** *1. See MCLKE1 description for further explanation for the usage of this pin.* *2. Internally pulled "Low" with a 50kΩ resistor.*
MCLKOUT	16	**O**	**Synthesized Master Clock Output** This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based on the mode of operation.
CLKSEL2 **CLKSEL1** **CLKSEL0**	17 18 19	**I**	**Clock Select input for Master Clock Synthesizer pin 2** **Clock Select input for Master Clock Synthesizer pin 1** **Clock Select input for Master Clock Synthesizer pin 0** In **Hardware** mode, CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the following table. The MCLKRATE control signal is generated from the state of EQC[4:0] inputs. See **Table 5** for description of Transmit Equalizer Control bits. In **Host** mode, the state of these pins are ignored and the master frequency PLL is controlled by the corresponding interface bits.

MCLKE1 (kHz)	MCLKT1 (kHz)	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	CLKOUT (KHz)
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544
8	X	0	1	0	0	2048
8	X	0	1	0	1	1544
16	X	0	1	1	0	2048
16	X	0	1	1	1	1544
56	X	1	0	0	0	2048
56	X	1	0	0	1	1544
64	X	1	0	1	0	2048
64	X	1	0	1	1	1544
128	X	1	1	0	0	2048
128	X	1	1	0	1	1544
256	X	1	1	1	0	2048
256	X	1	1	1	1	1544

NOTE: *Internally pulled "Low" with a 50kΩ resistor.*

REDUNDANCY SUPPORT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
DMO	11	**O**	**Driver Failure Monitor** This pin transitions "High" if a short circuit condition is detected in the transmit driver, or no transmit output pulse is detected for more than 128 TCLK cycles.

TERMINATIONS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
GAUGE	49	**I**	**Twisted Pair Cable Wire Gauge Select** In **Hardware** mode, connect this pin "High" to select 26 Gauge wire. Connect this pin “Low” to select 22 and 24 gauge wire. ***NOTE:*** *Internally pulled “Low” with a 50kΩ resistor.*
TRATIO	26	**I**	**Transmitter Transformer Ratio Select** In external termination mode, setting this pin "High" selects a transformer ratio of 1:2 for the transmitter. A "Low" on this pin sets the transmitter transformer ratio to 1:2.45. In the internal termination mode the transmitter transformer ratio is permanently set to 1:2 and the state of this pin is ignored. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
RXTSEL	44	**I**	**Receiver Termination Select** In **Hardware** mode when this pin is “Low” the receive line termination is determined only by the external resistor. When “High”, the receive termination is realized by internal resistors or the combination of internal and external resistors according to RXRES[1:0]. These conditions are described in the following table: **RXTSEL** / **RX Termination** **0** / **External** **1** / **Internal** ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TXTSEL	45	**I**	**Transmit Termination Select** In **Hardware** mode when this pin is “Low” the transmit line termination is determined only by external resistor. When “High”, the transmit termination is realized only by an internal resistor. These conditions are summarized in the following table: **TXTSEL** / **TX Termination** **0** / **External** **1** / **Internal** ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*

TERMINATIONS

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>TERSEL1
TERSEL0</td><td>43
42</td><td>I</td><td>Termination Impedance Select pin 1
Termination Impedance Select pin 0
In the Hardware mode and in the Internal Termination mode (TXTSEL="1" and/or RXTSEL="1") TERSEL[1:0] control the transmit and receive termination impedance according to the following table:

<table>
<tr><th>TERSEL1</th><th>TERSEL0</th><th>Termination</th></tr>
<tr><td>0</td><td>0</td><td>100Ω</td></tr>
<tr><td>0</td><td>1</td><td>110Ω</td></tr>
<tr><td>1</td><td>0</td><td>75 Ω</td></tr>
<tr><td>1</td><td>1</td><td>120Ω</td></tr>
</table>

In the Internal Termination mode, the receive termination is realized completely by internal resistors or the combination of internal and one fixed external resistor (see description for RXRES[1:0] pins). In the internal termination mode the transformer ratio of 1:2 and 2:1 is required for the transmitter and receiver respectively with the transmitter output AC coupled to the transformer.
NOTE: This pin is internally pulled "Low" with a 50kΩ resistor.</td></tr>
<tr><td>RXRES1
RXRES0</td><td>51
52</td><td>I</td><td>Receive External Resistor Control pin 1
Receive External Resistor Control pin 0
In Hardware mode, RXRES[1:0] pins selects the required value of the external fixed resistor for the receiver according to the following table. This mode is only available in the internal impedance mode by pulling RXTSEL “High”.

<table>
<tr><th>RXRES1</th><th>RXRES0</th><th>RX Fixed Resistor</th></tr>
<tr><td>0</td><td>0</td><td>No External Fixed Resistor</td></tr>
<tr><td>0</td><td>1</td><td>240Ω</td></tr>
<tr><td>1</td><td>0</td><td>210Ω</td></tr>
<tr><td>1</td><td>1</td><td>150Ω</td></tr>
</table>

NOTE: Internally pulled “Low” with 50kΩ resistor.</td></tr>
</table>

CONTROL FUNCTION

<table>
<tr><td>RESET</td><td>41</td><td>I</td><td>Hardware Reset (Active "Low")
When this pin is tied “Low” for more than 10µs, the device is put in the reset state.
Pulling RESET “Low” while the ICT pin is also “Low” will put the chip in factory test mode. This condition should never happen during normal operation.
NOTE: Internally pulled “High” with a 50kΩ resistor.</td></tr>
<tr><td>SR/DR</td><td>28</td><td>I</td><td>Single-Rail/Dual-Rail Data Format
In Hardware mode, connect this pin "Low" to select transmit and receive data format in dual-rail mode. In this mode, HDB3 or B8ZS encoder and decoder are not available.
Connect this pin "High" to select single-rail data format.
NOTE: Internally pulled "Low" with a 50kΩ resistor.</td></tr>
<tr><td>LOOP1
LOOP0</td><td>29
30</td><td>I</td><td>Loop-back Control pin 1
Loop-back Control pin 0
In Hardware mode, LOOP[1:0] pins are used to control the Loop-back functions according to the following table:
<table>
<tr><th>LOOP1</th><th>LOOP0</th><th>MODE</th></tr>
<tr><td>0</td><td>0</td><td>Normal Mode</td></tr>
<tr><td>0</td><td>1</td><td>Local Loop-Back</td></tr>
<tr><td>1</td><td>0</td><td>Remote Loop-Bac</td></tr>
<tr><td>1</td><td>1</td><td>Digital Loop-Back</td></tr>
</table>
NOTE: Internally pulled "Low" with a 50kΩ resistor.</td></tr>
<tr><td>EQC4

SDI</td><td>21</td><td>I</td><td>Equalizer Control Input pin 4
In Hardware mode, this pin together with EQC[3:0] are used for controlling the transmit pulse shaping, transmit line build-out (LBO), receive monitoring and also to select T1, E1 or J1 modes of operation. See Table 5 for description of Transmit Equalizer Control bits.

Serial Data Input
Host mode, SEE”SERIAL INTERFACE” ON PAGE 5.</td></tr>
<tr><td>EQC3

SDO</td><td>22</td><td>I

O</td><td>Equalizer Control Input pin 3
See EQC4/SDI description for further explanation for the usage of this pin.
Serial Data Output
Host mode, SEE”SERIAL INTERFACE” ON PAGE 5.</td></tr>
<tr><td>EQC2

SCLK</td><td>23</td><td>I</td><td>Equalizer Control Input pin 2
See EQC4/SDI description for further explanation for the usage of this pin.
Serial Interface Clock Input
Host mode, SEE”SERIAL INTERFACE” ON PAGE 5.</td></tr>
</table>

CONTROL FUNCTION

EQC1 **$\overline{CS}$**	24	**I**	**Equalizer Control Input pin 1** See EQC4/SDI description for further explanation for the usage of this pin. **Chip Select Input** **Host** mode, **SEE"SERIAL INTERFACE" ON PAGE 5.**
EQC0 **$\overline{INT}$**	25	**I** **O**	**Equalizer Control Input pin 0** See EQC4/SDI description for further explanation for the usage of this pin. **Interrupt Output** **Host** mode, **SEE"SERIAL INTERFACE" ON PAGE 5.**

ALARM FUNCTION/OTHER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
ATAOS	27	**I**	**Automatic Transmit "All Ones" Pattern** In **Hardware** mode, a "High" level on this pin enables the automatic transmission of an "All Ones" AMI pattern from the transmitter when the receiver has detected an LOS condition. A "Low" level on this pin disables this function. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
$\overline{ICT}$	59	**I**	**In-Circuit Testing (active "Low")** When this pin is tied "Low", all output pins are forced to a "High" impedance state for in-circuit testing. Pulling $\overline{RESET}$ "Low" while $\overline{ICT}$ pin is also "Low" will put the chip in factory test mode. This condition should never happen during normal operation. ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*

ALARM FUNCTION/OTHER

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>NLCDE1
NLCDE0</td><td>33
34</td><td>I</td><td>Network Loop Code Detection Enable pin 1
Network Loop Code Detection Enable pin 0
NLCDE[1:0] pins are used to control the Loop-Code detection according to the following table:

<table>
<tr><th>NLCDE1</th><th>NLCDE0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Disable Loop-Code Detection</td></tr>
<tr><td>0</td><td>1</td><td>Detect Loop-Up Code in Receive Data</td></tr>
<tr><td>1</td><td>0</td><td>Detect Loop-Down Code in Receive Data</td></tr>
<tr><td>1</td><td>1</td><td>Automatic Loop-Code Detection</td></tr>
</table>

When NLCDE1=”0” and NCLDE0=”1”, or NLCDE1=”1” and NLCDE0=”0”, the chip is manually programed to monitor the receive data for the Loop-Up or Loop-Down code respectively. When the presence of the “00001” or “001” pattern is detected for more than 5 seconds, the NLCD pin is set to “1” and the host has the option to activate the loop-back function manually.

Setting the NLCDE1=”1” and NLCDE0=”1” enables the Automatic Loop-Code detection and Remote-Loop-Back activation mode. As this mode is initiated, the state of the NLCD pin is reset to “0” and the chip is programmed to monitor the receive data for the Loop-Up Code. If the “00001” pattern is detected for longer than 5 seconds, the NLCD pin is set to “1”, Remote Loop-Back is activated and the chip is automatically programed to monitor the receive data for the Loop-Down code. The NLCD pin stays “High” even after the chip stops receiving the Loop-Up code. The remote Loop-Back condition is removed when the chip receives the Loop-Down code for more than 5 seconds or if the Automatic Loop-Code detection mode is terminated.</td></tr>
<tr><td>INSBPV</td><td>35</td><td>I</td><td>Insert Bipolar Violation
When this pin transitions from "0" to "1", a bipolar violation is inserted in the transmitted data stream. Bipolar violation can be inserted either in the QRSS pattern, or input data when operating in single-rail mode. The state of this pin is sampled on the rising edge of TCLK.
NOTE: To ensure the insertion of a bipolar violation, this pin should be reset to a "0" prior to setting to a "1".</td></tr>
</table>

ALARM FUNCTION/OTHER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
NLCD	38	**O**	**Network Loop-Code Detection Output pin** This pin operates differently in the Manual or the Automatic Network Loop-Code detection modes. In the Manual Loop-Code detection mode (NLCDE1 ="0" and NLCDE0 ="1", or NLCDE1 ="1" and NLCDE0 ="0") this pin gets set to "1" as soon as the Loop-Up ("00001") or Loop-Down ("001") code is detected in the receive data for longer than 5 seconds. The NLCD pin stays in the "1" state for as long as the chip detects the presence of the Loop-Code in the receive data and it is reset to "0" as soon as it stops receiving it. When the Automatic Loop-Code detection mode (NLCDE1 ="1" and NLCDE0 ="1") is initiated, the NLCD output pin is reset to "0" and the chip is programmed to monitor the receive input data for the Loop-Up Code. The NLCD pin is set to a "1" to indicate that the Network Loop Code is detected for more than 5 seconds. Simultaneously the Remote Loop-Back condition is automatically activated and the chip is programmed to monitor the receive data for the Network Loop-Down Code. The NLCD pin stays in the "1" state for as long as the Remote Loop-Back condition is in effect even if the chip stops receiving the Loop-Up Code. Remote Loop-Back is removed if the chip detects the "001" pattern for longer than 5 seconds in the receive data. Detecting the "001" pattern also results in resetting the NLCD output pin.
AISD	39	**O**	**Alarm Indication Signal Detect Output pin** This pin is set to "1" to indicate that an All Ones Signal is detected by the receiver. The value of this pin is based on the current status of Alarm Indication Signal detector.
QRPD	40	**O**	**Quasi-random Pattern Detection Output pin** This pin is set to "1" to indicate that the receiver is currently in synchronization with the QRSS pattern. The value of this pin is based on the current status of Quasi-random pattern detector.

POWER AND GROUND

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TAGND	7	****	**Transmitter Analog Ground**
TAVDD	9	****	**Transmitter Analog Positive Supply (3.3V ± 5%)**
RAGND	6	****	**Receiver Analog Ground**
RAVDD	3	****	**Receiver Analog Positive Supply (3.3V± 5%)**
VDDPLL	12	****	**Analog Positive Supply for Master Clock Synthesizer PLL (3.3V± 5%)**
GNDPLL	15	****	**Analog Ground for Master Clock Synthesizer PLL**
DVDD	36	****	**Digital Positive Supply (3.3V± 5%)**
AVDD	31	****	**Analog Positive Supply (3.3V± 5%)**
DGND	37	****	**Digital Ground**
AGND	32	****	**Analog Ground**

FUNCTIONAL DESCRIPTION

The XRT83L30 is a fully integrated single channel long-haul and short-haul transceiver intended for T1, J1 or E1 systems. Simplified block diagrams of the device are shown in Figure 1, **Host** mode and Figure 2, **Hardware** mode. The XRT83L30 can receive signals that have been attenuated from 0 to 36dB at 772kHz (0 to 6000 feet cable loss) for T1 and from 0 to 43dB at 1024kHz for E1 systems.

In T1 applications, the XRT83L30 can generate five transmit pulse shapes to meet the short-haul Digital Cross-connect (DSX-1) template requirement as well as four CSU Line Build-Out (LBO) filters of 0dB, -7.5dB, -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit output pulse generator that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions. The operation and configuration of the XRT83L30 can be controlled through a serial microprocessor **Host** interface or, by **Hardware** control.

MASTER CLOCK GENERATOR

Using a variety of external clock sources, the on-chip frequency synthesizer generates the T1 (1.544MHz) or E1 (2.048MHz) master clocks necessary for the transmit pulse shaping and receive clock recovery circuit.

There are two master clock inputs MCLKE1 and MCLKT1. In systems where both T1 and E1 master clocks are available these clocks can be connected to the respective pins.

In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. T1 or E1 master clocks can be generated from 8kHz, 16kHz, 56kHz, 64kHz, 128kHz and 256kHz external clocks under the control of CLKSEL[2:0] inputs according to Table 1.

NOTE: *EQC[4:0] determine the T1/E1 operating mode. See* Table 5 *for details.*

FIGURE 4. TWO INPUT CLOCK SOURCE

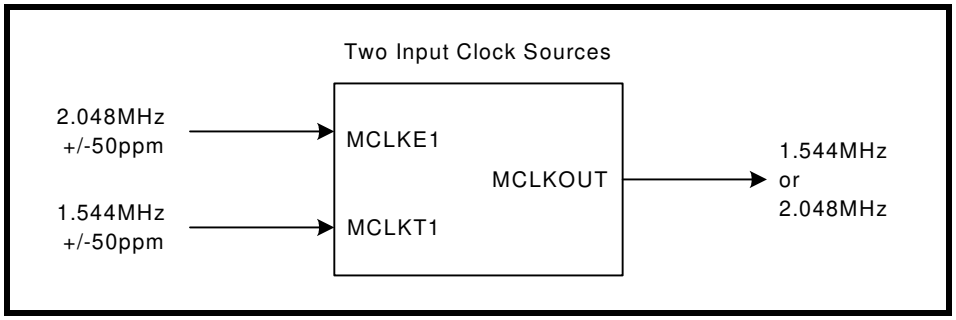


FIGURE 5. ONE INPUT CLOCK SOURCE

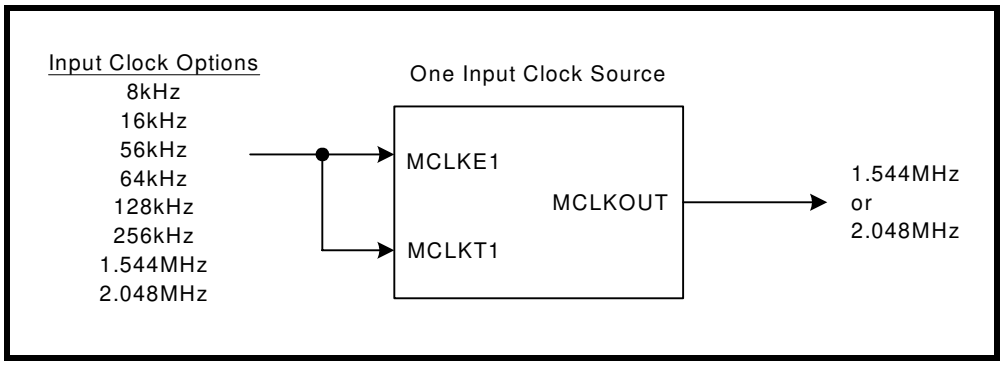


TABLE 1: MASTER CLOCK GENERATOR

MCLKE1 kHz	MCLKT1 kHz	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	MASTER CLOCK kHz
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544
8	x	0	1	0	0	2048
8	x	0	1	0	1	1544
16	x	0	1	1	0	2048
16	x	0	1	1	1	1544
56	x	1	0	0	0	2048
56	x	1	0	0	1	1544
64	x	1	0	1	0	2048
64	x	1	0	1	1	1544
128	x	1	1	0	0	2048
128	x	1	1	0	1	1544
256	x	1	1	1	0	2048
256	x	1	1	1	1	1544

In **Host** mode the programming is achieved through the corresponding interface control bits, the state of the CLKSEL[2:0] control bits and the state of the MCLKRATE interface control bit.

RECEIVER

RECEIVER INPUT

At the receiver input, a cable attenuated AMI signal can be coupled to the receiver through a capacitor or a 1:1 transformer. The input signal is first applied to a selective equalizer for signal conditioning. The maximum equalizer gain is up to 36dB for T1 and 43dB for E1 modes. The equalized signal is subsequently applied to a peak detector which in turn controls the equalizer settings and the data slicer. The slicer threshold for both E1 and T1 is typically set at 50% of the peak amplitude at the equalizer output. After the slicers, the digital representation of the AMI signals are applied to the clock and data recovery circuit. The recovered data subsequently goes through the jitter attenuator and decoder (if selected) for HDB3 or B8ZS decoding before being applied to the RPOS/RDATA and RNEG/LCV pins. Clock recovery is accomplished by a digital phase-locked loop (DPLL) which does not require any external components and can tolerate high levels of input jitter that meets or exceeds the ITU-G.823 and TR-TSY000499 standards.

In **Hardware** mode only, this receive channel is turned on upon power-up and is always on. In **Host** mode, the receiver can be turned on or off with the RXON bit. **SEE"MICROPROCESSOR REGISTER #2 BIT DESCRIPTION" ON PAGE 48.**

RECEIVE MONITOR MODE

In applications where Monitor mode is desired, the equalizer can be configured in a gain mode which handles input signals attenuated resistively up to 29dB, along with 0 to 6dB cable attenuation for both T1 and E1 applications, refer to **Table 5** for details. This feature is available in both **Hardware** and **Host** modes.

RECEIVER LOSS OF SIGNAL (RLOS)

For compatibility with ITU G.775 requirements, the RLOS monitoring function is implemented using both analog and digital detection schemes. If the analog RLOS condition occurs, a digital detector is activated to count for 32 consecutive zeros in E1 (4096 bits in Extended Los mode, EXLOS = "1") or 175 consecutive zeros in T1 before RLOS is asserted. RLOS is cleared when the input signal rises +3dB (built in hysteresis) above the point at which it was declared and meets 12.5% ones density of 4 ones in a 32 bit window, with no more than 16 consecutive zeros for E1. In T1 mode, RLOS is cleared when the input signal rises +3dB (built in hysteresis) above the point at which it was declared and contains 16 ones in a 128 bit window with no more than 100 consecutive zeros in the data stream. When loss of signal occurs, RLOS register indication and register status will change. If the RLOS register enable is set high (enabled), the alarm will trigger an interrupt causing the interrupt pin ($\overline{INT}$) to go low. Once the alarm status register has been read, it will automatically reset upon read (RUR), and the $\overline{INT}$ pin will return high.

Analog RLOS

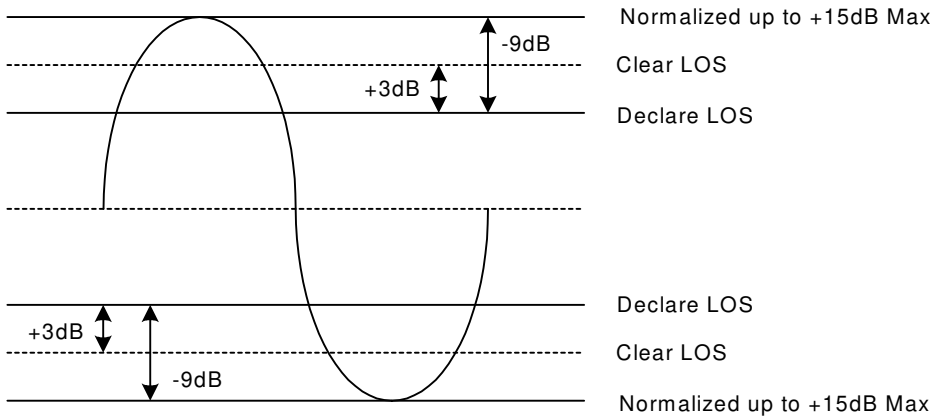
Setting the Receiver Input to -15dB T1/E1 Short Haul Mode

By setting the receiver input to -15dB T1/E1 short haul mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +15dB normalizing the T1/E1 input signal.

NOTE: *This setting refers to cable loss (frequency), not flat loss (resistive).*

Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+15dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -24dB (-15dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total cable attenuation of -21dB. See **Figure 6** for a simplified diagram.

FIGURE 6. SIMPLIFIED DIAGRAM OF -15dB T1/E1 SHORT HAUL MODE AND RLOS CONDITION



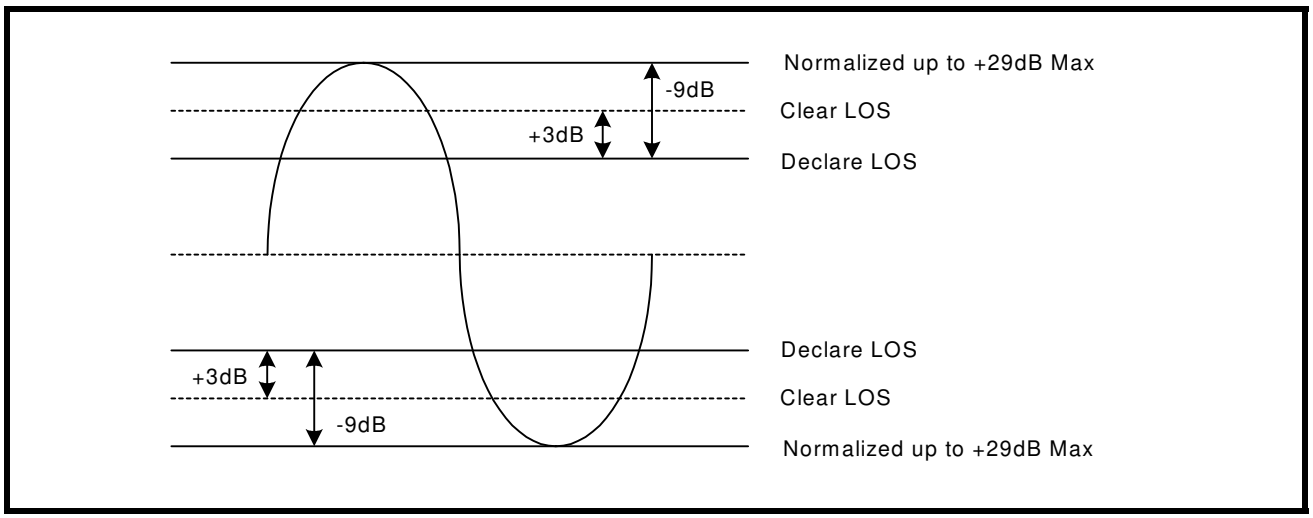
Setting the Receiver Input to -29dB T1/E1 Gain Mode

By setting the receiver input to -29dB T1/E1 gain mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +29dB normalizing the T1/E1 input signal.

NOTE: *This is the only setting that refers to flat loss (resistive). All other modes refer to cable loss (frequency).*

Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+29dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -38dB (-29dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total flat loss of -35dB. See **Figure 7** for a simplified diagram.

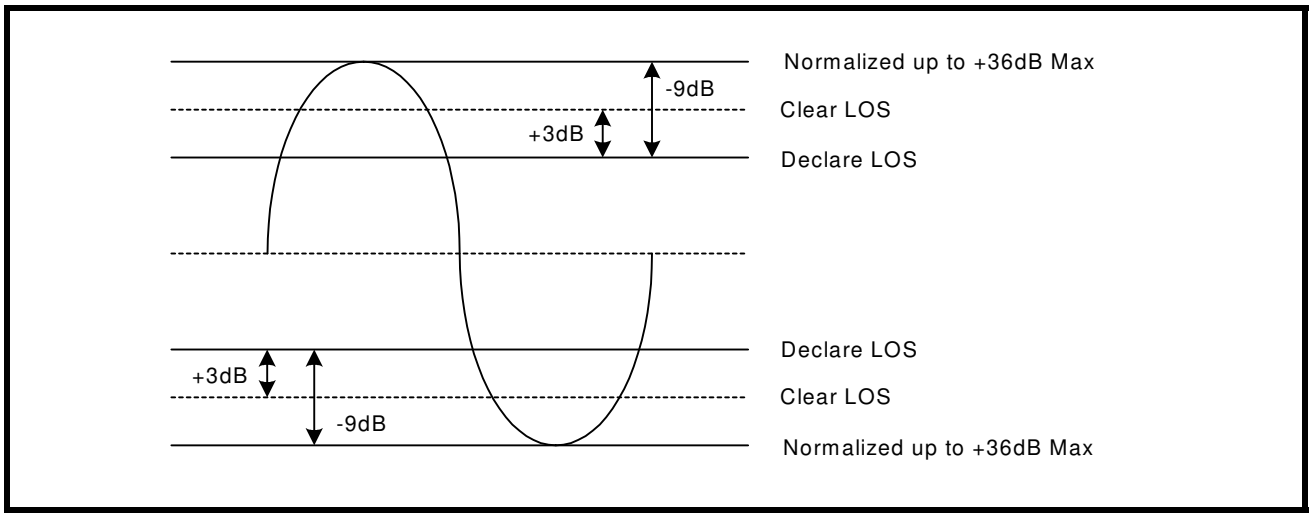
FIGURE 7. SIMPLIFIED DIAGRAM OF -29dB T1/E1 GAIN MODE AND RLOS CONDITION



Setting the Receiver Input to -36dB T1/E1 Long Haul Mode

By setting the receiver input to -36dB T1/E1 long haul mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +36dB normalizing the T1 input signal. This setting refers to cable loss (frequency), not flat loss (resistive). Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+36dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -45dB (-36dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total cable attenuation of -42dB. See **Figure 8** for a simplified diagram.

FIGURE 8. SIMPLIFIED DIAGRAM OF -36dB T1/E1 LONG HAUL MODE AND RLOS CONDITION



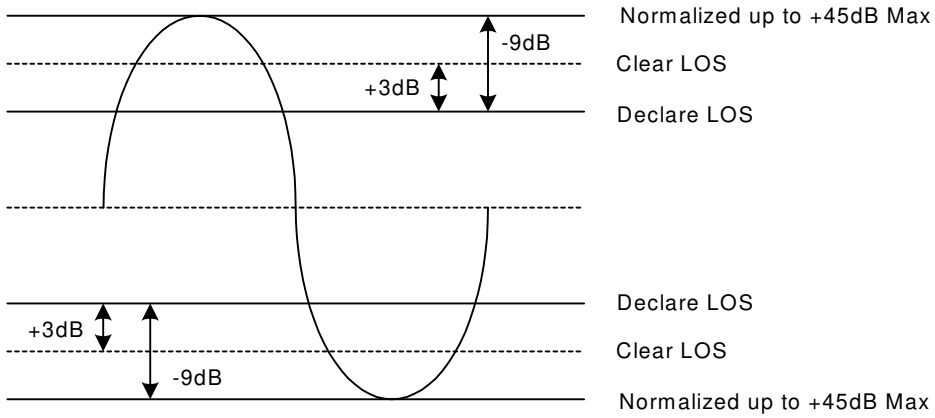
E1 Extended RLOS

E1: Setting the Receiver Input to Extended RLOS

By setting the receiver input to extended RLOS, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +43dB normalizing the E1 input signal. This setting refers to

cable loss (frequency), not flat loss (resistive). Once the E1 input signal has been normalized to 0dB by adding the maximum gain (+43dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -52dB (-43dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total cable attenuation of -49dB. See **Figure 9** for a simplified diagram.

FIGURE 9. SIMPLIFIED DIAGRAM OF EXTENDED RLOS MODE (E1 ONLY)



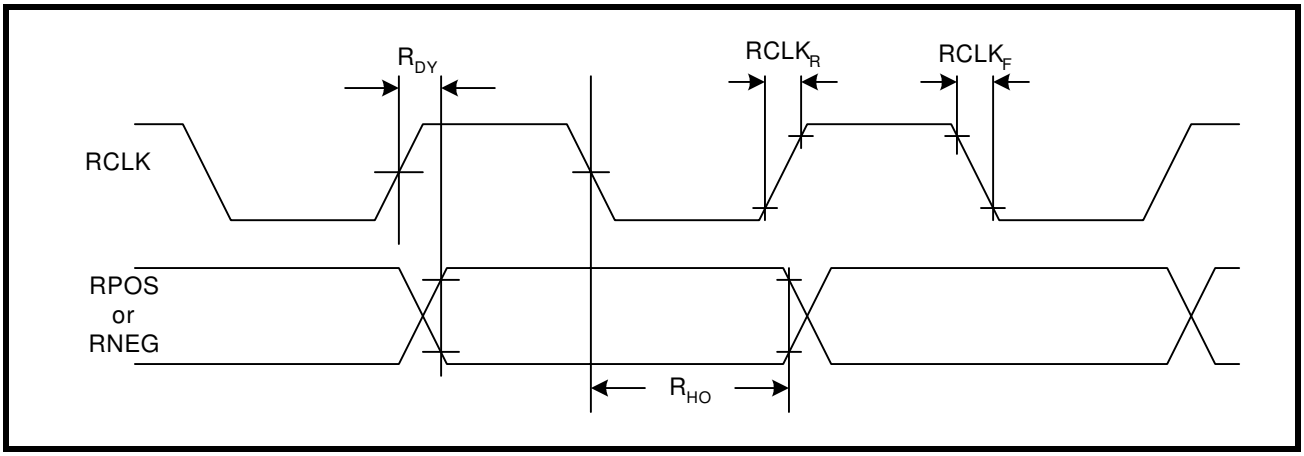
RECEIVE HDB3/B8ZS DECODER

The Decoder function is available in both **Hardware** and **Host** modes by controlling the TNEG/CODE pin or the CODE interface bit. The decoder function is only active in single-rail Mode. When selected, receive data in this mode will be decoded according to HDB3 rules for E1 and B8ZS for T1 systems. Bipolar violations that do not conform to the coding scheme will be reported as Line Code Violation at the RNEG/LCV pin. The length of the LCV pulse is one RCLK cycle for each code violation. Excessive number of zeros in the receive data stream is also reported as an error at the same output pin. If AMI decoding is selected in single rail mode, every bipolar violation in the receive data stream will be reported as an error at the RNEG/LCV pin.

RECOVERED CLOCK (RCLK) SAMPLING EDGE

This feature is available in both **Hardware** and **Host** modes. In **Host** mode, the sampling edge of RCLK output can be changed through the interface control bit RCLKE. If a “1” is written in the RCLKE interface bit, receive data output at RPOS/RDATA and RNEG/LCV are updated on the falling edge of RCLK. Writing a “0” to the RCLKE register, updates the receive data on the rising edge of RCLK. In **Hardware** mode the same feature is available under the control of the RCLKE pin.

FIGURE 10. RECEIVE CLOCK AND OUTPUT DATA TIMING



JITTER ATTENUATOR

To reduce phase and frequency jitter in the recovered clock, the jitter attenuator can be placed in the receive signal path. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth that can vary between 2x32 and 2x64. The jitter attenuator can also be placed in the transmit signal path or disabled altogether depending upon system requirements. The jitter attenuator, other than using the master clock as reference, requires no external components. With the jitter attenuator selected, the typical throughput delay from input to output is 16 bits for 32 bit FIFO size or 32 bits for 64 bit FIFO size. When the read and write pointers of the FIFO in the jitter attenuator are within two bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this situation occurs, the jitter attenuator will not attenuate input jitter until the read/write pointer's position is outside the two bits window. Under normal condition, the jitter transfer characteristic meets the narrow bandwidth requirement as specified in ITU- G.736, ITU- I.431 and AT&T Pub 62411 standards.

In T1 mode the Jitter Attenuator Bandwidth is always set to 3Hz. In E1 mode, the bandwidth can be reduced through the JABW control signal. When JABW is set “High” the bandwidth of the jitter attenuator is reduced from 10Hz to 1.5Hz. Under this condition the FIFO length is automatically set to 64 bits and the 32 bits FIFO length will not be available in this mode.

GAPPED CLOCK (JA MUST BE ENABLED IN THE TRANSMIT PATH)

The XRT83L30 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to T1 or E1 data, stuffing bits are removed which can leave gaps in the incoming data stream. If the jitter attenuator is enabled in the transmit path, the 32-Bit or 64-Bit FIFO is used to smooth the gapped clock into a steady T1 or E1 output. The maximum gap width is shown in **Table 2**.

TABLE 2: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the jitter attenuator should be enabled in the receive path.*