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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

FEBRUARY 2005

GENERAL DESCRIPTION

The XRT83L34 is a fully integrated Quad (four channel) long-haul and short-haul line interface unit for T1 (1.544Mbps) 100 Ω , E1 (2.048Mbps) 75 Ω or 120 Ω , or J1 110 Ω applications.

In long-haul applications the XRT83L34 accepts signals that have been attenuated from 0 to 36dB at 772kHz in T1 mode (equivalent of 0 to 6000 feet of cable loss) or 0 to 43dB at 1024kHz in E1 mode.

In T1 applications, the XRT83L34 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83L34 provides both a parallel Host microprocessor interface as well as a Hardware mode for programming and control.

Both the B8ZS and HDB3 encoding and decoding functions are selectable as well as AMI. An on-chip

crystal-less jitter attenuator with a 32 or 64 bit FIFO can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L34 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75 Ω , 100 Ω , 110 Ω and 120 Ω for both transmitter and receiver. In the absence of the power supply, the transmit outputs and receive inputs are tri-stated allowing for redundancy applications The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

Features (See Page 2)



FIGURE 1. BLOCK DIAGRAM OF THE XRT83L34 T1/E1/J1 LIU (HOST MODE)

REV. 1.0.1



FIGURE 2. BLOCK DIAGRAM OF THE XRT83L34 T1/E1/J1 LIU (HARDWARE MODE)

FEATURES

- Fully integrated four channel long-haul or short-haul transceivers for E1,T1 or J1 applications
- Adaptive Receive Equalizer for up to 36dB cable attenuation
- Programable Transmit Pulse Shaper for E1,T1 or J1 short-haul interfaces
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping that can be used for both T1 and E1 modes.
- Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps
- Selectable receiver sensitivity from 0 to 36dB cable loss for T1 @772kHz and 0 to 43dB for E1 @1024kHz
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for E1 and 0 to 3dB of cable attenuation for T1 modes
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications
- Internal and/or external impedance matching for 75 Ω , 100 Ω , 110 Ω and 120 Ω
- Tri-State transmit output and receive input capability for redundancy applications
- Provides High Impedance for Tx and Rx during power off
- Transmit return loss meets or exceeds ETSI 300-166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- High receiver interference immunity
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder functions
- QRSS pattern generator and detection for testing and monitoring

XRT83L34 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Local Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both Hardware and Host (parallel Microprocessor) interface for programming
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Single 3.3V Supply Operation
- 128 pin TQFP package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	Package	OPERATING TEMPERATURE RANGE
XRT83L34IV	128 Lead TQFP (14 x 20 x 1.4mm)	-40°C to +85°C



XRT83L34

TCLK_0 TPOS_0/TDATA_0 RLOS_0 RLOS_0 RNDE RNDC_0/CVC0 RND_0 RTIP_0 RTIP_0 RTIP_0 TTIP_0 TTIP_0 TTIP_0 TTIP_1 TTIP_1 RRING_1 TTIP_1 RRING_1 TTIP_1 RRING_1 TTIP_1 RRING_1 TTIP_1 RRING_1 TTIP_1 RRING_1 RRING_1

. 64

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62 61 60

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58 57 56

55 54

47 46

45 44 43

42 41

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DMO_0

A[0]/EQC0 A[1]/EQC1

• A[2]/EQC2

AI31/EQC3

A[4]/EQC4

DGND

DGND

DVDD

DVDD uPCLK/ATAOS
D[0]/LOOP0_3
D[1]/LOOP1_3

D[2]/LOOP0_2 D[3]/LOOP1_2

D[4]/LOOP0_1

D[5]/LOOP1 1

D[6]/LOOP0_0

D[7]/LOOP1_0

AGND

CLKSEL2

AVDD

A[5]/JASEL0 A[6]/JASEL1

TCLK_2 TPOS_2/TDATA_2

TNEG_2/CODES_2

uPTS1/RCLKE

uPTS2/TCLKE RXRES0

RXRES1

BXTSEL TXTSEL

TERSEL1

TERSEL0

GND

DVDD

DVDD

DGND

DGND INT/TRATIO

ICT RESET

TXON_0

TXON 1

TXON_2

TXON_3

TCLK_1

TNEG 1/CODES 1

TPOS_1/TDATA_1

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QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

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XRT83L34 **EXAR** *Rev. 1.0.1* QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

PIN DESCRIPTION BY FUNCTION

RECEIVE SECTIONS

SIGNAL NAME	Pin #	Түре	DESCRIPTION
RLOS_0 RLOS_1 RLOS_2 RLOS_3	4 28 75 99	0	Receiver LOS (Loss of Signal) Defect Indicator Output for Channel _n This output pin indicates whether or not the Receive Section associated with Channel n (within the LIU device) is declaring the LOS defect condition, as depicted below. LOGIC LOW - Indicates that this particular channel is currently not declaring the LOS defect condition. LOGIC HIGH - Indicates that this particular channel is currently declaring the LOS defect condition. See "Receiver Loss of Signal (RLOS)" on page 28.
RCLK_0 RCLK_1 RCLK_2 RCLK_3	5 27 76 98	0	Receiver Clock Output for Channel _n The Receive Section (of a given channel within the XRT83L34 device) will update the RPOS_n and RNEG_n/LCV_n output pins upon either the rising or falling edge of this output clock signal (depending upon user configura- tion).
RNEG_0/ LCV_0 RNEG_1/ LCV_1 RNEG_2/ LCV_2 RNEG_3/ LCV_3	6 26 77 97	0	 Receiver Negative-Polarity Data Output/Line Code Violation Indicator Output - Channel n: The exact function of this output pin depends upon whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual-Rail Mode, as described below. Dual-Rail Mode Operation - Receive Negative-Polarity Data Output - RNEG_n: The Receive Section of Channel n will output the negative-polarity portion of the recovered incoming DS1/E1 data (from the remote terminal equipment) via this output pin. Each channel (within the XRT83L34 device) will update this incoming DS1/E1 data upon the "user-selected" edge of the RCLK_n output signal. The "Positive-Polarity Portion" of the recovered incoming DS1/E1 data will be output via the RPOS_n output pin. Single-Rail Mode Operation - Line Code Violation Indicator Output - LCV_n: The Receive Section of Channel n will pulse this output pin "high" (for one RCLK_n period) each time it detects a Line Code Violation within the incom- ing DS1/E1 line signal. Each channel (within the XRT83L34 device) will update this output pin upon the "user-selected" edge of the RCLK_n output signal.

XRT83L34 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

SIGNAL NAME	PIN #	Түре	DESCRIPTION
RPOS_0/ RDATA_0 RPOS_1/ RDATA_1 RPOS_2/ RDATA_2 RPOS_3/ RDATA_3	7 25 78 96	0	Receiver Positive-Polarity Data Output/Receive Data Output - Channel n: The exact function of this output pin depends upon whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual-Rail Mode as described below. Dual-Rail Mode Operation - Receive Positive-Polarity Data Output Pin - RPOS_n: The Receive Section of Channel n will output the positive-polarity portion of the Recovered incoming DS1/E1 data (from the remote terminal equipment) via this output pin. Each Channel (within the XRT83L34 device) will update the data (that is output via this output pin) upon the "user-selected" edge of the RCLK_n output clock signal. The "Negative-Portion" of this recovered incoming DS1/E1 data (from the
			remote terminal equipment) will be output via the corresponding RNEG_n output pin. Single-Rail Mode Operation - Receive Data Output Pin - RDATA_n If Channel n has been configured to operate in the Single-Rail Mode, then the entire incoming DS1/E1 data (that has been recovered by the Receive Section of Channel n) will be output via this output pin upon the "user- selected" edge of the RCLK_n output clock signal.
RTIP_0 RTIP_1 RTIP_2 RTIP_3	9 23 80 94	Ι	Receiver Differential Tip Positive Input for Channel _n: This input pin, along with the corresponding RRING_n input pin functions as the "Receive DS1/E1 Line Signal" for Channel n, within the XRT83L34 device. The user is expected to connect this signal and the corresponding RRING_n input signal to a 1:1 transformer. Whenever the RTIP_n/RRING_n input pins are receiving a positive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "higher-voltage" than that of the corresponding RRING_n input pin. Conversely, whenever the RTIP_n/RRING_n input pins are receiving a nega- tive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "lower-voltage" than that of the corresponding RRING_n input pin.
RRING_0 RRING_1 RRING_2 RRING_3	10 22 81 93	I	Receiver Differential Ring Negative Input for Channel _n: This input pin, along with the corresponding RTIP_n input pin functions as the "Receive DS1/E1 Line Signal" for Channel n, within the XRT83L34 device. The user is expected to connect this signal and the corresponding RTIP_n input signal to a 1:1 transformer. Whenever the RTIP_n/RRING_n input pins are receiving a positive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "lower-voltage" than that of the corresponding RTIP_n input pin. Conversely, whenever the RTIP_n/RRING_n input pins are receiving a nega- tive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "higher-voltage" than that of the corresponding RTIP_n input pin.

XRT83L34 **EXAR** *REV. 1.0.1* QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

SIGNAL NAME	Pin #	Түре	DESCRIPTION
RXMUTE	73	I	Receive Muting upon LOS Command Input/READY or DTACK Output: The exact function of this Input/Output pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.
			Hardware Mode Operation - Receive Muting upon LOS Command Input pin: This input pin permits the user to enable or disable the "Muting upon LOS" feature within the XRT83L34 device. If the user enables the "Muting upon LOS" feature, then the Receive Section of each channel (within the XRT83L34 device) will automatically MUTE their own RPOS_n/RNEG_n out- put pins (e.g., force to ground) for the duration that they are declaring the LOS defect condition, as described below.
			LOW - Disables the "Muting upon LOS" feature for all four (4) HIGH - Enables the "Muting upon LOS" feature. <i>Notes:</i>
			 Internally pulled "Low" with 50kΩ resistor. In Hardware mode, all receive channels share the same RXMUTE control function.
RDY_DTACK	73	0	HOST Mode Operation - Ready or DTACK Output See "Ready or DTACK Output/Receive Muting upon LOS Command Input pin:" on page 16.

XRT83L34

QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

SIGNAL NAME	Pin #	Түре			D	ESCRIPTION	
RXRES0 RXRES1	108 109	I	Receive E Receive E Receive E These pins resistor acc	xternal Res xternal Res xternal Res are used to cording to th	sistor Cont sistor Cont sistor Cont o determine ne following	rol Pins - Hardware mode rol Pin 0 rol Pin 1 e the value of the external Receiv table:	ve fixed
				RXRES1	RXRES0	Required Fixed External RX Resistor	
				0	0	No External Fixed Resistor	
				0	1	240Ω	
				1	0	210Ω	
				1	1	150Ω	
			Note: The	ese pins are	internally p	oulled "Low" with 50k Ω resistor.	
RCLKE	106	I	Receive C The exact f device has described b	lock Edge function of t been config pelow.	Select/Mic his input pin gured to op	roprocessor Type Select Input n depends upon whether the XR erate in the HOST or Hardware	t pin: T83L34 Mode, as
μPTS1			RCLKE: This input p channel wit the RPOS_ ing edge of below. LOW - Cor RNEG_n/L HIGH - Cor RNEG_n/L HOST Moo This pin is Type Sele Edge Sele Note: This	bin permits thin the XR ¹ _n/RDATA_u r falling edg figures all f CV_n outpun figures all CV_n outpun de Operation used to sele the ct Input Piset Piset Input Pis	the user to T83L34 dev n and RNE0 e of the RC our channe to pins upor four channe to pins upor four channe to pins upor on - Microp ect the micr ns/Receiv in:" on page	configure the Receive Section (vice) to update the data (that is o G_n/LCV_n output pins) upon eit CLK_n output clock signal, as dep els to update the RPOS_n/RDATA n rising edge of RCLK_n. els to update the RPOS_n/RDATA n the falling edge of RCLK_n. rocessor Type Select Input pin oprocessor type. See "Microprice Clock Edge Select/Transminge 17. d"Low" with a 50kΩ resistor.	pin - of each utput via ther the ris- bicted A_n and A_n and h # 1: bccessor it Clock

XP EXAR REV. 1.0.1 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

TRANSMITTER SECTIONS

SIGNAL NAME	PIN #	Түре	DESCRIPTION
TCLKE μPTS2	107	Ι	Transmit Clock Edge - Hardware ModeWith this pin set to a "High", transmit input data of all channels are sampled at the rising edge of TCLK_n. With this pin tied "Low", input data are sampled at the falling edge of TCLK_n.Microprocessor Type Select Input pin 2 - Host ModeThis pin should be tied to GND. µPTS1(pin 106) selects the microprocessor type. See "Microprocessor Type Select Input Pins/Receive Clock Edge
TTIP_0 TTIP_1 TTIP_2 TTIP_3	13 19 84 90	0	 Transmitter Tip Output for Channel _n: This output pin, along with the corresponding TRING_n output pin, functions as the Transmit DS1/E1 Output signal drivers for the XRT83L34 device. The user is expected to connect this signal and the corresponding TRING_n output signal to a "1:2.45" step-up transformer. Whenever the Transmit Section of (a given channel within the XRT83L34 device) generates and transmits a "positive-polarity" pulse (onto the line), this output pin will be pulsed to a "higher-voltage" than its corresponding TRING_n output pins. Conversely, whenever the Transmit Section (of a given channel within the XRT83L34 device) generates and transmits a "negative-polarity" pulse (onto the line), then this output pin will be pulsed to a "lower-voltage" than that of the TRING_n output pin. Note: This output pin will be tri-stated whenever the user sets the "TxON" input pin (or bit-field) to "0".
TRING_0 TRING_1 TRING_2 TRING_3	15 17 86 88	0	 Transmitter Ring Output for Channel _n: This output pin, along with the corresponding TTIP_n output pin, functions as the Transmit DS1/E1" output signal drivers for the XRT83L34 device. The user is expected to connect this signal and the corresponding TTIP_n output signal to a "1:2.45" step-up transformer. Whenever the Transmit Section (of a given channel, within the XRT83L34 device) generates and transmits a "positive-polarity" pulse (onto the line), this output pin will be pulsed to a "lower-voltage" than its corresponding TTIP_n output pin. Conversely, whenever the Transmit Section (of a given channel, within the XRT83L34 device) generates and transmits a "negative-polarity" pulse (onto the line), this number of the line) this output pin will be pulsed to a "higher-voltage" than that of the TTIP_n output pin. Note: This output pin will be tri-stated whenever the user sets the "TxON" input pin (or bit-field) to "0".

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QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

SIGNAL NAME	PIN #	Түре	DESCRIPTION
TPOS_0/	2	I	Transmit Positive-Polarity Data Input pin/Transmit Data Input pin:
TDATA_0 TPOS_1/ TDATA_1	127		The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual-Mode, as described below.
TPOS_2/	104		Dual-Rail Mode Operation - Transmit Positive-Polarity Data Output - TPOS_n:
TPOS_3/ TDATA_3	101		For Dual-Rail Applications, the System-Side Terminal Equipment should apply the "positive-polarity" portion of the outbound DS1/E1 data-stream to this input pin. Likewise, the System-Side Terminal Equipment should also apply the "negative-polarity" portion of the outbound DS1/E1 data-stream to the TNEG_n input pin.
			The Transmit Section of Channel n will sample this input pin (along with TNEG_n) upon the "user-selected" edge of TCLK_n. The Transmit Section of Channel n will generate a "positive-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic "HIGH" level. The Transmit Section of Channel n will NOT generate a "positive-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic "HIGH" level. The Transmit Section of Channel n will NOT generate a "positive-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic "LOW" level.
			Single-Rail Mode Operation - Transmit Data Output - TDATA_n: For Single-Rail Applications, the System-Side Terminal Equipment should apply the entire "outbound" DS1/E1 data-stream to this input pin. The Trans- mit Section of Channel n will sample this input pin upon the "user-selected" edge of TCLK_n. In the Single-Rail Mode, the internal B8ZS/HDB3 Encoder will be enabled, and the Transmit Section of the Channel will generate and transmit "positive" and "negative-polarity" pulses within the outbound DS1/E1 line signal, based upon this "B8ZS/HDB3 Encoder.
			Note: This pin is internally pulled "Low" with a 50k Ω resistor for each channels.

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SIGNAL NAME	PIN #	Түре	DESCRIPTION
TNEG_0/	3	I	Transmitter Negative-Polarity Data Input/Line Code Select Input:
CODES_0			The exact function of this input pin depends upon the following.
TNEG_1/ CODES_1	126		 Whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual Mode
TNEG_2/	105		 Whether the XRT83L34 device has been configure to operate in the
CODES_2			HOST or Hardware Mode, as described below
TNEG_3/ CODES_3	100		Dual-Rail Mode Operation - Transmit Negative-Polarity Data Input - TNEG_n:
			For Dual-Rail Applications, the System-Side Terminal Equipment should apply the "negative-polarity" portion of the outbound DS1/E1 data-stream to this input pin. Likewise, the System-Side Terminal Equipment should also apply the "positive-polarity" portion of the outbound DS1/E1 data-stream to the TPOS_n input pin.
			The Transmit Section of Channel n will sample this input pin (along with TPOS_n) upon the "user-selected" edge of TCLK_n. The Transmit Section of Channel n will generate a "negative-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic "HIGH" level. The Transmit Section of Channel n will NOT generate a "negative-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic LOW" level.
			Single-Rail Mode Operation - Line Code Select Input/NO FUNCTION:
			If the XRT83L34 device has been configured to operate in the Single-Rail Mode, then the exact function of this input pin depends upon whether the chip has been configured to operate in the HOST or Hardware Mode, as described below.
			HOST Mode Operation - NO FUNCTION:
			If the XRT83L34 device has been configured to operate in both the HOST Mode, and Single-Rail Modes, then this input pin has no function. Since this input pin has an internal pull-down resistor, the user can either leave this pin floating, or he/she can tie this pin to GND.
			Hardware Mode Operation - Line Code Select Input pin - CODES_n:
			If the XRT83L34 device has been configured to operate in both the Hardware and Single-Rail Modes, then this input pin permits the user to configure a given channel to enable or disable the HDB3/B8ZS Encoder and Decoder blocks as described below.
			If the user enables the HDB3/B8ZS Encoder and Decoder blocks then the Channel will support the HDB3 line code (for E1 applications) and the B8ZS line code (for T1 applications).
			If the user disables the HDB3/B8ZS Encoder and Decoder blocks, then the Channel will support the AMI line code (for either T1 and E1 applications).
			LOW - Enables the HDB3/B8ZS Encoder and Decoder blocks within Channel n.
			HIGH - Disables the HDB3/B8ZS Encoder and Decoder blocks within Channel n.
			Note: Internally pulled "Low" with a 50k Ω resistor for channel_n

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SIGNAL NAME	PIN #	Түре	DESCRIPTION
TCLK_0 TCLK_1 TCLK_2 TCLK_3	1 128 103 102	1	Transmit Line Clock Input - Channel n: The Transmit Section of Channel n will use this input pin to sample and latch the data that is present on the "TPOS_n/TDATA_n" and "TNEG_n" input pins. This input clock signal also functions as the timing source for the "Transmit Direction" signal within the Channel. For T1 Applications, the user is expected to apply a 1.544MHz clock signal to this input pin. Similarly, for E1 Applications, the user is expected to apply a 2.048MHz clock signal to this input pin. NOTE: Internally pulled "Low" with a 50k Ω resistor for all channels.
TAOS_0 TAOS_1 TAOS_2 TAOS_3 WR_R/W RD_DS ALE_AS CS	69 70 71 72 69 70 71 72	1	 Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY) The exact function of these input pins depend upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Modes, as described below. Hardware Mode Operation - Transmit All Ones Command Input - Channel n - TAOS_n: These input pins permits the user to command a given Channel to transmit an "Unframed, All Ones" pattern (via the outbound DS1/E1 line signal) to the remote terminal equipment. Setting this pin to the logic "HIGH" level configures the Transmit Section (of the corresponding channel) to transmit an Unframed, All Ones pattern via the outbound DS1/E1 line signal. Setting this pin to the logic "LOW" level, configures the Transmit Section (of the corresponding channel) to transmit normal traffic via the outbound DS1/E1 line signal. Host Mode Operation: These pins act as various microprocessor functions. See "Microprocessor Interface" on page 13. Note: These pins are internally pulled "Low" with a 50kΩ resistor.
TXON_0 TXON_1 TXON_2 TXON_3	122 123 124 125	1	 Transmitter Turn On for Channel _0 Hardware mode Setting this pin "High" turns on the Transmit Section of Channel _0 and has no control of the Channel_0 receiver. When TXON_0 = "0" then TTIP_0 and TRING_0 driver outputs will be tri-stated. <i>NOTE:</i> In Hardware mode only, all receiver channels will be turned on upon power-up and there is no provision to power them off. The receive channels can only be independently powered on or off in Host mode. In Host mode The TXON_n bits in the channel control registers turn each channel Transmit section ON or OFF. However, control of the on/off function can be transferred to the Hardware pins by setting the TXONCTL bit (bit 6) to "1" in the register at address hex 0x42. Transmitter Turn On for Channel _1 Transmitter Turn On for Channel _2 Transmitter Turn On for Channel _3
			NOTE: Internally pulled "Low" with a 50k Ω resistor for all channels.

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MICROPROCESSOR INTERFACE

SIGNAL NAME	Pin #	Түре	DESCRIPTION				
HW_HOST	68	Ι	 HOST/HARDWARE Mode Control Input pin: This pin permits the user to configure the XRT83L34 device to operate in either the HOST or the Hardware Mode. If the user configures the XRT83L34 device to operate in the HOST Mode, then the Microprocessor Interface block will become active and virtually all configuration settings (within the XRT83L34 device) will be achieved by writing values into the on-chip registers (via the Microprocessor Interface). If the user configures the XRT83L34 device to operate in the Hardware Mode, then the Microprocessor Interface block will be disabled, and all configuration settings (within the XRT83L34 device) will be achieved by setting various input pins to logic HIGH or LOW settings. LOGIC LOW - Configures the XRT83L34 device to operate in the HOST Mode. LOGIC HIGH or FLOATING - Configures the XRT83L34 device to operate in the Hardware Mode. 				
WR_R/W	69	I	 Write Strobe/Read-Write Operation Identifier/Transmit All Ones Input Pin - Channel 0: The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or the Hardware Mode, as described below. <i>HOST Mode Operation - Write Strobe/Read-Write Operation Identifier:</i> Assuming that the XRT83L34 device has been configured to operate in the Host Mode, then the exact function of the this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. Intel-Asynchronous Mode - WR* - Write Strobe Input pin: If the Microprocessor Interface is configured to operate in the Intel-Asynchron- nous Mode, then the input pin functions as the WR* (Active-Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Direction Data bus pins, D[7:0]) will be enabled. The Microprocessor Interface will latch the con- tents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT83L34) upon the rising edge of this input pin. Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identifica- tion Input pin: If the Microprocessor Interface is operating in the "Motorola-Asynchronous" Mode, then this pin is functionally equivalent to the R/W* input pin. In the Motorola-Asynchronous Mode, a READ operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. 				
TAOS_0	69		Hardware Mode Operation - Transmit All "Ones" Channel_0 - Hardware Mode See "Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)" on page 12. Note: Internally pulled "Low" with a 50kΩ resistor.				

XRT83L34 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

SIGNAL NAME	Pin #	Түре	DESCRIPTION
RD_DS	70	I	Read Strobe/Data Strobe/Transmit All Ones Command Input - Channel 1:
			The exact function of this input pin depends upon whether the XRT83L34 device has been configure to operate in the HOST or Hardware Mode, as described below.
			HOST Mode Operation - READ Strobe/Data Strobe Input:
			The exact function of this input pin depends upon which mode the Micropro- cessor Interface has been configured to operate in, as described below.
			Intel-Asynchronous Mode - RD* - READ Strobe Input:
			If the MIcroprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the RD* (Active Low READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT83L34 device will place the contents of the addressed register on the Microprocessor Interface Bi-Directional Data Bus (D[7:0]). When this signal is negated, then the Bi-Directional Data Bus will be tri-stated.
			Motorola-Asynchronous Mode - DS* - Data Strobe Input:
			If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this input pin will function as the DS * (Data Strobe) input signal
TAOS_1	70		Hardware Mode Operation - Transmit All One Command Input - Channel 1:
			See "Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)" on page 12.
			Note: Internally pulled "Low" with a 50k Ω resistor.

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SIGNAL NAME	Pin #	Түре	DESCRIPTION
ALE_AS	71	I	Address Latch Enable/Address Strobe/Transmit All Ones Input - Chan- nel 2:
			The exact function of this input pin depend upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.
TAOS_2	71		HOST Mode Operation - Address Latch Enable/Address Strobe Input Pin:
			The exact function of this input pin depends upon which mode the Micropro- cessor Interface has been configured to operate in, as described below. Intel-Asynchronous Mode - ALE - Address Latch Enable:
			If the Microprocessor Interface (of the XRT83L34 device) has been config- ured to operate in the Intel-Asynchronous Mode, then this active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[6:0]) into the XRT83L34 Microprocessor Interface bloc and to indicate the start of a READ or WRITE cycle.
			Pulling this input pin "high" enables the input bus drivers for the Address Bus Input pins (A[6:0]). The contents of the Address Bus will be latched into the XRT83L34 Microprocessor Interface circuitry, upon the falling edge of this input signal.
			Motorola Asynchronous Mode - AS* - Address Strobe Input:
			If the Microprocessor Interface has been configured to operate in the Motor- ola-Asynchronous Mode, then pulling this input pin "LOW enables the "input" bus drivers for the Address Bus Input pins.
			During each READ or WRITE operation, the user is expected to drive this input pin "LOW" after (or around the time that) he/she has places the address (of the "target" register) onto the Address Bus pins (A[6:0]). The user is then expected to hold this input pin "LOW" for the remainder of the READ or WRITE cycle.
			Note: It is permissible to tie the ALE_AS* and CS* input pins together Read and Write operations will be performed properly if ALE_AS is driven "LOW" coincident to whenever CS* is also driven "LOW".
			Hardware Mode Operation - Transmit All "Ones" Channel_2 - Hardware Mode
			See "Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)" on page 12.
			Note: Internally pulled "Low" with a 50k Ω resistor.
CS	72	I	Chip Select Input/Transmit All Ones Input - Channel 3: The exact function of this input pin depends upon whether the XRT83L34
TAOS_3	72		device has been configured to operate in the HOST or Hardware Mode, as described below.
			HOST Mode Operation - Chip Select Input pin: The user must assert this active-low signal in order to select the Micropro-
			cessor Interface for READ and WRITE operations between the Microprocessor and the XRT83L34 on-chip registers.
			Hardware Mode Operation - Transmit All Ones Input - Channel 3:
			See "Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)" on page 12.
			Note: Internally pulled "Low" with a 50k Ω resistor.

XRT83L34 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

SIGNAL NAME	Pin #	Түре	DESCRIPTION
RDY_DTACK	73	0	Ready or DTACK Output/Receive Muting upon LOS Command Input pin:
			The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.
RXMUTE	73	I	HOST Mode Operation - READY or DTACK Output Pin:
			The exact function of this input pin depends upon which mode the Micropro- cessor Interface has been configured to operate in, as described below.
			Intel-Asynchronous Mode - RDY* - Ready Output:
			If the Microprocessor Interface has been configured to operate in the Intel- Asynchronous Mode, then this output pin will function as the "active-low" READY output.
			During a READ or WRITE cycle, the Microprocessor Interface block will tog- gle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has tog- gled to the logic "low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
			If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "high" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
			Motorola-Asynchronous Mode - DTACK* - Data Transfer Acknowledge Output:
			If the Microprocessor interface has been configured to operate in the Motor- ola-Asynchronous Mode, then this output pin will function as the "active-low" DTACK output.
			During a READ or WRITE cycle, the Microprocessor Interface block will tog- gle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor Interface has determined that this input pin has toggled to the logic "low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
			If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "HIGH" level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic "LOW" level.
			Receive Muting - Hardware mode
			See "Receive Muting upon LOS Command Input/READY or DTACK Output:" on page 7.
			Note: Internally pulled "Low" with a 50k Ω resistor.

XRT83L34 REV. 1.0.1 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

μPTS1 106 1 Microprocessor Type Select Input Pins/Receive Clock Edge Select/ Transmit Clock Edge Select Input Pins. μPTS2 107 1 Microprocessor Type Select Input Pins. The exact function of these input pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. HOST Mode Operation - Microprocessor Type Select Input Bits 2 and 1 - μPTS[2:1]: These two input pins permit the user to configure the Microprocessor Inter- face to operate in either of the following modes. • Intel-Asynchronous Mode • Motorola-Asynchronous Mode The relationship between the settings of these input pins and the corre- sponding Microprocessor Interface configuration is presented below. MOTE: The μPTS2 (pin107) should be lied to GND. The μPTS(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Mode. NOTE: The μPTS2 (pin107) should be lied to GND. The μPTS(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. TCLKE 107 See "Receive Clock Edge Select Input pin: See "Receive Clock Edge Select Mode" on page 9. NoTE: These pins are internally pulled "Low" with a 50KΩ resistor. D[7] 42 I/O Bi-Directional Data Bus Pins/Loop-back Control Input Pins - Df7:0]: The exact function of these input/output pins depends upon whether the Microprocessor Interface of the XRT83L34 device. HOST Mode Operation - 1-Bi-Dir	SIGNAL NAME	Pin #	Түре			I	DESCRIPTION		
Product Not The exact function of these input pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. HOST Mode Operation - Microprocessor Type Select Input Bits 2 and 1 - µPTS[2:1]: These two input pins permit the user to configure the Microprocessor Interface to operate in either of the following modes. Intel-Asynchronous Mode • Intel-Asynchronous Mode • Intel-Asynchronous Mode • Intel-Asynchronous Mode • Intel-Asynchronous Mode • Motorola-Asynchronous Mode • Motorola-Asynchronous Mode Note: The upTS2 (pin107) should be tied to GND. The µPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Mode Note: The upTS2 (pin107) should be tied to GND. The µPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Mode Note: The upTS2 (pin107) should be tied to GND. The µPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. TCLKE 107 See "Receive Clock Edge Select/Input pin: See "Transmit Clock Edge - Hardware Mode" on page 9. Nore: These pins are internally pulled "Low" with a 50kΩ resistor. D[7] 42 I/O Bi-Directional Data Bus PinsLoop-back Control Input Pins - 0[7:0]: The exact function of these input output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.	μPTS1 uPTS2	106 107	I	Microprocessor Type Select Input Pins/Receive Clock Edge Select/ Transmit Clock Edge Select Input Pin:					
PTS[2:1]: These two input pins permit the user to configure the Microprocessor Interface to operate in either of the following modes. • Intel-Asynchronous Mode • Motorola-Asynchronous Mode The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. <u>μPTS2</u> <u>μPTS1</u> <u>μPTS1</u> <u>μPType</u> <u>0</u> <u>0</u> <u>1</u> Motorola-Asynchronous Mode Notre: The μPTS2 (pin107) should be tied to GND. The μPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. RCLKE 106 RCLKE 107 RCLKE RCLKE RCLKE RCLKE RCLKE <td></td> <td></td> <td></td> <td colspan="6">The exact function of these input pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.</td>				The exact function of these input pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.					
RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge - Hardware Mode" NOTE: The µPTS2 µPTS1 µP Type 0 0 Intel Asynchronous Mode NOTE: The piPTS2 µPTS1 µP Type 0 0 Intel Asynchronous Mode NOTE: The µPTS2 (pin107) should be tied to GND. The µPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge Select/Microprocessor Type Select Input pin: on page 8. TCLKE 107 See "Transmit Clock Edge - Hardware Mode" on page 9. NOTE: These pins are internally pulled "Low" with a 50kΩ resistor. D[7] 42 I/O D[7] 42 I/O D[8] 43 D[9] 44 D[9] 44 D[1] 42 D[2] 47 D[3] 46 D[4] 45 D[5] 44 D[7] 42 D[9] 46 D[17] 42				μ PTS [[2:1]:			a 1	
Pintel-Asynchronous Mode • Intel-Asynchronous Mode • Motorola-Asynchronous Mode The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. <u>μPTS2</u> μPTS1 μPTS1 μPT ype <u>0</u> 0 Intel Asynchronous Mode <u>0</u> 1 Motorola Asynchronous Mode <u>1</u> Motorola Asynchronous Modes. RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge Select Input pin: See "Transmit Clock Edge - Hardware Mode" on page 9. <i>Nore: These pins are internally pulled "Low" with a 50kQ resistor.</i> D[7] 42 I/O Bi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]: The exact function of these input/output pins depends upon whether the XFT381.34 device has been configured to operate in the HOST or Hardware Mode, as described below. D[3] 46 HOST Mode Operation - Bi-Directional Data Bus Input/Output Pins device. D[9] 47 The seas ins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs a READ or WRITE operation				These face to	two input pin operate in ei	s permit the u ther of the fo	user to configure the Microprocessor Int Ilowing modes.	er-	
Picture • Motorola-Asynchronous Mode The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. Image: transmit Clock Edge Select Input pins RCLKE 106 RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: on page 8. Hardware Mode Operation - Receive Clock Edge Select Input pin: on page 8. TCLKE 107 BioDirectional Data Bus Pins/Loop-back Control Input Pins - D[7:0]: These pins are internally pulled "Low" with a 50kΩ resistor. D[7] 42 D[6] 44 D[7] 42 D[6] 44 D[7] 42 D[8] 46 HOST Mode Operation - Bi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]: The exact function of these input/output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. D[8] 46 HOST Mode Operation - Bi-Directional Data Bus Input/Output Pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. D[9] 47 D[6] 44 D[7] 42 D[8] 46				• Inte	el-Asynchror	nous Mode			
RCLKE 106 WTE: The µPTS2 (pin107) should be tied to GND. The µPTS1(pin 106), input pin permits the user to selects either the Intel-Asynchronous Mode RCLKE 106 NOTE: The µPTS2 (pin107) should be tied to GND. The µPTS1(pin 106), input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge Select Input pin:" on page 8. TCLKE 107 See "Receive Clock Edge Select Microprocessor Type Select Input pin:" on page 8. D[7] 42 I/O D[6] 43 D[7] 42 D[6] 43 D[7] 42 D[7] 42 D[7] 42 D[7] 42 D[7] 42 D[6] 43 D[7] 42 D[6] 43 D[7] 42 D[8] 46 D[9] 46 D[9] 46 D[9] 46 D[9] 46 D[9] 47 D[17] 42 D[2] 47				• Mo	torola-Async	chronous M	ode		
μPTS2 μPTS1 μP Type 0 0 Intel Asynchronous Mode 0 1 Motorola Asynchronous Mode NOTE: The μPTS2 (pin107) should be tied to GND. The μPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge Select/Microprocessor Type Select Input pin: See "Transmit Clock Edge - Hardware Mode" on page 9. NOTE: These pins are internally pulled "Low" with a 50kΩ resistor. D[7] 42 I/O D[6] 43 D[7] 42 I/O D[6] 43 D[7] 44 D[8] Host function of these input/output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode as described below. D[3] 46 D[4] 45 D[6] 43 D[2]/ 47 D[1]/ <td></td> <td></td> <td></td> <td>The re spond</td> <td>lationship bet ing Microproc</td> <td>ween the set essor Interfa</td> <td>tings of these input pins and the corre- ce configuration is presented below.</td> <td></td>				The re spond	lationship bet ing Microproc	ween the set essor Interfa	tings of these input pins and the corre- ce configuration is presented below.		
0 0 Intel Asynchronous Mode 0 1 Motorola Asynchronous Mode 0 1 Motorola Asynchronous Mode 0 1 Motorola Asynchronous Mode Nore: The µPTS2 (pin107) should be lied to GND. The µPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge Select/Microprocessor Type Select Input pin:" on page 8. TCLKE 107 Hardware Mode Operation - Transmit Clock Edge Select Input pin: See "Transmit Clock Edge - Hardware Mode" on page 9. Nore: These pins are internally pulled "Low" with a 50kΩ resistor. D[7] 42 D[6] 43 D[5] 44 D[7] 42 D[8] Bi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]: The exact function of these input/output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. D[3] 46 D[1]/ 48 D[2]/ 47 D[1]/ 48 D[2]/ 49 UOP1_0 <td></td> <td></td> <td></td> <td></td> <td>µPTS2</td> <td>µPTS1</td> <td>μР Туре</td> <td></td>					µPTS2	µPTS1	μР Туре		
0 1 Motorola Asynchronous Mode NoTE: The µPTS2 (pin107) should be tied to GND. The µPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge Select/Microprocessor Type Select Input pin:" on page 8. TCLKE 107 Hardware Mode Operation - Transmit Clock Edge Select Input pin: See "Transmit Clock Edge - Hardware Mode" on page 9. NOTE: These pins are internally pulled "Low" with a 50kΩ resistor. D[7] 42 I/O D[6] 43 D[5] 44 XR33L34 device has been configured to operate in the HOST or Hardware Mode, as described below. D[3] 46 D[4] 45 D[3] 46 D[7]/ 42 D[7] 43 D[3] 46 D[4] 45 D[3] 46 D[4] 45 D[7]/ 42 D[7] 42 D[7] 48 D[7] 49 D[7] 41 D[8] The exact function of these input/o					0	0	Intel Asynchronous Mode		
NoTE: The μPTS2 (pin107) should be tied to GND. The μPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes. RCLKE 106 Hardware Mode Operation - Receive Clock Edge Select Input pin: See "Receive Clock Edge Select/Microprocessor Type Select Input pin:" on page 8. TCLKE 107 See "Transmit Clock Edge - Hardware Mode" on page 9. D[7] 42 I/O Bi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]: The exact function of these input/output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. HOST Mode Operation - Bi-Directional Data Bus Input/Output Pins (Microprocessor Interface block) - D[7:0]: These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs a READ or WRITE operation with the Microprocessor Interface of the XRT83L34 device. LOOP1_0 42 Hardware Mode Operation - Loop-back Control pin, Bits [1:0]_Channel_n - Hardware Mode LOOP1_1 44 Pins 42 - 49 control which Loop-Back mode is selected per channel. See "LoOp-Back Control Pins - Hardware Mode LOOP1_2 46 Wicreare Mode Operation - Loop-back Control pin, Bits [1:0]_Channel_n - Hardware Mode LOOP1_2 46 Wicreare Mode Operation - Loop-Back mode is selected per channel. See "LoOP0_2 47					0	1	Motorola Asynchronous Mode		
TCLKE107pin:" on page 8. Hardware Mode Operation - Transmit Clock Edge Select Input pin: See "Transmit Clock Edge - Hardware Mode" on page 9. NoTE: These pins are internally pulled "Low" with a 50kΩ resistor.D[7]42I/OBi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]: The exact function of these input/output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.D[3]46HOST Mode Operation - Bi-Directional Data Bus Input/Output Pins (Microprocessor Interface block) - D[7:0]: These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs a READ or WRITE operation with the Microprocessor Interface of the XRT83L34 device.LOOP1_042Hardware Mode Operation - Loop-back Control pin, Bits [1:0]_Channel_n - Hardware ModeLOOP1_144Pins 42 - 49 control which Loop-Back mode is selected per channel. See "LoOp-Back Control Pins - Hardware Mode:" on page 22. NOTE: Internally pulled "Low" with a 50kΩ resistor.	RCLKE	106		Note: Hardw See "	input pin pe the Motorol vare Mode Op Receive Cloo	e (pin107) sh armits the use a Asynchrone ceration - Re ck Edge Se	ould be tied to GND. The μPTS1(pin or to selects either the Intel-Asynchronou ous Modes. eceive Clock Edge Select Input pin: lect/Microprocessor Type Select Inp	106) us or out	
D[7]42I/OBi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]: The exact function of these input/output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.D[4]45HOST Mode Operation - Bi-Directional Data Bus Input/Output Pins (Microprocessor Interface block) - D[7:0]: These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor Interface block) - D[7:0]: These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor Interface of the XRT83L34 device.LOOP1_042Hardware Mode Operation - Loop-back Control pin, Bits [1:0]_Channel_n - Hardware ModeLOOP1_144Pins 42 - 49 control which Loop-Back mode is selected per channel. See "Loop-Back Control Pins - Hardware Mode:" on page 22. NOTE: Internally pulled "Low" with a 50kΩ resistor.	TCLKE	107		pin:" on page 8. Hardware Mode Operation - Transmit Clock Edge Select Input pin: See "Transmit Clock Edge - Hardware Mode" on page 9. Note: These pins are internally pulled "Low" with a 50kΩ resistor.					
D[6]43D[5]44D[4]45D[3]46D[2]/47D[1]/48D[0]/49LOOP1_042LOOP1_144LOOP1_144LOOP1_246LOOP1_246LOOP1_247LOOP1_247LOOP1_247LOOP1_247LOOP1_247LOOP1_247LOOP1_247LOOP1_246LOOP1_247 <tr< td=""><td>D[7]</td><td>42</td><td>I/O</td><td>Bi-Dir</td><td>ectional Data</td><td>Bus Pins/L</td><td>oop-back Control Input Pins - D[7:0]:</td><td></td></tr<>	D[7]	42	I/O	Bi-Dir	ectional Data	Bus Pins/L	oop-back Control Input Pins - D[7:0]:		
D[3]44Mode, as described below.D[4]45D[3]46D[2]/47D[1]/48D[0]/49LOOP1_042LOOP1_143LOOP1_144LOOP1_144LOOP1_246LOOP1_246LOOP1_246LOOP1_247	D[6]	43		The ex	act function o	of these input	/output pins depends upon whether the igured to operate in the HOST or Hardw	vare	
D[3]46D[2]/47D[1]/48D[0]/49LOOP1_042LOOP1_1042LOOP1_144LOOP1_144LOOP1_245LOOP1_246LOOP1_247LOOP1_247	D[3] D[4]	44 45		Mode,	as described	below.		Varo	
D[2]/47D[1]/48D[0]/49LOOP1_042LOOP0_043LOOP1_144LOOP1_144LOOP0_145LOOP1_246LOOP1_247	D[3]	46		HOST (Micro	Mode Opera	tion - Bi-Dir	ectional Data Bus Input/Output Pins		
D[1]/48D[0]/49bus, whenever the Microprocessor performs a READ or WRITE operation with the Microprocessor Interface of the XRT83L34 device.LOOP1_042LOOP0_043LOOP1_144LOOP0_145LOOP1_246LOOP0_247	D[2]/	47		These	pins are used	d to drive and	I receive data over the bi-directional dat	a	
LOOP1_042LOOP0_043LOOP1_144LOOP0_145LOOP1_246LOOP0_247	D[0]/	48 49		bus, w with th	henever the Ne Microproce	Aicroprocess ssor Interface	or performs a READ or WRITE operatic o of the XRT83L34 device.	on	
LOOP0_043[1:0]_Channel_n - Hardware ModeLOOP1_144Pins 42 - 49 control which Loop-Back mode is selected per channel. SeeLOOP0_145"Loop-Back Control Pins - Hardware Mode:" on page 22.LOOP1_246Note: Internally pulled "Low" with a 50kΩ resistor.	LOOP1_0	42		Hardw	/are Mode Op	peration - Lo	op-back Control pin, Bits		
LOOP1_145Plns 42 - 49 control which Loop-Back mode is selected per channel. SeeLOOP0_145"Loop-Back Control Pins - Hardware Mode:" on page 22.LOOP1_246Note: Internally pulled "Low" with a 50kΩ resistor.LOOP0_247	LOOP0_0	43		[1:0]_	Channel_n - I	Hardware M			
LOOP1_2 46 Note: Internally pulled "Low" with a 50kΩ resistor.	LOOP0_1	45		"Loop	 - 49 control -Back Control 	ol Pins - Ha	back mode is selected per channel. Se rdware Mode:" on page 22.	;e	
LOOP0_2 47	LOOP1_2	46		NOTE:	Internally pu	lled "Low" wi	th a 50k Ω resistor.		
	LOOP0_2	47							
LOOP1_3 48 LOOP0 3 49	LOOP1_3 LOOP0_3	48 49							

XP EXAR QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

SIGNAL NAME	PIN #	Түре	DESCRIPTION
A[6] A[5] A[4] A[3] A[2] A[1] A[0] JASEL1 JASEL0 EQC4 EQC4 EQC3 EQC2 EQC1 EQC1 EQC0	PIN # 57 58 59 60 61 62 63 57 58 59 60 61 62 63	I	DESCRIPTION Address Bus Input Pins/Jitter Attenuator Select Input Pins/Equalizer Control Input pins: The exact function of these input pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. HOST Mode Operation - Address Bus Input Pins - A[6:0]: These pins permits the Microprocessor to identity on-chip registers (within the XRT83L34 device0 whenever it performs READ and WRITE operations with the XRT83L34 device. Microprocessor Interface Address Bus[6] Microprocessor Interface Address Bus[5] Microprocessor Interface Address Bus[3] Microprocessor Interface Address Bus[3] Microprocessor Interface Address Bus[2] Microprocessor Interface Address Bus[1] Microprocessor Interface Address Bus[0] Jitter Attenuator Select Pins - Hardware Mode Jitter Attenuator select pin 1 Jitter Attenuator select pin 0 See "Jitter Attenuator" on page 19. Equalizer Control Input pin 4 Equalizer Control Input pin 3 Equalizer Control Input pin 1 Equalizer Control Input pin 0 Pins EQCI4:0] select the Receive Equalizer and Transmitter Line Build Out.
			See "Alarm Function//Redundancy Support" on page 21. Note: Internally pulled "Low" with a 50kΩ resistor.
INT TRATIO	119	I	Interrupt Output - Host Mode This pin goes "Low" to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to "0" in the command control register. Transmitter Transformer Ratio Select - Hardware mode The function of this pin is to select the transmitter transformer ratio. See
			 "Alarm Function//Redundancy Support" on page 21. Note: This pin is an open drain output and requires an external 10kΩ pull- up resistor.

XP EXAR REV. 1.0.1 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

JITTER ATTENUATOR

SIGNAL NAME	Pin #	Түре		DESCRIPTION					
JASEL0 JASEL1	58 57	I	Jitter Attenuator Select Pins - Hardware Mode Jitter Attenuator select pin 0 Jitter Attenuator select pin 1 JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it.						
					IA Dath	JA E	W Hz		
			JASELI	JASELU	JA Path	T1	E1	FIFU Size	
			0	0	Disabled				
			0	1	Transmit	3	10	32/32	
			1	0	Receive	3	10	32/32	
			1	1	Receive	3	1.5	64/64	
A[6] A[5]	57 58		Microprocesso See "Address Equalizer Con Note: Internal	or Address Bus Input trol Input p y pulled "Lo	Bits A[6:5] -H Pins/Jitter A bins:" on pag w" with a 50k	lost Mo ttenuato e 18. Ω <i>resisto</i>	de or Select r.	Input Pins/	

XRT83L34 QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

CLOCK SYNTHESIZER

SIGNAL NAME	PIN #	Түре	DESCRIPTION						
MCLKE1	32	I	E1 Master	Clock In	put				
			A 2.048MHz clock for with an accuracy of better than \pm 50ppm and a duty cycle of 40% to 60% can be provided at this pin.						
			clock shou operation.	lld be coni	nected to b	oth MCLK	E1 and M	CLKT1 input	s for proper
			Notes:						
			1. A ra	II channel ate, either	s of the XI T1, E1 or	RT83L34 r. J1.	nust be op	perated at th	e same clock
			2. li	nternally p	ulled "Low	" with a 50	$k\Omega$ resisto	r.	
CLKSEL0	37	Ι	Clock Sel	ect inputs	for Maste	er Clock S	ynthesize	er - Hardwar	re mode
CLKSEL1	38		CLKSEL[2	:0] are inp	ut signals t	to a progra	mmable fr	equency syr	nthesizer that
CLKSEL2	39		can be use	ed to gene	rate a mas	ster clock f	rom an ac	curate exteri	nal clock
			Source acc	Coraing to	trel eignel	ig lable.	od from th	o ototo of E(
			inputs. Se	e Table 4 f	or descript	tion of Trai	ea from in nsmit Faua	alizer Contro	JO[4.0] I bits.
			Host Mod	e: The sta	te of these	pins are i	anored an	d the master	r frequency
			PLL is con	trolled by	the corres	ponding in	terface bits	s. See regis	ter address
			1000001.						
			MCLKE1 MCLKT1 CLKSEL2 CLKSEL1 CLKSEL0 MCLKRATE CLKOUT					CLKOUT (KHz)	
			2048	2048	0	0	0	0	2048
			2048	2048	0	0	0	1	1544
			2048	1544	0	0	0	0	2048
			1544	1544	0	0	1	1	1544
			1544	1544	0	0	1	0	2048
			2048	1544	0	0	1	1	1544
			8	х	0	1	0	0	2048
			8	х	0	1	0	1	1544
			16	х	0	1	1	0	2048
			16	х	0	1	1	1	1544
			56	х	1	0	0	0	2048
			56	х	1	0	0	1	1544
			64	х	1	0	1	0	2048
			64	Х	1	0	1	1	1544
			128	Х	1	1	0	0	2048
			128	Х	1	1	0	1	1544
			256	Х	1	1	1	0	2048
			256	Х	1	1	1	1	1544
			Note: Th	ese pins a	re internal	ly pulled "L	ow" with a	a 50k Ω resis	tor.

XRT83L34 **EXAR** *Rev. 1.0.1* QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

SIGNAL NAME	Pin #	Түре	DESCRIPTION
MCLKT1	33	I	T1 Master Clock Input
			This signal is an independent 1.544MHz clock for T1 systems with required accuracy of better than ±50ppm and duty cycle of 40% to 60%. MCLKT1 input is used in the T1 mode.
	1	l	Notes:
			1. All channels of the XRT83L34 must be operated at the same clock rate, either T1, E1 or J1.
			2. See pin 32 description for further explanation for the usage of this pin.
			3. Internally pulled "Low" with a 50k Ω resistor.
MCLKOUT	36	0	Synthesized Master Clock Output
			This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.

ALARM FUNCTION//REDUNDANCY SUPPORT

SIGNAL NAME	PIN #	Түре	DESCRIPTION
GAUGE	87	I	Twisted Pair Cable Wire Gauge Select - Hardware mode Connect this pin "High" to select 26 Gauge wire. Connect this pin "Low" to select 22 and 24 gauge wire for all channels. Note: Internally pulled "Low" with a 50k Ω resistor.
DMO_0 DMO_1 DMO_2 DMO_3	64 65 66 67	0	Driver Failure Monitor Channel _0 This pin transitions "High" if a short circuit condition is detected in the trans- mit driver of Channel _0, or no transmit output pulse is detected for more than 128 TCLK_0 cycles. Driver Failure Monitor Channel _1 Driver Failure Monitor Channel _2 Driver Failure Monitor Channel _3
ATAOS	50	I	 Automatic Transmit "All Ones" Pattern - Hardware Mode Only: A "High" level on this pin enables the automatic transmission of an "All Ones" AMI pattern from the transmitter of any channel that the receiver of that channel has detected an LOS condition. A "Low" level on this pin disables this function. Note: All channels share the same ATAOS input control function. Microprocessor Clock Input - Host Mode This pin should be tied to GND for asynchronous microprocessor modes. Note: This pin is internally pulled "Low" for asynchronous microprocessor interface when no clock is present.

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QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR REV. 1.0.1

SIGNAL NAME	Pin #	Түре			DESCRIPTION				
TRATIO	119	0	Transmitter Transformer Ratio Select - Hardware ModeIn external termination mode (TXSEL = 0), setting this pin "High" selects atransformer ratio of 1:2 for the transmitter. A "Low" on this pin sets the transmitter transformer ratio to 1:2.45. In the internal termination mode thetransmitter transformer ratio to 1:2.45. In the internal termination mode thetransmitter transformer ratio is permanently set to 1:2 and the state of this pinis ignored.Interrupt Output - Host ModeThis pin is asserted "Low" to indicate an alarm condition. See "Microprocessor Interface" on page 13.Note: This pin is an open drain output and requires an external 10kΩ pull- up resistor.						
RESET	121	Ι	Hardware Reset (Active "Low") When this pin is tied "Low" for more than 10μ s, the device is put in the reset state. Pulling RESET and ICT pins "Low" simultaneously will put the chip in factory test mode. This condition should not be permitted during normal operation. Note: Internally pulled "High" with a 50k Ω resistor.						
SR/DR	16	I	Single-Rail/Dual-Rail Data Format Connect this pin "Low" to select transmit and receive data format in Dual-rail mode. In this mode, HDB3 or B8ZS encoder and decoder are not available. Connect this pin "High" to select single-rail data format. Note: Internally pulled "Low" with a 50kΩ resistor.						
LOOP1_0 LOOP0_0 LOOP1_1 LOOP0_1 LOOP1_2 LOOP0_2 LOOP1_3 LOOP0_3	42 43 44 45 46 47 48 49	I/O	Loop-Back Control Pins - Hardware Mode: Loop-back control pin 1 - Channel _0 Loop-back control pin 0 - Channel _0 Loop-back control pin 1 - Channel _1 Loop-back control pin 0 - Channel _1 Loop-back control pin 1 - Channel _2 Loop-back control pin 0 - Channel _2 Loop-back control pin 1 - Channel _3 Loop-back control pin 0 - Channel _3						
			LOOP1_n	LOOP0_n	MODE				
			0	0	Normal Mode No Loop-back Channel_n				
			0	1	Local Loop-Back Channel_n				
			1	0	Remote Loop-Back Channel_n				
			1	1	Digital Loop-Back Channel_n				
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	42 43 44 45 46 47 48 49		Microprocesso These pins are Bus Pins/Loop Note: These p	or R/W Data b microprocesse o-back Contr oins are interna	its [7:0] - Host Mode or data bus pins. See "Bi-Directional Data ol Input Pins - D[7:0]:" on page 17. ally pulled "Low" with a 50kΩ resistor.				