Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

QUAD T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

FEBRUARY 2005 *REV. 1.0.1*

GENERAL DESCRIPTION

The XRT83L34 is a fully integrated Quad (four channel) long-haul and short-haul line interface unit for T1 (1.544Mbps) 100Ω, E1 (2.048Mbps) 75Ω or 120Ω, or J1 110Ω applications.

In long-haul applications the XRT83L34 accepts signals that have been attenuated from 0 to 36dB at 772kHz in T1 mode (equivalent of 0 to 6000 feet of cable loss) or 0 to 43dB at 1024kHz in E1 mode.

In T1 applications, the XRT83L34 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83L34 provides both a parallel Host microprocessor interface as well as a Hardware mode for programming and control.

Both the B8ZS and HDB3 encoding and decoding functions are selectable as well as AMI. An on-chip crystal-less jitter attenuator with a 32 or 64 bit FIFO can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L34 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. In the absence of the power supply, the transmit outputs and receive inputs are tri-stated allowing for redundancy applications The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

Features (See Page 2)

FIGURE 1. BLOCK DIAGRAM OF THE XRT83L34 T1/E1/J1 LIU (HOST MODE)

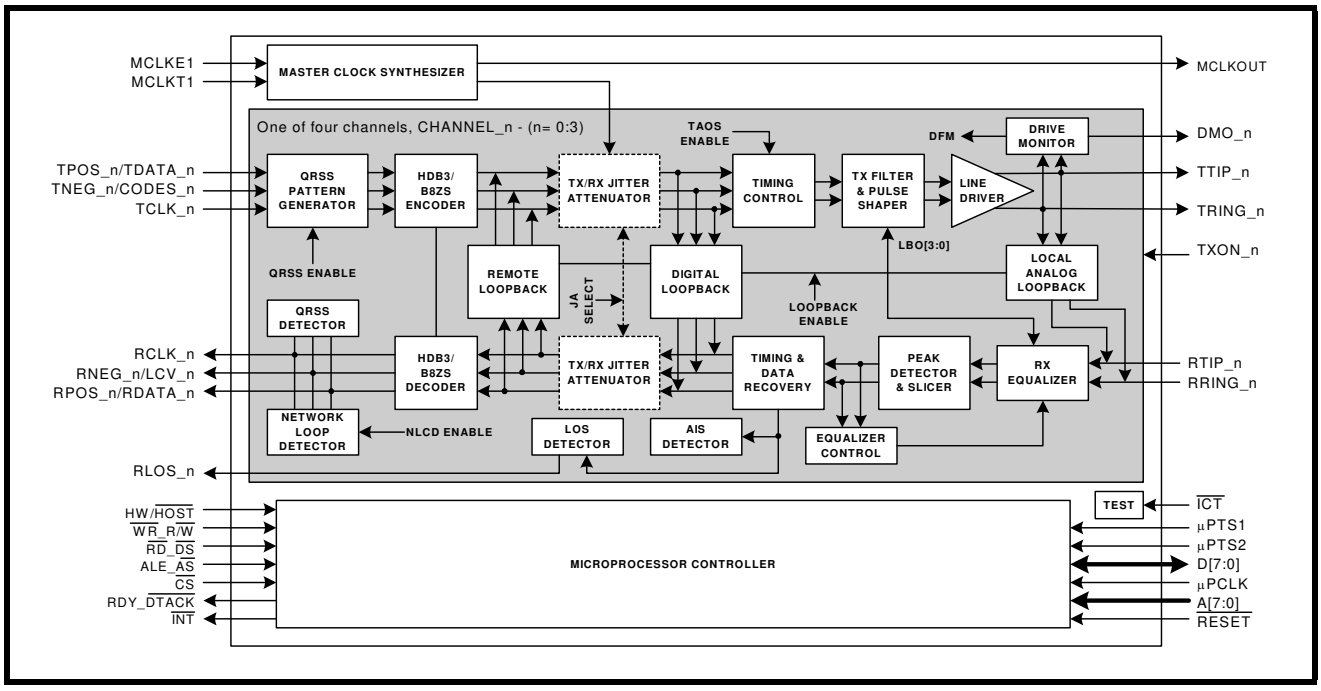
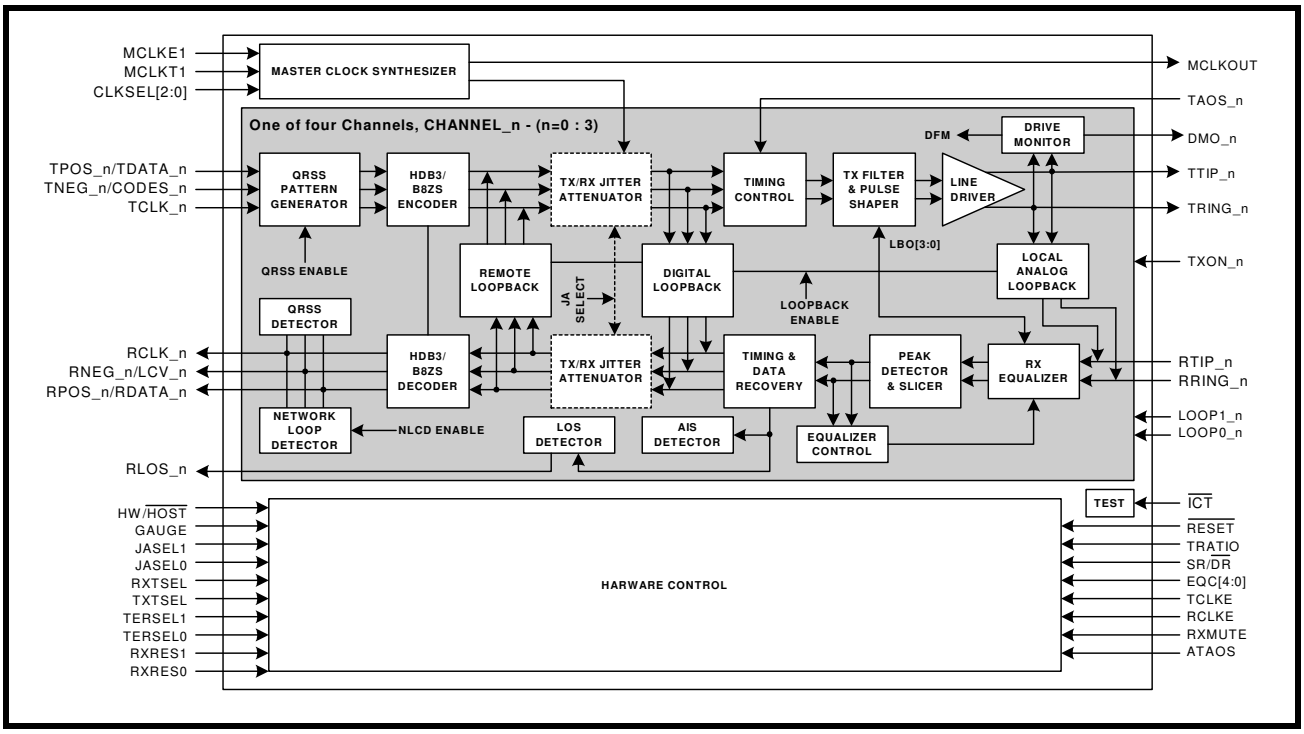


FIGURE 2. BLOCK DIAGRAM OF THE XRT83L34 T1/E1/J1 LIU (HARDWARE MODE)



FEATURES

- Fully integrated four channel long-haul or short-haul transceivers for E1,T1 or J1 applications
- Adaptive Receive Equalizer for up to 36dB cable attenuation
- Programable Transmit Pulse Shaper for E1,T1 or J1 short-haul interfaces
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping that can be used for both T1 and E1 modes.
- Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps
- Selectable receiver sensitivity from 0 to 36dB cable loss for T1 @772kHz and 0 to 43dB for E1 @1024kHz
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for E1 and 0 to 3dB of cable attenuation for T1 modes
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications
- Internal and/or external impedance matching for 75Ω, 100Ω, 110Ω and 120Ω
- Tri-State transmit output and receive input capability for redundancy applications
- Provides High Impedance for Tx and Rx during power off
- Transmit return loss meets or exceeds ETSI 300-166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- High receiver interference immunity
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder functions
- QRSS pattern generator and detection for testing and monitoring

- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Local Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both Hardware and Host (parallel Microprocessor) interface for programming
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Single 3.3V Supply Operation
- 128 pin TQFP package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L34IV	128 Lead TQFP (14 x 20 x 1.4mm)	-40°C to +85°C

FIGURE 3. PIN OUT OF THE XRT83L34

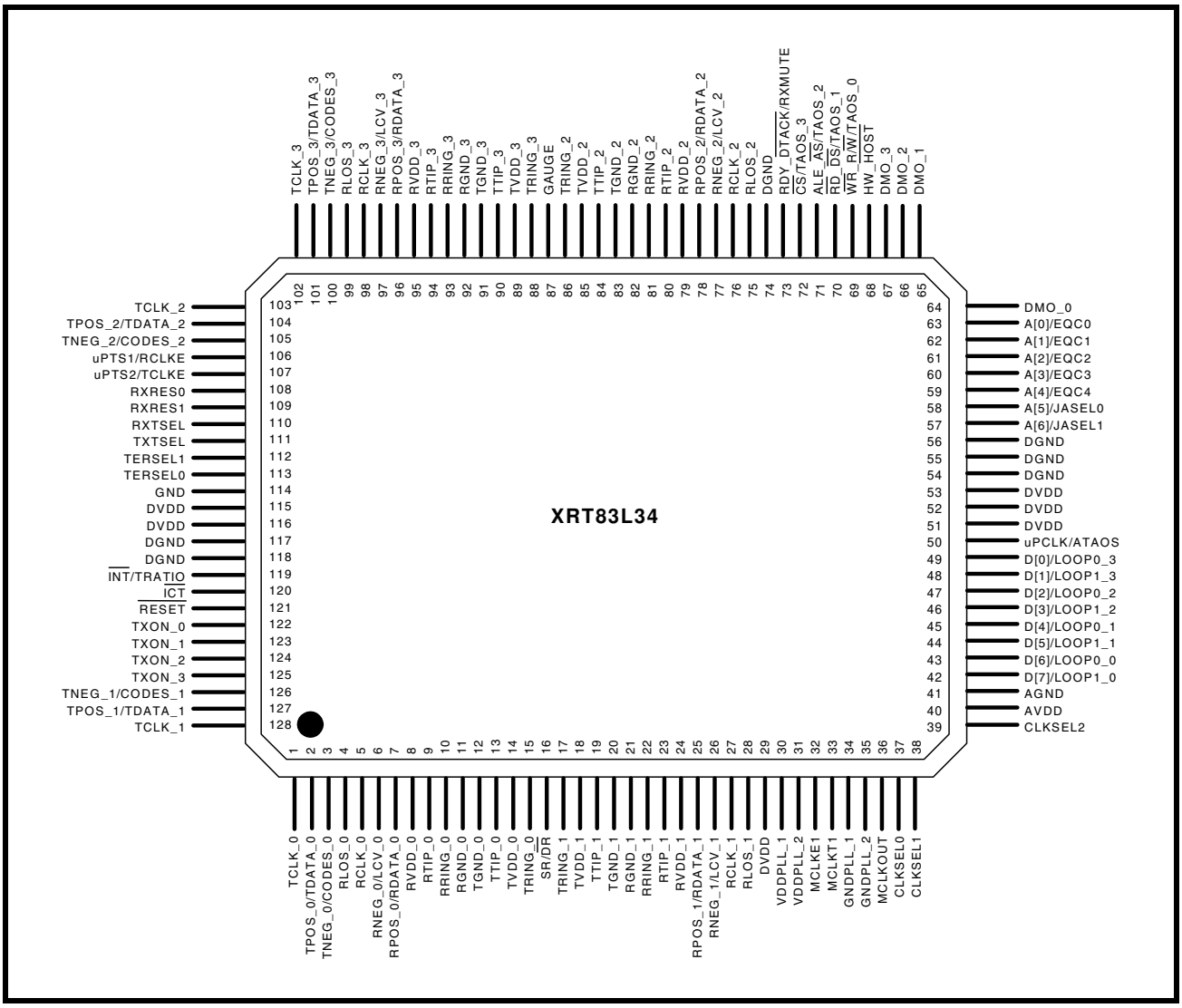


TABLE OF CONTENTS

PIN DESCRIPTION BY FUNCTION

RECEIVE SECTIONS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RLOS_0 RLOS_1 RLOS_2 RLOS_3	4 28 75 99	O	**Receiver LOS (Loss of Signal) Defect Indicator Output for Channel _n** This output pin indicates whether or not the Receive Section associated with Channel n (within the LIU device) is declaring the LOS defect condition, as depicted below. LOGIC LOW - Indicates that this particular channel is currently not declaring the LOS defect condition. LOGIC HIGH - Indicates that this particular channel is currently declaring the LOS defect condition. See “Receiver Loss of Signal (RLOS)” on page 28.
RCLK_0 RCLK_1 RCLK_2 RCLK_3	5 27 76 98	O	**Receiver Clock Output for Channel _n** The Receive Section (of a given channel within the XRT83L34 device) will update the RPOS_n and RNEG_n/LCV_n output pins upon either the rising or falling edge of this output clock signal (depending upon user configuration).
RNEG_0/ LCV_0 RNEG_1/ LCV_1 RNEG_2/ LCV_2 RNEG_3/ LCV_3	6 26 77 97	O	**Receiver Negative-Polarity Data Output/Line Code Violation Indicator Output - Channel n:** The exact function of this output pin depends upon whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual-Rail Mode, as described below. **Dual-Rail Mode Operation - Receive Negative-Polarity Data Output - RNEG_n:** The Receive Section of Channel n will output the negative-polarity portion of the recovered incoming DS1/E1 data (from the remote terminal equipment) via this output pin. Each channel (within the XRT83L34 device) will update this incoming DS1/E1 data upon the "user-selected" edge of the RCLK_n output signal. The "Positive-Polarity Portion" of the recovered incoming DS1/E1 data will be output via the RPOS_n output pin. **Single-Rail Mode Operation - Line Code Violation Indicator Output - LCV_n:** The Receive Section of Channel n will pulse this output pin "high" (for one RCLK_n period) each time it detects a Line Code Violation within the incoming DS1/E1 line signal. Each channel (within the XRT83L34 device) will update this output pin upon the "user-selected" edge of the RCLK_n output signal.

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RPOS_0/ RDATA_0 RPOS_1/ RDATA_1 RPOS_2/ RDATA_2 RPOS_3/ RDATA_3	7 25 78 96	O	**Receiver Positive-Polarity Data Output/Receive Data Output - Channel n:** The exact function of this output pin depends upon whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual-Rail Mode as described below. **Dual-Rail Mode Operation - Receive Positive-Polarity Data Output Pin - RPOS_n:** The Receive Section of Channel n will output the positive-polarity portion of the Recovered incoming DS1/E1 data (from the remote terminal equipment) via this output pin. Each Channel (within the XRT83L34 device) will update the data (that is output via this output pin) upon the "user-selected" edge of the RCLK_n output clock signal. The "Negative-Portion" of this recovered incoming DS1/E1 data (from the remote terminal equipment) will be output via the corresponding RNEG_n output pin. **Single-Rail Mode Operation - Receive Data Output Pin - RDATA_n** If Channel n has been configured to operate in the Single-Rail Mode, then the entire incoming DS1/E1 data (that has been recovered by the Receive Section of Channel n) will be output via this output pin upon the "user-selected" edge of the RCLK_n output clock signal.
RTIP_0 RTIP_1 RTIP_2 RTIP_3	9 23 80 94	I	**Receiver Differential Tip Positive Input for Channel _n:** This input pin, along with the corresponding RRING_n input pin functions as the "Receive DS1/E1 Line Signal" for Channel n, within the XRT83L34 device. The user is expected to connect this signal and the corresponding RRING_n input signal to a 1:1 transformer. Whenever the RTIP_n/RRING_n input pins are receiving a positive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "higher-voltage" than that of the corresponding RRING_n input pin. Conversely, whenever the RTIP_n/RRING_n input pins are receiving a negative-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "lower-voltage" than that of the corresponding RRING_n input pin.
RRING_0 RRING_1 RRING_2 RRING_3	10 22 81 93	I	**Receiver Differential Ring Negative Input for Channel _n:** This input pin, along with the corresponding RTIP_n input pin functions as the "Receive DS1/E1 Line Signal" for Channel n, within the XRT83L34 device. The user is expected to connect this signal and the corresponding RTIP_n input signal to a 1:1 transformer. Whenever the RTIP_n/RRING_n input pins are receiving a positive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "lower-voltage" than that of the corresponding RTIP_n input pin. Conversely, whenever the RTIP_n/RRING_n input pins are receiving a negative-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a "higher-voltage" than that of the corresponding RTIP_n input pin.

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RXMUTE	73	I	**Receive Muting upon LOS Command Input/READY or DTACK Output:** The exact function of this Input/Output pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. ***Hardware Mode Operation - Receive Muting upon LOS Command Input pin:*** This input pin permits the user to enable or disable the "Muting upon LOS" feature within the XRT83L34 device. If the user enables the "Muting upon LOS" feature, then the Receive Section of each channel (within the XRT83L34 device) will automatically MUTE their own RPOS_n/RNEG_n output pins (e.g., force to ground) for the duration that they are declaring the LOS defect condition, as described below. LOW - Disables the "Muting upon LOS" feature for all four (4) HIGH - Enables the "Muting upon LOS" feature. ***NOTES:*** 1. *Internally pulled "Low" with 50kΩ resistor.* 2. *In Hardware mode, all receive channels share the same RXMUTE control function.*
RDY_$\overline{\text{DTACK}}$	73	O	***HOST Mode Operation - Ready or DTACK Output*** See “Ready or DTACK Output/Receive Muting upon LOS Command Input pin:” on page 16.

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RXRES0
RXRES1</td><td>
108
109</td><td>
I</td><td>Receive External Resistor Control Pins - Hardware mode
Receive External Resistor Control Pin 0
Receive External Resistor Control Pin 1
These pins are used to determine the value of the external Receive fixed resistor according to the following table:
<table><tr><th>RXRES1</th><th>RXRES0</th><th>Required Fixed External RX Resistor</th></tr><tr><td>0</td><td>0</td><td>No External Fixed Resistor</td></tr><tr><td>0</td><td>1</td><td>240Ω</td></tr><tr><td>1</td><td>0</td><td>210Ω</td></tr><tr><td>1</td><td>1</td><td>150Ω</td></tr></table>NOTE: These pins are internally pulled “Low” with 50kΩ resistor.</td></tr>
<tr><td>RCLKE

µPTS1</td><td>106</td><td>I</td><td>Receive Clock Edge Select/Microprocessor Type Select Input pin:
The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.
Hardware Mode Operation - Receive Clock Edge Select Input pin - RCLKE:
This input pin permits the user to configure the Receive Section (of each channel within the XRT83L34 device) to update the data (that is output via the RPOS_n/RDATA_n and RNEG_n/LCV_n output pins) upon either the rising edge or falling edge of the RCLK_n output clock signal, as depicted below.
LOW - Configures all four channels to update the RPOS_n/RDATA_n and RNEG_n/LCV_n output pins upon rising edge of RCLK_n.
HIGH - Configures all four channels to update the RPOS_n/RDATA_n and RNEG_n/LCV_n output pins upon the falling edge of RCLK_n.
HOST Mode Operation - Microprocessor Type Select Input pin # 1:
This pin is used to select the microprocessor type. See “Microprocessor Type Select Input Pins/Receive Clock Edge Select/Transmit Clock Edge Select Input Pin:” on page 17.
NOTE: This pin is internally pulled "Low" with a 50kΩ resistor.</td></tr>
</table>

TRANSMITTER SECTIONS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCLKE µPTS2	107	I	**Transmit Clock Edge - Hardware Mode** With this pin set to a "High", transmit input data of all channels are sampled at the rising edge of TCLK_n. With this pin tied "Low", input data are sampled at the falling edge of TCLK_n. **Microprocessor Type Select Input pin 2 - Host Mode** This pin should be tied to GND. µPTS1(pin 106) selects the microprocessor type. See "Microprocessor Type Select Input Pins/Receive Clock Edge Select/Transmit Clock Edge Select Input Pin:" on page 17. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TTIP_0 TTIP_1 TTIP_2 TTIP_3	13 19 84 90	O	**Transmitter Tip Output for Channel _n:** This output pin, along with the corresponding TRING_n output pin, functions as the Transmit DS1/E1 Output signal drivers for the XRT83L34 device. The user is expected to connect this signal and the corresponding TRING_n output signal to a "1:2.45" step-up transformer. Whenever the Transmit Section of (a given channel within the XRT83L34 device) generates and transmits a "positive-polarity" pulse (onto the line), this output pin will be pulsed to a "higher-voltage" than its corresponding TRING_n output pins. Conversely, whenever the Transmit Section (of a given channel within the XRT83L34 device) generates and transmits a "negative-polarity" pulse (onto the line), then this output pin will be pulsed to a "lower-voltage" than that of the TRING_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the "TxON" input pin (or bit-field) to "0".*
TRING_0 TRING_1 TRING_2 TRING_3	15 17 86 88	O	**Transmitter Ring Output for Channel _n:** This output pin, along with the corresponding TTIP_n output pin, functions as the Transmit DS1/E1" output signal drivers for the XRT83L34 device. The user is expected to connect this signal and the corresponding TTIP_n output signal to a "1:2.45" step-up transformer. Whenever the Transmit Section (of a given channel, within the XRT83L34 device) generates and transmits a "positive-polarity" pulse (onto the line), this output pin will be pulsed to a "lower-voltage" than its corresponding TTIP_n output pin. Conversely, whenever the Transmit Section (of a given channel, within the XRT83L34 device) generates and transmits a "negative-polarity" pulse (onto the line) this output pin will be pulsed to a "higher-voltage" than that of the TTIP_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the "TxON" input pin (or bit-field) to "0".*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TPOS_0/ TDATA_0 TPOS_1/ TDATA_1 TPOS_2/ TDATA_2 TPOS_3/ TDATA_3	2 127 104 101	I	**Transmit Positive-Polarity Data Input pin/Transmit Data Input pin:** The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual-Mode, as described below. **Dual-Rail Mode Operation - Transmit Positive-Polarity Data Output - TPOS_n:** For Dual-Rail Applications, the System-Side Terminal Equipment should apply the "positive-polarity" portion of the outbound DS1/E1 data-stream to this input pin. Likewise, the System-Side Terminal Equipment should also apply the "negative-polarity" portion of the outbound DS1/E1 data-stream to the TNEG_n input pin. The Transmit Section of Channel n will sample this input pin (along with TNEG_n) upon the "user-selected" edge of TCLK_n. The Transmit Section of Channel n will generate a "positive-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic "HIGH" level. The Transmit Section of Channel n will NOT generate a "positive-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic "LOW" level. **Single-Rail Mode Operation - Transmit Data Output - TDATA_n:** For Single-Rail Applications, the System-Side Terminal Equipment should apply the entire "outbound" DS1/E1 data-stream to this input pin. The Transmit Section of Channel n will sample this input pin upon the "user-selected" edge of TCLK_n. In the Single-Rail Mode, the internal B8ZS/HDB3 Encoder will be enabled, and the Transmit Section of the Channel will generate and transmit "positive" and "negative-polarity" pulses within the outbound DS1/E1 line signal, based upon this "B8ZS/HDB3 Encoder. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor for each channels.*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TNEG_0/ CODES_0 TNEG_1/ CODES_1 TNEG_2/ CODES_2 TNEG_3/ CODES_3	3 126 105 100	I	**Transmitter Negative-Polarity Data Input/Line Code Select Input:** The exact function of this input pin depends upon the following. • Whether the XRT83L34 device has been configured to operate in the Single-Rail or Dual Mode • Whether the XRT83L34 device has been configure to operate in the HOST or Hardware Mode, as described below ***Dual-Rail Mode Operation - Transmit Negative-Polarity Data Input - TNEG_n:*** For Dual-Rail Applications, the System-Side Terminal Equipment should apply the "negative-polarity" portion of the outbound DS1/E1 data-stream to this input pin. Likewise, the System-Side Terminal Equipment should also apply the "positive-polarity" portion of the outbound DS1/E1 data-stream to the TPOS_n input pin. The Transmit Section of Channel n will sample this input pin (along with TPOS_n) upon the "user-selected" edge of TCLK_n. The Transmit Section of Channel n will generate a "negative-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic "HIGH" level. The Transmit Section of Channel n will NOT generate a "negative-polarity" pulse (via the outbound DS1/E1 line signal) anytime it samples this input pin at a logic LOW" level. ***Single-Rail Mode Operation - Line Code Select Input/NO FUNCTION:*** If the XRT83L34 device has been configured to operate in the Single-Rail Mode, then the exact function of this input pin depends upon whether the chip has been configured to operate in the HOST or Hardware Mode, as described below. **HOST Mode Operation - NO FUNCTION:** If the XRT83L34 device has been configured to operate in both the HOST Mode, and Single-Rail Modes, then this input pin has no function. Since this input pin has an internal pull-down resistor, the user can either leave this pin floating, or he/she can tie this pin to GND. **Hardware Mode Operation - Line Code Select Input pin - CODES_n:** If the XRT83L34 device has been configured to operate in both the Hardware and Single-Rail Modes, then this input pin permits the user to configure a given channel to enable or disable the HDB3/B8ZS Encoder and Decoder blocks as described below. If the user enables the HDB3/B8ZS Encoder and Decoder blocks then the Channel will support the HDB3 line code (for E1 applications) and the B8ZS line code (for T1 applications). If the user disables the HDB3/B8ZS Encoder and Decoder blocks, then the Channel will support the AMI line code (for either T1 and E1 applications). LOW - Enables the HDB3/B8ZS Encoder and Decoder blocks within Channel n. HIGH - Disables the HDB3/B8ZS Encoder and Decoder blocks within Channel n. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for channel _n*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCLK_0 TCLK_1 TCLK_2 TCLK_3	1 128 103 102	I	**Transmit Line Clock Input - Channel n:** The Transmit Section of Channel n will use this input pin to sample and latch the data that is present on the "TPOS_n/TDATA_n" and "TNEG_n" input pins. This input clock signal also functions as the timing source for the "Transmit Direction" signal within the Channel. For T1 Applications, the user is expected to apply a 1.544MHz clock signal to this input pin. Similarly, for E1 Applications, the user is expected to apply a 2.048MHz clock signal to this input pin. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
TAOS_0 TAOS_1 TAOS_2 TAOS_3 $\overline{WR}$_R/$\overline{W}$ $\overline{RD}$_$\overline{DS}$ ALE_$\overline{AS}$ CS	69 70 71 72 69 70 71 72	I	**Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)** The exact function of these input pins depend upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Modes, as described below. **Hardware Mode Operation - Transmit All Ones Command Input - Channel n - TAOS_n:** These input pins permits the user to command a given Channel to transmit an "Unframed, All Ones" pattern (via the outbound DS1/E1 line signal) to the remote terminal equipment. Setting this pin to the logic "HIGH" level configures the Transmit Section (of the corresponding channel) to transmit an Unframed, All Ones pattern via the outbound DS1/E1 line signal. Setting this pin to the logic "LOW" level, configures the Transmit Section (of the corresponding channel) to transmit normal traffic via the outbound DS1/E1 line signal. **Host Mode Operation:** These pins act as various microprocessor functions. See "Microprocessor Interface" on page 13. ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
TXON_0	122	I	**Transmitter Turn On for Channel _0** **Hardware mode** Setting this pin "High" turns on the Transmit Section of Channel _0 and has no control of the Channel_0 receiver. When TXON_0 = "0" then TTIP_0 and TRING_0 driver outputs will be tri-stated. ***NOTE:*** *In **Hardware** mode only, all receiver channels will be turned on upon power-up and there is no provision to power them off. The receive channels can only be independently powered on or off in **Host** mode.* **In Host mode** The TXON_n bits in the channel control registers turn each channel Transmit section ON or OFF. However, control of the on/off function can be transferred to the Hardware pins by setting the TXONCTL bit (bit 6) to "1" in the register at address hex 0x42.
TXON_1	123		**Transmitter Turn On for Channel _1**
TXON_2	124		**Transmitter Turn On for Channel _2**
TXON_3	125		**Transmitter Turn On for Channel _3** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
HW_$\overline{HOST}$	68	I	**HOST/HARDWARE Mode Control Input pin:** This pin permits the user to configure the XRT83L34 device to operate in either the HOST or the Hardware Mode. If the user configures the XRT83L34 device to operate in the HOST Mode, then the Microprocessor Interface block will become active and virtually all configuration settings (within the XRT83L34 device) will be achieved by writing values into the on-chip registers (via the Microprocessor Interface). If the user configures the XRT83L34 device to operate in the Hardware Mode, then the Microprocessor Interface block will be disabled, and all configuration settings (within the XRT83L34 device) will be achieved by setting various input pins to logic HIGH or LOW settings. LOGIC LOW - Configures the XRT83L34 device to operate in the HOST Mode. LOGIC HIGH or FLOATING - Configures the XRT83L34 device to operate in the Hardware Mode. ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
$\overline{WR}$_R/$\overline{W}$	69	I	**Write Strobe/Read-Write Operation Identifier/Transmit All Ones Input Pin - Channel 0:** The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or the Hardware Mode, as described below. ***HOST Mode Operation - Write Strobe/Read-Write Operation Identifier:*** Assuming that the XRT83L34 device has been configured to operate in the Host Mode, then the exact function of the this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - WR* - Write Strobe Input pin:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the WR* (Active-Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Direction Data bus pins, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT83L34) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input pin:** If the Microprocessor Interface is operating in the "Motorola-Asynchronous" Mode, then this pin is functionally equivalent to the R/W* input pin. In the Motorola-Asynchronous Mode, a READ operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. Similarly, a WRITE operation occurs if this input is at a logic "0", coincident to a falling edge of the RD/DS* (Data Strobe) input pin.
TAOS_0	69		***Hardware Mode Operation - Transmit All "Ones" Channel_0 - Hardware Mode*** See "Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)" on page 12. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
$\overline{RD}$_$\overline{DS}$	70	I	**Read Strobe/Data Strobe/Transmit All Ones Command Input - Channel 1:** The exact function of this input pin depends upon whether the XRT83L34 device has been configure to operate in the HOST or Hardware Mode, as described below. ***HOST Mode Operation - READ Strobe/Data Strobe Input:*** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - RD* - READ Strobe Input:** If the MIcroprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the RD* (Active Low READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT83L34 device will place the contents of the addressed register on the Microprocessor Interface Bi-Directional Data Bus (D[7:0]). When this signal is negated, then the Bi-Directional Data Bus will be tri-stated. **Motorola-Asynchronous Mode - DS* - Data Strobe Input:** If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this input pin will function as the DS* (Data Strobe) input signal .
TAOS_1	70		**Hardware Mode Operation - Transmit All One Command Input - Channel 1:** See “Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)” on page 12. ***NOTE:*** *Internally pulled “Low” with a 50kΩ resistor.*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
ALE_AS TAOS_2	71 71	I	**Address Latch Enable/Address Strobe/Transmit All Ones Input - Channel 2:** The exact function of this input pin depend upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. **HOST Mode Operation - Address Latch Enable/Address Strobe Input Pin:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - ALE - Address Latch Enable:** If the Microprocessor Interface (of the XRT83L34 device) has been configured to operate in the Intel-Asynchronous Mode, then this active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[6:0]) into the XRT83L34 Microprocessor Interface bloc and to indicate the start of a READ or WRITE cycle. Pulling this input pin "high" enables the input bus drivers for the Address Bus Input pins (A[6:0]). The contents of the Address Bus will be latched into the XRT83L34 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola Asynchronous Mode - AS* - Address Strobe Input:** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then pulling this input pin "LOW enables the "input" bus drivers for the Address Bus Input pins. During each READ or WRITE operation, the user is expected to drive this input pin "LOW" after (or around the time that) he/she has places the address (of the "target" register) onto the Address Bus pins (A[6:0]). The user is then expected to hold this input pin "LOW" for the remainder of the READ or WRITE cycle. ***NOTE:*** *It is permissible to tie the ALE_AS* and CS* input pins together.. Read and Write operations will be performed properly if ALE_AS is driven "LOW" coincident to whenever CS* is also driven "LOW".* **Hardware Mode Operation - Transmit All "Ones" Channel_2 - Hardware Mode** See "Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)" on page 12. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
CS TAOS_3	72 72	I	**Chip Select Input/Transmit All Ones Input - Channel 3:** The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. **HOST Mode Operation - Chip Select Input pin:** The user must assert this active-low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT83L34 on-chip registers. **Hardware Mode Operation - Transmit All Ones Input - Channel 3:** See "Transmit All Ones Command Input - Channel n: (Hardware Mode ONLY)" on page 12. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION

RDY_$\overline{\text{DTACK}}$
 	
RXMUTE
	73
	
	73
		O
		
		I
			Ready or DTACK Output/Receive Muting upon LOS Command Input pin:
			The exact function of this input pin depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.
			HOST Mode Operation - READY or DTACK Output Pin:
			The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below.
			Intel-Asynchronous Mode - RDY* - Ready Output:
			If the Microprocessor Interface has been configured to operate in the Intel-Asynchronous Mode, then this output pin will function as the "active-low" READY output.
			During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
			If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "high" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
			Motorola-Asynchronous Mode - DTACK* - Data Transfer Acknowledge Output:
			If the Microprocessor interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the "active-low" DTACK output.
			During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor Interface has determined that this input pin has toggled to the logic "low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
			If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "HIGH" level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic "LOW" level.
			
			Receive Muting - Hardware mode
			See “Receive Muting upon LOS Command Input/READY or DTACK Output:” on page 7.
			NOTE: *Internally pulled “Low” with a 50kΩ resistor.*

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>µPTS1
µPTS2</td><td>106
107</td><td>I</td><td>Microprocessor Type Select Input Pins/Receive Clock Edge Select/ Transmit Clock Edge Select Input Pin:
The exact function of these input pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.
HOST Mode Operation - Microprocessor Type Select Input Bits 2 and 1 - µPTS[2:1]:
These two input pins permit the user to configure the Microprocessor Interface to operate in either of the following modes.
• Intel-Asynchronous Mode
• Motorola-Asynchronous Mode
The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below.
<table>
<tr><th>µPTS2</th><th>µPTS1</th><th>µP Type</th></tr>
<tr><td>0</td><td>0</td><td>Intel Asynchronous Mode</td></tr>
<tr><td>0</td><td>1</td><td>Motorola Asynchronous Mode</td></tr>
</table>
NOTE: The µPTS2 (pin107) should be tied to GND. The µPTS1(pin 106) input pin permits the user to selects either the Intel-Asynchronous or the Motorola Asynchronous Modes.

Hardware Mode Operation - Receive Clock Edge Select Input pin:
See “Receive Clock Edge Select/Microprocessor Type Select Input pin:” on page 8.
Hardware Mode Operation - Transmit Clock Edge Select Input pin:
See “Transmit Clock Edge - Hardware Mode” on page 9.
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>RCLKE

TCLKE</td><td>106

107</td><td></td><td></td></tr>
<tr><td>D[7]
D[6]
D[5]
D[4]
D[3]
D[2]/
D[1]/
D[0]/</td><td>42
43
44
45
46
47
48
49</td><td>I/O</td><td>Bi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]:
The exact function of these input/output pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below.
HOST Mode Operation - Bi-Directional Data Bus Input/Output Pins (Microprocessor Interface block) - D[7:0]:
These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs a READ or WRITE operation with the Microprocessor Interface of the XRT83L34 device.</td></tr>
<tr><td>LOOP1_0
LOOP0_0
LOOP1_1
LOOP0_1
LOOP1_2
LOOP0_2
LOOP1_3
LOOP0_3</td><td>42
43
44
45
46
47
48
49</td><td></td><td>Hardware Mode Operation - Loop-back Control pin, Bits [1:0]_Channel_n - Hardware Mode
Pins 42 - 49 control which Loop-Back mode is selected per channel. See “Loop-Back Control Pins - Hardware Mode:” on page 22.
NOTE: Internally pulled “Low” with a 50kΩ resistor.</td></tr>
</table>

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
A[6] A[5] A[4] A[3] A[2] A[1] A[0] JASEL1 JASEL0 EQC4 EQC3 EQC2 EQC1 EQC0	57 58 59 60 61 62 63 57 58 59 60 61 62 63	I	**Address Bus Input Pins/Jitter Attenuator Select Input Pins/Equalizer Control Input pins:** The exact function of these input pins depends upon whether the XRT83L34 device has been configured to operate in the HOST or Hardware Mode, as described below. **HOST Mode Operation - Address Bus Input Pins - A[6:0]:** These pins permits the Microprocessor to identity on-chip registers (within the XRT83L34 device0 whenever it performs READ and WRITE operations with the XRT83L34 device. **Microprocessor Interface Address Bus[6]** **Microprocessor Interface Address Bus[5]** **Microprocessor Interface Address Bus[4]** **Microprocessor Interface Address Bus[3]** **Microprocessor Interface Address Bus[2]** **Microprocessor Interface Address Bus[1]** **Microprocessor Interface Address Bus[0]** **Jitter Attenuator Select Pins - Hardware Mode** **Jitter Attenuator select pin 1** **Jitter Attenuator select pin 0** See "Jitter Attenuator" on page 19. **Equalizer Control Pins - Hardware Mode** **Equalizer Control Input pin 4** **Equalizer Control Input pin 3** **Equalizer Control Input pin 2** **Equalizer Control Input pin 1** **Equalizer Control Input pin 0** Pins EQC[4:0] select the Receive Equalizer and Transmitter Line Build Out. See "Alarm Function//Redundancy Support" on page 21. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
INT TRATIO	119 119	I	**Interrupt Output - Host Mode** This pin goes "Low" to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to "0" in the command control register. **Transmitter Transformer Ratio Select - Hardware mode** The function of this pin is to select the transmitter transformer ratio. See "Alarm Function//Redundancy Support" on page 21. ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*

JITTER ATTENUATOR

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>JASEL0
JASEL1</td><td>58
57</td><td>I</td><td>Jitter Attenuator Select Pins - Hardware Mode
Jitter Attenuator select pin 0
Jitter Attenuator select pin 1
JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it.

<table>
<tr><th rowspan="2">JASEL1</th><th rowspan="2">JASEL0</th><th rowspan="2">JA Path</th><th colspan="2">JA BW Hz</th><th rowspan="2">FIFO Size</th></tr>
<tr><th>T1</th><th>E1</th></tr>
<tr><td>0</td><td>0</td><td>Disabled</td><td>-----</td><td>-----</td><td>--------</td></tr>
<tr><td>0</td><td>1</td><td>Transmit</td><td>3</td><td>10</td><td>32/32</td></tr>
<tr><td>1</td><td>0</td><td>Receive</td><td>3</td><td>10</td><td>32/32</td></tr>
<tr><td>1</td><td>1</td><td>Receive</td><td>3</td><td>1.5</td><td>64/64</td></tr>
</table>
</td></tr>
<tr><td>A[6]
A[5]</td><td>57
58</td><td></td><td>Microprocessor Address Bits A[6:5] -Host Mode
See “Address Bus Input Pins/Jitter Attenuator Select Input Pins/ Equalizer Control Input pins:” on page 18.
NOTE: Internally pulled “Low” with a 50kΩ resistor.</td></tr>
</table>

CLOCK SYNTHESIZER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
MCLKE1	32	I	**E1 Master Clock Input** A 2.048MHz clock for with an accuracy of better than ±50ppm and a duty cycle of 40% to 60% can be provided at this pin. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. ***NOTES:*** *1. All channels of the XRT83L34 must be operated at the same clock rate, either T1, E1 or J1.* *2. Internally pulled "Low" with a 50kΩ resistor.*
CLKSEL0 CLKSEL1 CLKSEL2	37 38 39	I	**Clock Select inputs for Master Clock Synthesizer - Hardware mode** CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an accurate external clock source according to the following table. The MCLKRATE control signal is generated from the state of EQC[4:0] inputs. See Table 4 for description of Transmit Equalizer Control bits. **Host Mode:** The state of these pins are ignored and the master frequency PLL is controlled by the corresponding interface bits. See register address 1000001.

MCLKE1 (kHz)	MCLKT1 (kHz)	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	CLKOUT (KHz)
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544
8	X	0	1	0	0	2048
8	X	0	1	0	1	1544
16	X	0	1	1	0	2048
16	X	0	1	1	1	1544
56	X	1	0	0	0	2048
56	X	1	0	0	1	1544
64	X	1	0	1	0	2048
64	X	1	0	1	1	1544
128	X	1	1	0	0	2048
128	X	1	1	0	1	1544
256	X	1	1	1	0	2048
256	X	1	1	1	1	1544

NOTE: *These pins are internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
MCLKT1	33	I	**T1 Master Clock Input** This signal is an independent 1.544MHz clock for T1 systems with required accuracy of better than ±50ppm and duty cycle of 40% to 60%. MCLKT1 input is used in the T1 mode. ***NOTES:*** *1. All channels of the XRT83L34 must be operated at the same clock rate, either T1, E1 or J1.* *2. See pin 32 description for further explanation for the usage of this pin.* *3. Internally pulled "Low" with a 50kΩ resistor.*
MCLKOUT	36	O	**Synthesized Master Clock Output** This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.

ALARM FUNCTION//REDUNDANCY SUPPORT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
GAUGE	87	I	**Twisted Pair Cable Wire Gauge Select - Hardware mode** Connect this pin "High" to select 26 Gauge wire. Connect this pin "Low" to select 22 and 24 gauge wire for all channels. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
DMO_0	64	O	**Driver Failure Monitor Channel _0** This pin transitions "High" if a short circuit condition is detected in the transmit driver of Channel _0, or no transmit output pulse is detected for more than 128 TCLK_0 cycles.
DMO_1	65		**Driver Failure Monitor Channel _1**
DMO_2	66		**Driver Failure Monitor Channel _2**
DMO_3	67		**Driver Failure Monitor Channel _3**
ATAOS	50	I	**Automatic Transmit "All Ones" Pattern - Hardware Mode Only:** A "High" level on this pin enables the automatic transmission of an "All Ones" AMI pattern from the transmitter of any channel that the receiver of that channel has detected an LOS condition. A "Low" level on this pin disables this function. ***NOTE:*** *All channels share the same ATAOS input control function.* **Microprocessor Clock Input - Host Mode** This pin should be tied to GND for asynchronous microprocessor modes. ***NOTE:*** *This pin is internally pulled "Low" for asynchronous microprocessor interface when no clock is present.*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TRATIO	119	I	**Transmitter Transformer Ratio Select - Hardware Mode** In **external termination mode** (TXSEL = 0), setting this pin "High" selects a transformer ratio of 1:2 for the transmitter. A "Low" on this pin sets the transmitter transformer ratio to 1:2.45. In the **internal termination mode** the transmitter transformer ratio is permanently set to 1:2 and the state of this pin is ignored.
INT		O	**Interrupt Output - Host Mode** This pin is asserted “Low” to indicate an alarm condition. See “Microprocessor Interface” on page 13. ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*
RESET	121	I	**Hardware Reset (Active "Low")** When this pin is tied “Low” for more than 10µs, the device is put in the reset state. Pulling $\overline{\text{RESET}}$ and $\overline{\text{ICT}}$ pins “Low” simultaneously will put the chip in factory test mode. This condition should not be permitted during normal operation. ***NOTE:*** *Internally pulled “High” with a 50kΩ resistor.*
SR/$\overline{\text{DR}}$	16	I	**Single-Rail/Dual-Rail Data Format** Connect this pin "Low" to select transmit and receive data format in **Dual-rail mode**. In this mode, HDB3 or B8ZS encoder and decoder are not available. Connect this pin "High" to select **single-rail data format**. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
			Loop-Back Control Pins - Hardware Mode:
LOOP1_0	42	I/O	**Loop-back control pin 1 - Channel _0**
LOOP0_0	43		**Loop-back control pin 0 - Channel _0**
LOOP1_1	44		**Loop-back control pin 1 - Channel _1**
LOOP0_1	45		**Loop-back control pin 0 - Channel _1**
LOOP1_2	46		**Loop-back control pin 1 - Channel _2**
LOOP0_2	47		**Loop-back control pin 0 - Channel _2**
LOOP1_3	48		**Loop-back control pin 1 - Channel _3**
LOOP0_3	49		**Loop-back control pin 0 - Channel _3**
			Microprocessor R/W Data bits [7:0] - Host Mode These pins are microprocessor data bus pins. See “Bi-Directional Data Bus Pins/Loop-back Control Input Pins - D[7:0]:” on page 17. ***NOTE:*** *These pins are internally pulled “Low” with a 50kΩ resistor.*
D[7]	42		
D[6]	43		
D[5]	44		
D[4]	45		
D[3]	46		
D[2]	47		
D[1]	48		
D[0]	49		

LOOP1_n	LOOP0_n	MODE
0	0	Normal Mode No Loop-back Channel_n
0	1	Local Loop-Back Channel_n
1	0	Remote Loop-Back Channel_n
1	1	Digital Loop-Back Channel_n