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GENERAL DESCRIPTION

The XRT83L38 is a fully integrated Octal (eight channel) long-haul and short-haul line interface unit for T1 (1.544Mbps) 100Ω, E1 (2.048Mbps) 75Ω or 120Ω, or J1 110Ω applications.

In long-haul applications the XRT83L38 accepts signals that have been attenuated from 0 to 36dB at 772kHz in T1 mode (equivalent of 0 to 6000 feet of cable loss) or 0 to 43dB at 1024kHz in E1 mode.

In T1 applications, the XRT83L38 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions (The arbitrary pulse generators are available in both T1 and E1 modes).

The XRT83L38 provides both a parallel **Host** microprocessor interface as well as a **Hardware** mode for programming and control.

Both the B8ZS and HDB3 encoding and decoding functions are selectable as well as AMI. An on-chip crystal-less jitter attenuator with a 32 or 64 bit FIFO can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L38 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. In the absence of the power supply, the transmit outputs and receive inputs are tri-stated allowing for redundancy applications The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

Features (See Page 2)

FIGURE 1. BLOCK DIAGRAM OF THE XRT83L38 T1/E1/J1 LIU (HOST MODE)

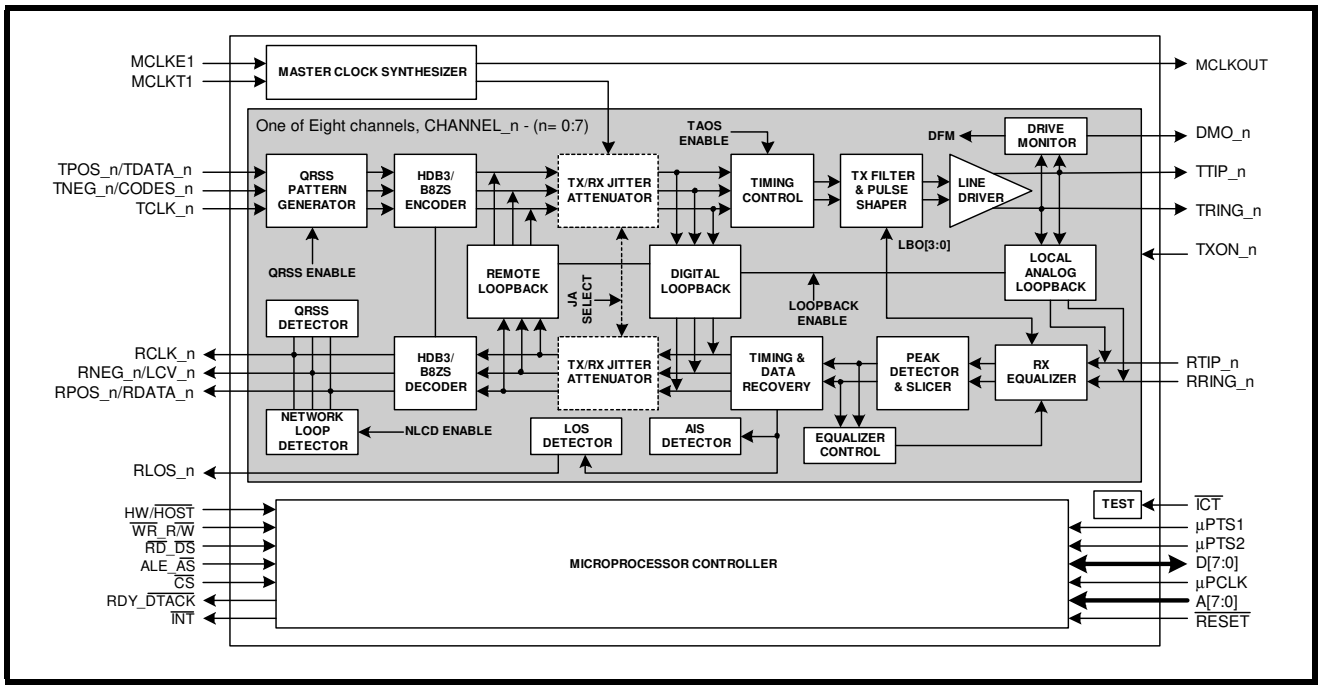
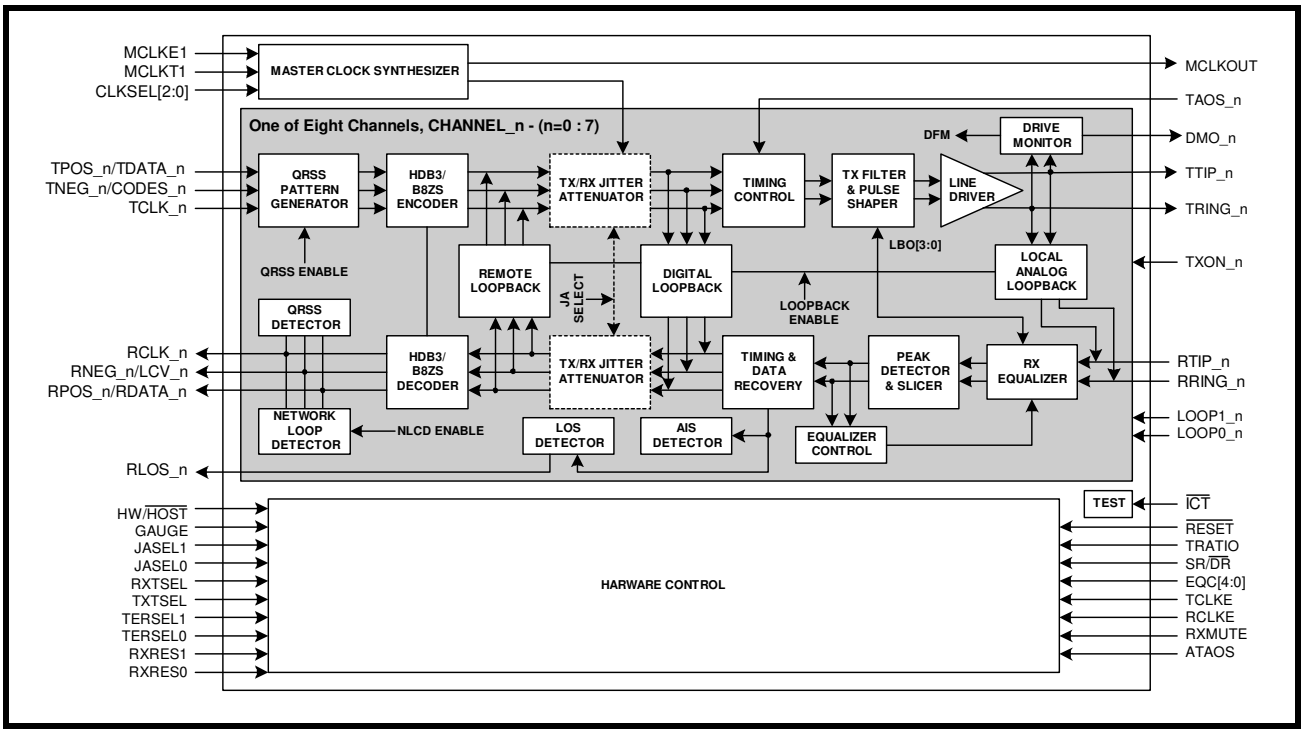


FIGURE 2. BLOCK DIAGRAM OF THE XRT83L38 T1/E1/J1 LIU (HARDWARE MODE)



FEATURES

- Fully integrated eight channel long-haul or short-haul transceivers for E1,T1 or J1 applications
- Adaptive Receive Equalizer for up to 36dB cable attenuation
- Programable Transmit Pulse Shaper for E1,T1 or J1 short-haul interfaces
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping available for both T1 and E1 modes
- Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps
- Selectable receiver sensitivity from 0 to 36dB cable loss for T1 @772kHz and 0 to 43dB for E1 @1024kHz
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for E1 and 0 to 3dB of cable attenuation for T1 modes
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications
- Internal and/or external impedance matching for 75Ω, 100Ω, 110Ω and 120Ω
- Tri-State transmit output and receive input capability for redundancy applications
- Provides High Impedance for Tx and Rx during power off
- Transmit return loss meets or exceeds ETSI 300-166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- High receiver interference immunity
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Receive loss of signal (RLOS) output

- On-chip HDB3/B8ZS/AMI encoder/decoder functions
- QRSS pattern generator and detection for testing and monitoring
- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Local Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both **Hardware** and **Host** (parallel Microprocessor) interface for programming
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Single 3.3V Supply Operation
- 225 ball BGA package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L38IB	225 Ball BGA	-40°C to +85°C

FIGURE 3. PACKAGE PIN OUT

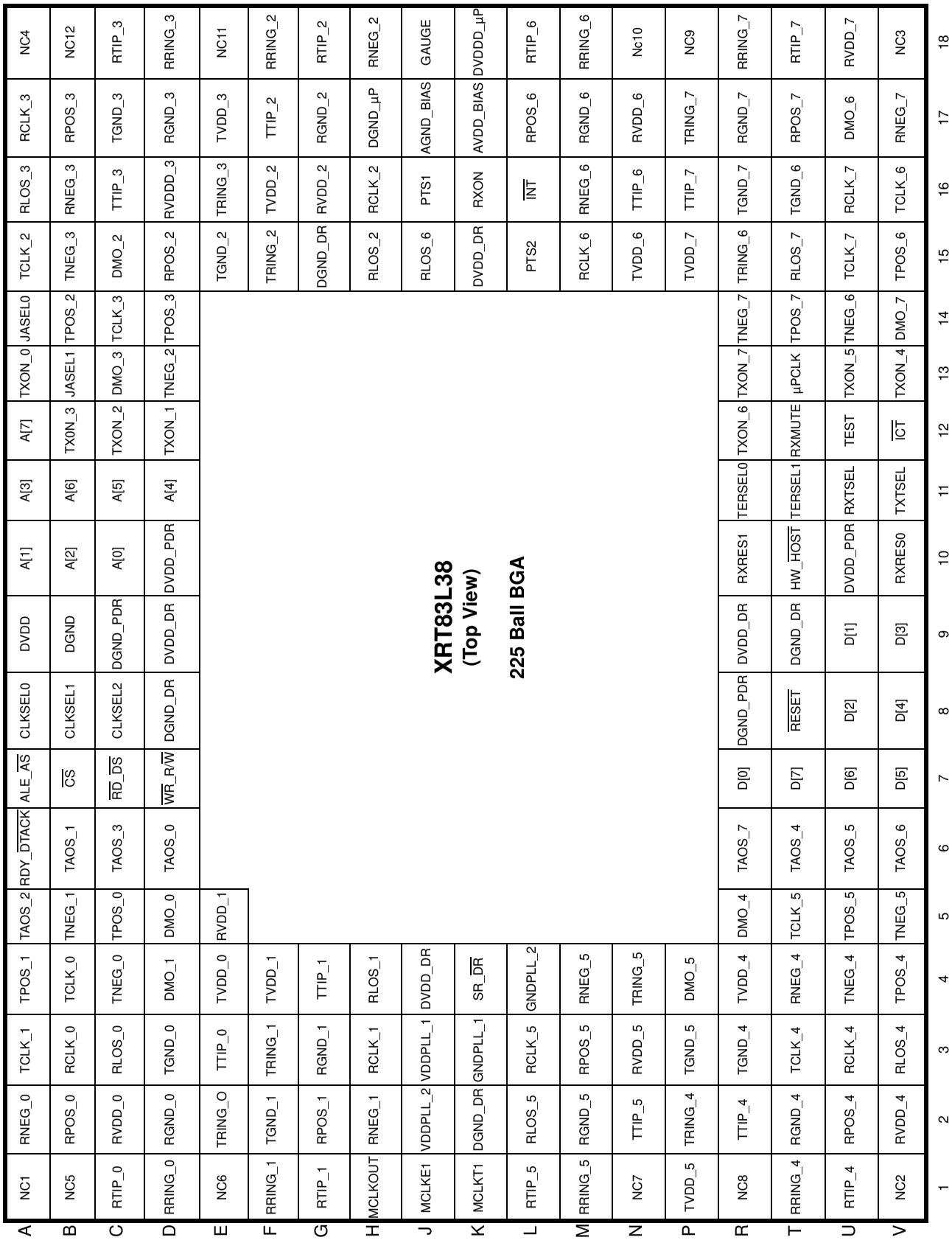


TABLE OF CONTENTS

PIN DESCRIPTION BY FUNCTION

RECEIVE SECTIONS

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RLOS_0	C3	**O**	**Receiver Loss of Signal for Channel_ 0:** This output signal goes "High" for at least one RCLK_0 cycle to indicate loss of signal at the receive 0 input. RLOS will remain "High" for the entire duration of the Loss of Signal detected by the receiver logic. **SEE"RECEIVER LOSS OF SIGNAL (RLOS)" ON PAGE 24.**
RLOS_1	H4		**Receiver Loss of Signal for Channel _1**
RLOS_2	H15		**Receiver Loss of Signal for Channel _2**
RLOS_3	A16		**Receiver Loss of Signal for Channel _3**
RLOS_4	V3		**Receiver Loss of Signal for Channel _4**
RLOS_5	L2		**Receiver Loss of Signal for Channel_ 5**
RLOS_6	J15		**Receiver Loss of Signal for Channel _6**
RLOS_7	T15		**Receiver Loss of Signal for Channel _7**
RCLK_0	B3	**O**	**Receiver Clock Output for Channel _0**
RCLK_1	H3		**Receiver Clock Output for Channel _1**
RCLK_2	H16		**Receiver Clock Output for Channel _2**
RCLK_3	A17		**Receiver Clock Output for Channel _3**
RCLK_4	U3		**Receiver Clock Output for Channel _4**
RCLK_5	L3		**Receiver Clock Output for Channel _5**
RCLK_6	M15		**Receiver Clock Output for Channel _6**
RCLK_7	U16		**Receiver Clock Output for Channel _7**
RNEG_0	A2	**O**	**Receiver Negative Data Output for Channel_0 - Dual-Rail mode** This signal is the receive negative-rail output data.
LCV_0	A2		**Line Code Violation Output for Channel_0 - Single-Rail mode** This signal goes "High" for one RCLK_0 cycle to indicate a code violation is detected in the received data of Channel _0. If AMI coding is selected, every bipolar violation received will cause this pin to go "High".
RNEG_1	H2		**Receiver Negative Data Output for Channel _1**
LCV_1			**Line Code Violation Output for Channel _1**
RNEG_2	H18		**Receiver Negative Data Output for Channel _2**
LCV_2			**Line Code Violation Output for Channel _2**
RNEG_3	B16		**Receiver Negative Data Output for Channel _3**
LCV_3			**Line Code Violation Output for Channel _3**
RNEG_4	T4		**Receiver Negative Data Output for Channel _4**
LCV_4			**Line Code Violation Output for Channel _4**
RNEG_5	M4		**Receiver Negative Data Output for Channel _5**
LCV_5			**Line Code Violation Output for Channel _5**
RNEG_6	M16		**Receiver Negative Data Output for Channel _6**
LCV_6			**Line Code Violation Output for Channel _6**
RNEG_7	V17		**Receiver Negative Data Output for Channel _7**
LCV_7			**Line Code Violation Output for Channel _7**

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RPOS_0	B2	**O**	**Receiver Positive Data Output for Channel _0 - Dual-Rail mode** This signal is the receive positive-rail output data sent to the Framer.
RDATA_0	B2		**Receiver NRZ Data Output for Channel _0 - Single-Rail mode** This signal is the receive output data.
RPOS_1	G2		**Receiver Positive Data Output for Channel _1** **Receiver NRZ Data Output for Channel _1**
RDATA_1			**Receiver Positive Data Output for Channel _2**
RPOS_2	D15		**Receiver NRZ Data Output for Channel _2**
RDATA_2			**Receiver Positive Data Output for Channel _3**
RPOS_3	B17		**Receiver NRZ Data Output for Channel _3**
RDATA_3			**Receiver Positive Data Output for Channel _4**
RPOS_4	U2		**Receiver NRZ Data Output for Channel _4**
RDATA_4			**Receiver Positive Data Output for Channel _5**
RPOS_5	M3		**Receiver NRZ Data Output for Channel _5**
RDATA_5			**Receiver Positive Data Output for Channel _6**
RPOS_6	L17		**Receiver NRZ Data Output for Channel 6**
RDATA_6			**Receiver Positive Data Output for Channel _7**
RPOS_7	T17		**Receiver NRZ Data Output for Channel _7**
RDATA_7			
RTIP_0	C1	**I**	**Receiver Differential Tip Input for Channel _0** Positive differential receive input from the line
RTIP_1	G1		**Receiver Differential Tip Input for Channel _1**
RTIP_2	G18		**Receiver Differential Tip Input for Channel _2**
RTIP_3	C18		**Receiver Differential Tip Input for Channel _3**
RTIP_4	U1		**Receiver Differential Tip Input for Channel _4**
RTIP_5	L1		**Receiver Differential Tip Input for Channel _5**
RTIP_6	L18		**Receiver Differential Tip Input for Channel _6**
RTIP_7	T18		**Receiver Differential Tip Input for Channel _7**
RRING_0	D1	**I**	**Receiver Differential Ring Input for Channel _0** Negative differential receive input from the line
RRING_1	F1		**Receiver Differential Ring Input for Channel _1**
RRING_2	F18		**Receiver Differential Ring Input for Channel _2**
RRING_3	D18		**Receiver Differential Ring Input for Channel _3**
RRING_4	T1		**Receiver Differential Ring Input for Channel _4**
RRING_5	M1		**Receiver Differential Ring Input for Channel _5**
RRING_6	M18		**Receiver Differential Ring Input for Channel _6**
RRING_7	R18		**Receiver Differential Ring Input for Channel _7**
RXMUTE	T12	**I**	**Receive Data Muting** When a LOS condition occurs, the outputs RPOS_n/RNEG_n will be muted, (forced to ground) to prevent data chattering. Tie this pin "Low" to disable the muting function. ***NOTES:*** *1. This pin is internally pulled "High" with a 50kΩ resistor.* *2. In **Hardware mode**, all receive channels share the same RXMUTE control function.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RXRES1 **RXRES0**	R10 V10	**I**	**Receive External Resistor Control Pins - Hardware mode** **Receive External Resistor Control Pin 1:** **Receive External Resistor Control Pin 0:** These pins determine the value of the external Receive fixed resistor according to the following table: **RXRES1 / RXRES0 / Required Fixed External RX Resistor** **0 / 0 / No External Fixed Resistor** **0 / 1 / 240Ω** **1 / 0 / 210Ω** **1 / 1 / 150Ω** ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
RCLKE	J16	**I**	**Receive Clock Edge - Hardware mode** Set this pin "High" to sample RPOS_N/RNEG_n on the falling edge of RCLK_n. With this pin tied "Low", output data are updated on the rising edge of RCLK_n.
µPTS1	J16		**Microprocessor Type Select Input pin 1 - Host mode** This pin along with µPTS2 (pin 128) is used to select the microprocessor type. **SEE"MICROPROCESSOR TYPE SELECT INPUT PINS - HOST MODE:" ON PAGE 12.** ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*

TRANSMITTER SECTIONS

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TCLKE	L15	**I**	**Transmit Clock Edge - Hardware mode** Set this pin "High" to sample transmit input data on the rising edge of TCLK_n. With this pin tied "Low", input data are sampled on the falling edge of TCLK_n.
µPTS2	L15		**Microprocessor Type Select Input pin 2 - Host mode** This pin along with µPTS1 (pin 133) selects the microprocessor type. **SEE"MICROPROCESSOR TYPE SELECT INPUT PINS - HOST MODE:" ON PAGE 12.** ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TTIP_0	E3	**O**	**Transmitter Tip Output for Channel _0** Positive differential transmit output to the line.
TTIP_1	G4		**Transmitter Tip Output for Channel _1**
TTIP_2	F17		**Transmitter Tip Output for Channel _2**
TTIP_3	C16		**Transmitter Tip Output for Channel _3**
TTIP_4	R2		**Transmitter Tip Output for Channel _4**
TTIP_5	N2		**Transmitter Tip Output for Channel _5**
TTIP_6	N16		**Transmitter Tip Output for Channel _6**
TTIP_7	P16		**Transmitter Tip Output for Channel _7**

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TRING_0	E2	**O**	**Transmitter Ring Output for Channel _0** Negative differential transmit output to the line.
TRING_1	F3		**Transmitter Ring Output for Channel _1**
TRING_2	F15		**Transmitter Ring Output for Channel _2**
TRING_3	E16		**Transmitter Ring Output for Channel _3**
TRING_4	P2		**Transmitter Ring Output for Channel _4**
TRING_5	N4		**Transmitter Ring Output for Channel _5**
TRING_6	R15		**Transmitter Ring Output for Channel _6**
TRING_7	P17		**Transmitter Ring Output for Channel _7**
TPOS_0	C5	**I**	**Transmitter Positive Data Input for Channel _0 - Dual-Rail mode** This signal is the positive-rail input data for transmitter 0.
TDATA_0			**Transmitter 0 Data Input - Single-Rail mode** This pin is used as the NRZ input data for transmitter 0.
TPOS_1	A4		**Transmitter Positive Data Input for Channel _1**
TDATA_1			**Transmitter 1 Data Input**
TPOS_2	B14		**Transmitter Positive Data Input for Channel _2**
TDATA_2			**Transmitter 2 Data Input**
TPOS_3	D14		**Transmitter Positive Data Input for Channel _3**
TDATA_3			**Transmitter 3 Data Input**
TPOS_4	V4		**Transmitter Positive Data Input for Channel _4**
TDATA_4			**Transmitter 4 Data Input**
TPOS_5	U5		**Transmitter Positive Data Input for Channel _5**
TDATA_5			**Transmitter 5 Data Input**
TPOS_6	V15		**Transmitter Positive Data Input for Channel _6**
TDATA_6			**Transmitter 6 Data Input**
TPOS_7	T14		**Transmitter Positive Data Input for Channel _7**
TDATA_7			**Transmitter 7 Data Input** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for each channel.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TNEG_0	C4	**I**	**Transmitter Negative NRZ Data Input for Channel _0** **Dual-Rail mode** This signal is the negative-rail input data for transmitter 0. **Single-Rail mode** This pin can be left unconnected.
CODES_0	C4		**Coding Select for Channel _0 - Hardware mode and Single-Rail mode** Connecting this pin "Low" enables HDB3 in E1 or B8ZS in T1 encoding and decoding for Channel _0. Connecting this pin "High" selects AMI data format.
TNEG_1	B5		**Transmitter Negative NRZ Data Input for Channel _1**
CODES_1			**Coding Select for Channel _1**
TNEG_2	D13		**Transmitter Negative NRZ Data Input for Channel _2**
CODES_2			**Coding Select for Channel _2**
TNEG_3	B15		**Transmitter Negative NRZ Data Input for Channel _3**
CODES_3			**Coding Select for Channel _3**
TNEG_4	U4		**Transmitter Negative NRZ Data Input for Channel _4**
CODES_4			**Coding Select for Channel _4**
TNEG_5	V5		**Transmitter Negative NRZ Data Input for Channel _5**
CODES_5			**Coding Select for Channel _5**
TNEG_6	U14		**Transmitter Negative NRZ Data Input for Channel _6**
CODES_6			**Coding Select for Channel _6**
TNEG_7	R14		**Transmitter Negative NRZ Data Input for Channel _7**
CODES_7			**Coding Select for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for each channel.*
TCLK_0	B4	**I**	**Transmitter Clock Input for Channel _0 - Host mode and Hardware mode** **E1** rate at 2.048MHz ± 50ppm. **T1** rate at 1.544MHz ± 32ppm. During normal operation TCLK_0 is used for sampling input data at TPOS_0/ TDATA_0 and TNEG_0/CODES_0 while MCLK is used as the timing reference for the transmit pulse shaping circuit.
			Transmitter Clock Input for Channel _1
TCLK_1	A3		**Transmitter Clock Input for Channel _2**
TCLK_2	A15		**Transmitter Clock Input for Channel _3**
TCLK_3	C14		**Transmitter Clock Input for Channel _4**
TCLK_4	T3		**Transmitter Clock Input for Channel _5**
TCLK_5	T5		**Transmitter Clock Input for Channel _6**
TCLK_6	V16		**Transmitter Clock Input for Channel _7**
TCLK_7	U15		***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TAOS_0	D6	**I**	**Transmit All Ones for Channel _0 - Hardware mode** Setting this pin "High" enables the transmission of an "All Ones" Pattern from Channel _0. A "Low" level stops the transmission of the "All Ones" Pattern. **Transmit All Ones for Channel _1** **Transmit All Ones for Channel _2** **Transmit All Ones for Channel _3** **Transmit All Ones for Channel _4** **Transmit All Ones for Channel _5** **Transmit All Ones for Channel _6** **Transmit All Ones for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
TAOS_1	B6		
TAOS_2	A5		
TAOS_3	C6		
TAOS_4	T6		
TAOS_5	U6		
TAOS_6	V6		
TAOS_7	R6		
TXON_0	A13	**I**	**Transmitter Turn On for Channel _0** **Hardware mode** Setting this pin "High" turns on the Transmit and Receive Sections of Channel _0. When TXON_0 = "0" then TTIP_0 and TRING_0 driver outputs will be tri-stated. **In Host mode** The TXON_n bits in the channel control registers turn each channel Transmit and Receive section ON or OFF. However, control of the on/off function can be transferred to the **Hardware** pins by setting the TXONCNTL bit (bit 7) to "1" in the register at address hex 0x82. **Transmitter Turn On for Channel _1** **Transmitter Turn On for Channel _2** **Transmitter Turn On for Channel _3** **Transmitter Turn On for Channel _4** **Transmitter Turn On for Channel _5** **Transmitter Turn On for Channel _6** **Transmitter Turn On for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
TXON_1	D12		
TXON_2	C12		
TXON_3	B12		
TXON_4	V13		
TXON_5	U13		
TXON_6	R12		
TXON_7	R13		

MICROPROCESSOR INTERFACE

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
HW_$\overline{\text{HOST}}$	T10	I	**Mode Control Input** This pin selects **Hardware** or **Host mode**. Leave this pin unconnected or tie "High" to select **Hardware mode**. For **Host mode**, this pin must be tied "Low". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
$\overline{\text{WR}}$_R/$\overline{\text{W}}$	D7	I	**Write Input (Read/Write) - Host mode:** **Intel bus timing**: A "Low" pulse on $\overline{\text{WR}}$ selects a write operation when $\overline{\text{CS}}$ pin is "Low". **Motorola bus timing:** A "High" pulse on R/$\overline{\text{W}}$ selects a read operation and a "Low" pulse on R/$\overline{\text{W}}$ selects a write operation when $\overline{\text{CS}}$ is "Low".
EQC0	D7		**Equalizer Control Input pin 0 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 30.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{RD}}$_$\overline{\text{DS}}$	C7	I	**Read Input (Data Strobe) - Host mode** **Intel bus timing:** A "Low" pulse on $\overline{\text{RD}}$ selects a read operation when the $\overline{\text{CS}}$ pin is "Low". **Motorola bus timing:** A "Low" pulse on $\overline{\text{DS}}$ indicates a read or write operation when the $\overline{\text{CS}}$ pin is "Low".
EQC1	C7		**Equalizer Control Input pin 1 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 30.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
ALE_$\overline{\text{AS}}$	A7	I	**Address Latch Input (Address Strobe) - Host mode** **Intel bus timing:** The address inputs are latched into the internal register on the falling edge of ALE. **Motorola bus timing:** The address inputs are latched into the internal register on the falling edge of $\overline{\text{AS}}$.
EQC2	A7		**Equalizer Control Input pin 2 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 30.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{CS}}$	B7	I	**Chip Select Input - Host mode:** This signal must be "Low" in order to access the parallel port.
EQC3	B7		**Equalizer Control Input pin 3 - Hardware mode:** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 30.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

<table>
<tr><th>SIGNAL NAME</th><th>LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RDY_DTACK</td><td>A6</td><td>O</td><td>Ready Output (Data Transfer Acknowledge Output) - Host mode
Intel bus timing: RDY is asserted “High” to indicate the device has completed a read or write operation.
Motorola bus timing: $\overline{\text{DTACK}}$ is asserted “Low” to indicate the device has completed a read or write cycle.</td></tr>
<tr><td>EQC4</td><td>A6</td><td>I</td><td>Equalizer Control Input pin 4 - Hardware mode
Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. SEE”RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS” ON PAGE 30.
NOTE: Internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>µPTS1
µPTS2</td><td>J16
L15</td><td>I</td><td>Microprocessor Type Select Input Pins - Host Mode:
Microprocessor Type Select Input Bit 1
Microprocessor Type Select Input Bit 2
<table>
<tr><th>µPTS2</th><th>µPTS1</th><th>µP Type</th></tr>
<tr><td>0</td><td>0</td><td>68HC11, 8051, 80C188 (async.)</td></tr>
<tr><td>0</td><td>1</td><td>Motorola 68K (async.)</td></tr>
<tr><td>1</td><td>0</td><td>Intel x86 (sync.)</td></tr>
<tr><td>1</td><td>1</td><td>Motorola 860 (sync.)</td></tr>
</table></td></tr>
<tr><td>RCLKE</td><td>J16</td><td></td><td>Receive Clock Edge - Hardware mode
SEE”RECEIVE CLOCK EDGE - HARDWARE MODE” ON PAGE 7.</td></tr>
<tr><td>TCLKE</td><td>L15</td><td></td><td>Transmit Clock Edge - Hardware mode
SEE”TRANSMIT CLOCK EDGE - HARDWARE MODE” ON PAGE 7.
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td></td><td></td><td>I/O</td><td>Microprocessor Read/Write Data Bus Pins - Host mode</td></tr>
<tr><td>D[7]</td><td>T7</td><td></td><td>Data Bus[7]</td></tr>
<tr><td>D[6]</td><td>U7</td><td></td><td>Data Bus[6]</td></tr>
<tr><td>D[5]</td><td>V7</td><td></td><td>Data Bus[5]</td></tr>
<tr><td>D[4]</td><td>V8</td><td></td><td>Data Bus[4]</td></tr>
<tr><td>D[3]</td><td>V9</td><td></td><td>Data Bus[3]</td></tr>
<tr><td>D[2]</td><td>U8</td><td></td><td>Data Bus[2]</td></tr>
<tr><td>D[1]</td><td>U9</td><td></td><td>Data Bus[1]</td></tr>
<tr><td>D[0]</td><td>R7</td><td></td><td>Data Bus[0]</td></tr>
<tr><td>LOOP1_4
LOOP0_4
LOOP1_5
LOOP0_5
LOOP1_6
LOOP0_6
LOOP1_7
LOOP0_7</td><td>T7
U7
V7
V8
V9
U8
U9
R7</td><td></td><td>Loop-back Control Pins, Bits [1:0] Channel_[7:4] - Hardware Mode
Pins 67-74 and 173-180 control which Loop-Back mode is selected per channel. SEE”LOOP-BACK CONTROL PINS, BITS [1:0] CHANNEL_[7:0]” ON PAGE 17.
NOTE: Internally pulled “Low” with a 50kΩ resistor for all channels.</td></tr>
</table>

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
			Microprocessor Interface Address Bus Pins - Host mode:
A[7]	A12	**I**	**Microprocessor Interface Address Bus[7]**
A[6]	B11		**Microprocessor Interface Address Bus[6]**
A[5]	C11		**Microprocessor Interface Address Bus[5]**
A[4]	D11		**Microprocessor Interface Address Bus[4]**
A[3]	A11		**Microprocessor Interface Address Bus[3]**
A[2]	B10		**Microprocessor Interface Address Bus[2]**
A[1]	A10		**Microprocessor Interface Address Bus[1]**
A[0]	C10		**Microprocessor Interface Address Bus[0]**
			Loop-back Control Pins, Bits [1:0] Channel_[3:0]
LOOP1_3	A12		In **Hardware mode**, pins 67-74 and 173-180 control which Loop-Back mode is selected per channel. **SEE"LOOP-BACK CONTROL PINS, BITS [1:0] CHANNEL_[7:0]" ON PAGE 17.**
LOOP0_3	B11		
LOOP1_2	C11		
LOOP0_2	D11		***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
LOOP1_1	A11		
LOOP0_1	B10		
LOOP1_0	A10		
LOOP0_0	C10		
µPCLK	T13	**I**	**Microprocessor Clock Input - Host Mode:** Input clock for synchronous microprocessor operation. Maximum clock rate is 54 MHz. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor for asynchronous microprocessor interface when no clock is present.*
ATAOS	T13		**Automatic Transmit "All Ones" - Hardware mode** This pin functions as an Automatic Transmit "All Ones". **SEE"AUTOMATIC TRANSMIT "ALL ONES" PATTERN - HARDWARE MODE" ON PAGE 16.**
$\overline{INT}$	L16	**O**	**Interrupt Output - Host mode** This pin goes "Low" to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to a "0" in the command control register.
TRATIO	L16	**I**	**Transmitter Transformer Ratio Select - Hardware mode** The function of this pin is to select the transmitter transformer ratio. **SEE"TRANSMITTER TRANSFORMER RATIO SELECT - HARDWARE MODE" ON PAGE 16.** ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*

JITTER ATTENUATOR

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
JASEL0 JASEL1	A14 B13	I	**Jitter Attenuator Select Pins Hardware Mode** **Jitter Attenuator select Bit 0** **Jitter Attenuator select Bit 1** JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it. **NOTE:** *These pins are internally pulled "Low" with 50kΩ resistors.*

JASEL1	JASEL0	JA Path	JA BW Hz		FIFO Size
			T1	E1	
0	0	Disabled	-----	-----	--------
0	1	Transmit	3	10	32/32
1	0	Receive	3	10	32/32
1	1	Receive	3	1.5	64/64

CLOCK SYNTHESIZER

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
MCLKOUT	H1	O	**Synthesized Master Clock Output** This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.
MCLKT1	K1	I	**T1 Master Clock Input** This signal is an independent 1.544MHz clock for T1 systems with accuracy better than ±50ppm and duty cycle within 40% to 60%. MCLKT1 is used in the T1 mode. **NOTES:** 1. *All channels of the XRT83L38 must be operated at the same clock rate, either T1, E1 or J1.* 2. *See pin 26 description for further explanation for the usage of this pin.* 3. *Internally pulled "Low" with a 50kΩ resistor.*
MCLKE1	J1	I	**E1 Master Clock Input** A 2.048MHz clock for with an accuracy of better than ±50ppm and a duty cycle of 40% to 60% can be provided at this pin. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. **NOTES:** 1. *All channels of the XRT83L38 must be operated at the same clock rate, either T1, E1 or J1.* 2. *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
CLKSEL0 **CLKSEL1** **CLKSEL2**	A8 B8 C8	**I**	**Clock Select inputs for Master Clock Synthesizer - Hardware mode** CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the table below. In **Hardware mode,** the MCLKRATE control signal is generated from the state of EQC[4:0] inputs. In **Host mode,** the state of these pins are ignored and the master frequency PLL is controlled by the corresponding interface bits. See **Table 36** register address 10000001

MCLKE1 kHz	MCLKT1 kHz	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	CLKOUT/ kHz
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544
8	X	0	1	0	0	2048
8	X	0	1	0	1	1544
16	X	0	1	1	0	2048
16	X	0	1	1	1	1544
56	X	1	0	0	0	2048
56	X	1	0	0	1	1544
64	X	1	0	1	0	2048
64	X	1	0	1	1	1544
128	X	1	1	0	0	2048
128	X	1	1	0	1	1544
256	X	1	1	1	0	2048
256	X	1	1	1	1	1544

NOTE: *These pins are internally pulled "Low" with a 50kΩ resistor.*

ALARM FUNCTIONS/REDUNDANCY SUPPORT

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
GAUGE	J18	**I**	**Twisted Pair Cable Wire Gauge Select - Hardware Mode** Connect this pin "High" to select 26 Gauge wire. Connect this pin "Low" to select 22 and 24 gauge wire for all channels. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
DMO_0	D5	**O**	**Driver Failure Monitor Channel _0:** This pin transitions "High" if a short circuit condition is detected in the transmit driver of Channel _0, or no transmit output pulse is detected for more than 128 TCLK_0 cycles.
			Driver Failure Monitor Channel _1
DMO_1	D4		**Driver Failure Monitor Channel _2**
DMO_2	C15		**Driver Failure Monitor Channel _3**
DMO_3	C13		**Driver Failure Monitor Channel _4**
DMO_4	R5		**Driver Failure Monitor Channel _5**
DMO_5	P4		**Driver Failure Monitor Channel _6**
DMO_6	U17		**Driver Failure Monitor Channel _7**
DMO_7	V14		
ATAOS	T13	**I**	**Automatic Transmit "All Ones" Pattern - Hardware Mode** A "High" level on this pin enables the automatic transmission of an "All Ones" AMI pattern from the transmitter of any channel that the receiver of that channel has detected an LOS condition. A "Low" level on this pin disables this function. *Note: All channels share the same ATAOS control function.*
			Microprocessor Clock Input - Host mode
µPCLK	T13		**SEE"MICROPROCESSOR CLOCK INPUT - HOST MODE:" ON PAGE 13.** ***NOTE:*** *This pin is internally pulled "Low" for asynchronous microprocessor interface when no clock is present.*
TRATIO	L16	**I**	**Transmitter Transformer Ratio Select - Hardware mode** In **external termination mode** (TXTSEL = 0), setting this pin "High" selects a transformer ratio of 1:2 for the transmitter. A "Low" on this pin sets the transmitter transformer ratio to 1:2.45. In the **internal termination mode** the transmitter transformer ratio is permanently set to 1:2 and the state of this pin is ignored.
			Interrupt Output - Host mode
$\overline{\text{INT}}$	L16	**O**	This pin is asserted "Low" to indicate an alarm condition. **SEE"INTERRUPT OUTPUT - HOST MODE" ON PAGE 13.** ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*
$\overline{\text{RESET}}$	T8	**I**	**Hardware Reset (Active "Low"):** When this pin is tied "Low" for more than 10µs, the device is put in the reset state. **Exar recommends initiating a Harware reset upon power up.** ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor.*
SR/$\overline{\text{DR}}$	K4	**I**	**Single-Rail/Dual-Rail Data Format:** Connect this pin "Low" to select transmit and receive data format in **Dual-Rail mode**. In this mode, HDB3 or B8ZS encoder and decoder are not available. Connect this pin "High" to select **single-rail data format**. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
			Loop-back Control Pins, Bits [1:0] Channel_[7:0]
LOOP1_0	A10	**I**	**Loop-back Control bit 1, Channel _0**
LOOP0_0	C10		**Loop-back Control bit 0, Channel _0**
LOOP1_1	A11		**Loop-back Control bit 1, Channel _1**
LOOP0_1	B10		**Loop-back Control bit 0, Channel _1**
LOOP1_2	C11		**Loop-back Control bit 1, Channel _2**
LOOP0_2	D11		**Loop-back Control bit 0, Channel _2**
LOOP1_3	A12		**Loop-back Control bit 1, Channel _3**
LOOP0_3	B11		**Loop-back Control bit 0, Channel _3**
LOOP1_4	T7		**Loop-back Control bit 1, Channel _4**
LOOP0_4	U7		**Loop-back Control bit 0, Channel _4**
LOOP1_5	V7		**Loop-back Control bit 1, Channel _5**
LOOP0_5	V8		**Loop-back Control bit 0, Channel _5**
LOOP1_6	V9		**Loop-back Control bit 1, Channel _6**
LOOP0_6	U8		**Loop-back Control bit 0, Channel _6**
LOOP1_7	U9		**Loop-back Control bit 1, Channel _7**
LOOP0_7	R7		**Loop-back Control bit 0, Channel _7** **In Hardware mode**, these pins control the Loop-Back mode for each channel_n per the following table.

LOOP1_n	LOOP0_n	MODE
0	0	Normal Mode No Loop-Back Channel_n
0	1	Local Loop-Back Channel_n
1	0	Remote Loop-Back Channel_n
1	1	Digital Loop-Back Channel_n

A[1]	A10		**Microprocessor Address A[7:0] and Data Bus Pins D[7:0] - Host mode** These pins are microprocessor address and data bus pins. **SEE"MICROPROCESSOR INTERFACE ADDRESS BUS PINS - HOST MODE:" ON PAGE 13.** and **see "Microprocessor Read/Write Data Bus Pins - Host mode" on page 12.** ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
A[0]	C10		
A[3]	A11		
A[2]	B10		
A[5]	C11		
A[4]	D11		
A[7]	A12		
A[6]	B11		
D[7]	T7		
D[6]	U7		
D[5]	V7		
D[4]	V8		
D[3]	V9		
D[2]	U8		
D[1]	U9		
D[0]	R7		

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
EQC4 **EQC3** **EQC2** **EQC1** **EQC0** **RDY_DTACK** **CS** **ALE_AS** **RD_DS** **WR_R/W**	A6 B7 A7 C7 D7 A6 B7 A7 C7 D7	**I** **O** **I** **I** **I** **I**	**Equalizer Control Input 4 - Hardware mode** This pin together with pins EQC[3:0] is used to control the transmit pulse shaping, transmit line build-out (LBO) and receive monitoring while operating at one of either the T1, E1 or J1 clock rates/modes. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 30.** for description of Transmit Equalizer Control bits. **Equalizer Control Input 3** **Equalizer Control Input 2** **Equalizer Control Input 1** **Equalizer Control Input 0** ***NOTES:*** 1. *In **Hardware mode** all transmit channels share the same pulse setting controls function.* 2. *All channels of an XRT83L38 must operate at the same clock rate, either the T1, E1 or J1 modes.* In **Host mode**, these pins perform various microprocessor functions. **SEE"MICRO-PROCESSOR INTERFACE" ON PAGE 11.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
RXTSEL	U11	**I**	**Receiver Termination Select** In **Hardware mode**, when this pin is "Low" the receive line termination is determined only by an external resistor. When "High", the receive termination is realized by the internal resistor or the combination of internal and external resistors. These conditions are described in the table below. ***NOTE:*** *In **Hardware mode** all channels share the same RXTSEL control function.* **RXTSEL** / **RX Termination**: **0** = **External**; **1** = **Internal** In **Host mode**, the RXTSEL_n bits in the channel control registers determine if the receiver termination is external or internal. However, the function of RXTSEL can be transferred to the **Hardware** pin by setting the TERCNTL bit (bit 6) to "1" in the register address hex 0x82. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TXTSEL	V11	**I**	**Transmit Termination Select - Hardware Mode** When this pin is "Low" the transmit line termination is determined only by an external resistor. When "High", the transmit termination is realized only by the internal resistor. **TXTSEL** / **TX Termination**: **0** = **External**; **1** = **Internal** ***NOTES:*** 1. *This pin is internally pulled "Low" with a 50kΩ resistor.* 2. *In **Hardware mode** all channels share the same **TXTSEL** control function.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TERSEL1 **TERSEL0**	T11 R11	**I**	**Termination Impedance Select bit 1:** **Termination Impedance Select bit 0:** In the **Hardware mode** and in the **internal termination mode** (TXTSEL="1" and RXTSEL="1") TERSEL[1:0] control the transmit and receive termination impedance according to the following table. **TERSEL1** / **TERSEL0** / **Termination** 0 / 0 / 100Ω 0 / 1 / 110Ω 1 / 0 / 75Ω 1 / 1 / 120Ω In the **internal termination mode** the receiver termination of each receiver is realized completely by internal resistors or by the combination of internal and one fixed external resistor (see description of RXRES[1:0] pins). In the **internal termination mode** the transformer ratio of 1:2 or 1:2.45 and 1:1 is required for transmitter and receiver respectively with the transmitter output AC coupled to the transformer. ***NOTES:*** *1. This pin is internally pulled "Low" with a 50kΩ resistor.* *2. In **Hardware mode**, all channels share the same TERSEL control function.* *3. In the external termination mode a 1:2 or 1:2.45 transformer ratio must be used for the transmitter.*
TEST	U12	**I**	**Manufacturing Test:** ***NOTE:*** *For normal operation this pin must be tied to ground.*
$\overline{\text{ICT}}$	V12	**I**	**In-Circuit Testing (Active "Low"):** When this pin is tied "Low", all output pins are forced to a high impedance state for in-circuit testing. Pulling $\overline{\text{RESET}}$ and $\overline{\text{ICT}}$ pins "Low" simultaneously will put the chip in factory test mode. This condition should not be permitted during normal operation. ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor.*

POWER AND GROUND

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TGND_0	D3	****	**Transmitter Analog Ground for Channel _0**
TGND_1	F2		**Transmitter Analog Ground for Channel _1**
TGND_2	E15		**Transmitter Analog Ground for Channel _2**
TGND_3	C17		**Transmitter Analog Ground for Channel _3**
TGND_4	R3		**Transmitter Analog Ground for Channel _4**
TGND_5	P3		**Transmitter Analog Ground for Channel _5**
TGND_6	T16		**Transmitter Analog Ground for Channel _6**
TGND_7	R16		**Transmitter Analog Ground for Channel _7**

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TVDD_0	E4	****	**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _0**
TVDD_1	F4		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _1**
TVDD_2	F16		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _2**
TVDD_3	E17		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _3**
TVDD_4	R4		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _4**
TVDD_5	P1		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _5**
TVDD_6	N15		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _6**
TVDD_7	P15		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _7**
RVDD_0	C2	****	**Receiver Analog Positive Supply (3.3V± 5%) for Channel _0**
RVDD_1	E5		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _1**
RVDD_2	G16		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _2**
RVDD_3	D16		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _3**
RVDD_4	V2		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _4**
RVDD_5	N3		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _5**
RVDD_6	N17		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _6**
RVDD_7	U18		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _7**
RGND_0	D2	****	**Receiver Analog Ground for Channel_0**
RGND_1	G3		**Receiver Analog Ground for Channel_1**
RGND_2	G17		**Receiver Analog Ground for Channel_2**
RGND_3	D17		**Receiver Analog Ground for Channel_3**
RGND_4	T2		**Receiver Analog Ground for Channel_4**
RGND_5	M2		**Receiver Analog Ground for Channel_5**
RGND_6	M17		**Receiver Analog Ground for Channel_6**
RGND_7	R17		**Receiver Analog Ground for Channel_7**
AVDD Bias	K17	****	**Analog Positive Supply (3.3V± 5%)**
VDDPLL_1	J3		**Analog Positive Supply for Master Clock Synthesizer PLL (3.3V± 5%)**
VDDPLL_2	J2		**Analog Positive Supply for Master Clock Synthesizer PLL (3.3V± 5%)**
AGND Bias	J17	****	**Analog Ground**
GNDPLL_1	K3		**Analog Ground for Master Clock Synthesizer PLL**
GNDPLL_2	L4		**Analog Ground for Master Clock Synthesizer PLL**
DVDD_DRV	R9	****	**Digital Positive Supply (3.3V± 5%)**
DVDD_PRE	U10		**Digital Positive Supply (3.3V± 5%)**
DVDD µP	K18		**Digital Positive Supply (3.3V± 5%)**
DVDD_PRE	D10		**Digital Positive Supply (3.3V± 5%)**
DVDD_DRV	K15		**Digital Positive Supply (3.3V± 5%)**
DVDD	A9		**Digital Positive Supply (3.3V± 5%)**
DGND_PRE	R8	****	**Digital Ground**
DGND_DRV	T9		**Digital Ground**
DGND µP	H17		**Digital Ground**
DGND	B9		**Digital Ground**
DGND_DRV	D8		**Digital Ground**
DGND_PRE	C9		**Digital Ground**

PINS ONLY AVAILABLE IN BGA PACKAGE

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
DVDD_DRV **DVDD_DRV**	J4 D9	****	**Digital Positive Supply (3.3V± 5%)** **Digital Positive Supply (3.3V± 5%)**
DGND_DRV **DGND_DRV**	G15 K2	****	**Digital Ground** **Digital Ground**
RXON	K16	**I**	**Receiver On - Harware Mode** Writing a "1" to this pin in **Hardware** mode turns on the Receive Sections of all channels. Writing a "0" shuts off the Receiver Sections of all channels.
NC1 **NC2** **NC3** **NC4** **NC5** **NC6** **NC7** **NC8** **NC9** **NC10** **NC11** **NC12**	A1 V1 V18 A18 B1 E1 N1 R1 P18 N18 E18 B18	****	**No Connect Pins**

FUNCTIONAL DESCRIPTION

The XRT83L38 is a fully integrated long-haul and short-haul transceiver intended for T1, J1 or E1 systems. Simplified block diagrams of the chip are shown in Figure 1, **Host** mode and Figure 2, **Hardware** mode. The XRT83L38 can receive signals that have been attenuated from 0 to 36dB at 772kHz (0 to 6000 feet cable loss) for T1 and from 0 to 43dB at 1024kHz for E1 systems.

In T1 applications, the XRT83L38 can generate five transmit pulse shapes to meet the short-haul Digital Cross-connect (DSX-1) template requirement as well as four CSU Line Build-Out (LBO) filters of 0dB, -7.5dB, -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit output pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions (The arbitrary pulse generators are available in both T1 and E1). The operation and configuration of the XRT83L38 can be controlled through a parallel microprocessor **Host** interface or **Hardware** control.

MASTER CLOCK GENERATOR

Using a variety of external clock sources, the on-chip frequency synthesizer generates the T1 (1.544MHz) or E1 (2.048MHz) master clocks necessary for the transmit pulse shaping and receive clock recovery circuit.

There are two master clock inputs MCLKE1 and MCLKT1. In systems where both T1 and E1 master clocks are available these clocks can be connected to the respective pins. All channels of a given XRT83l38 must be operated at the same clock rate, either T1, E1 or J1 modes.

In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. T1 or E1 master clocks can be generated from 8kHz, 16kHz, 56kHz, 64kHz, 128kHz and 256kHz external clocks under the control of CLKSEL[2:0] inputs according to Table 1.

NOTE: *EQC[4:0] determine the T1/E1 operating mode. See* Table 5 *for details.*

FIGURE 4. TWO INPUT CLOCK SOURCE

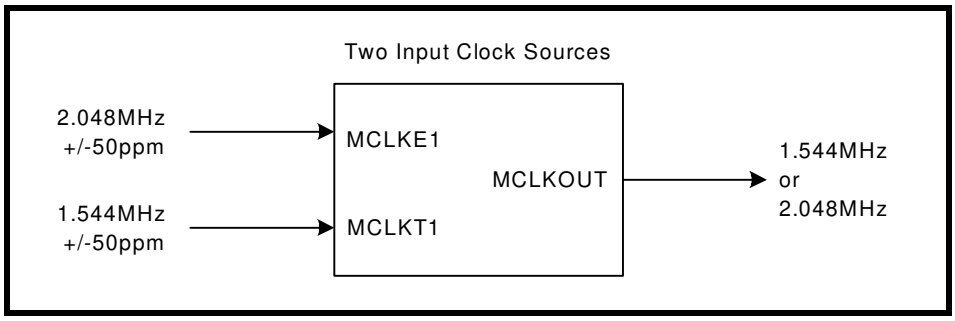


FIGURE 5. ONE INPUT CLOCK SOURCE