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GENERAL DESCRIPTION

The XRT83SL28 is a fully integrated 8-channel E1 short-haul LIU which optimizes system cost and performance by offering key design features. The XRT83SL28 operates from a single 3.3V power supply. The LIU features are programmed through a standard serial microprocessor interface or hardware control. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

Additional features include TAOS for transmit and receive, RLOS, LCV, AIS, DMO, and diagnostic loopback modes.

APPLICATIONS

- ISDN Primary Rate Interface
- CSU/DSU E1 Interface
- E1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- E1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA) Wireless Base Stations

FIGURE 1. HOST MODE BLOCK DIAGRAM OF THE XRT83SL28

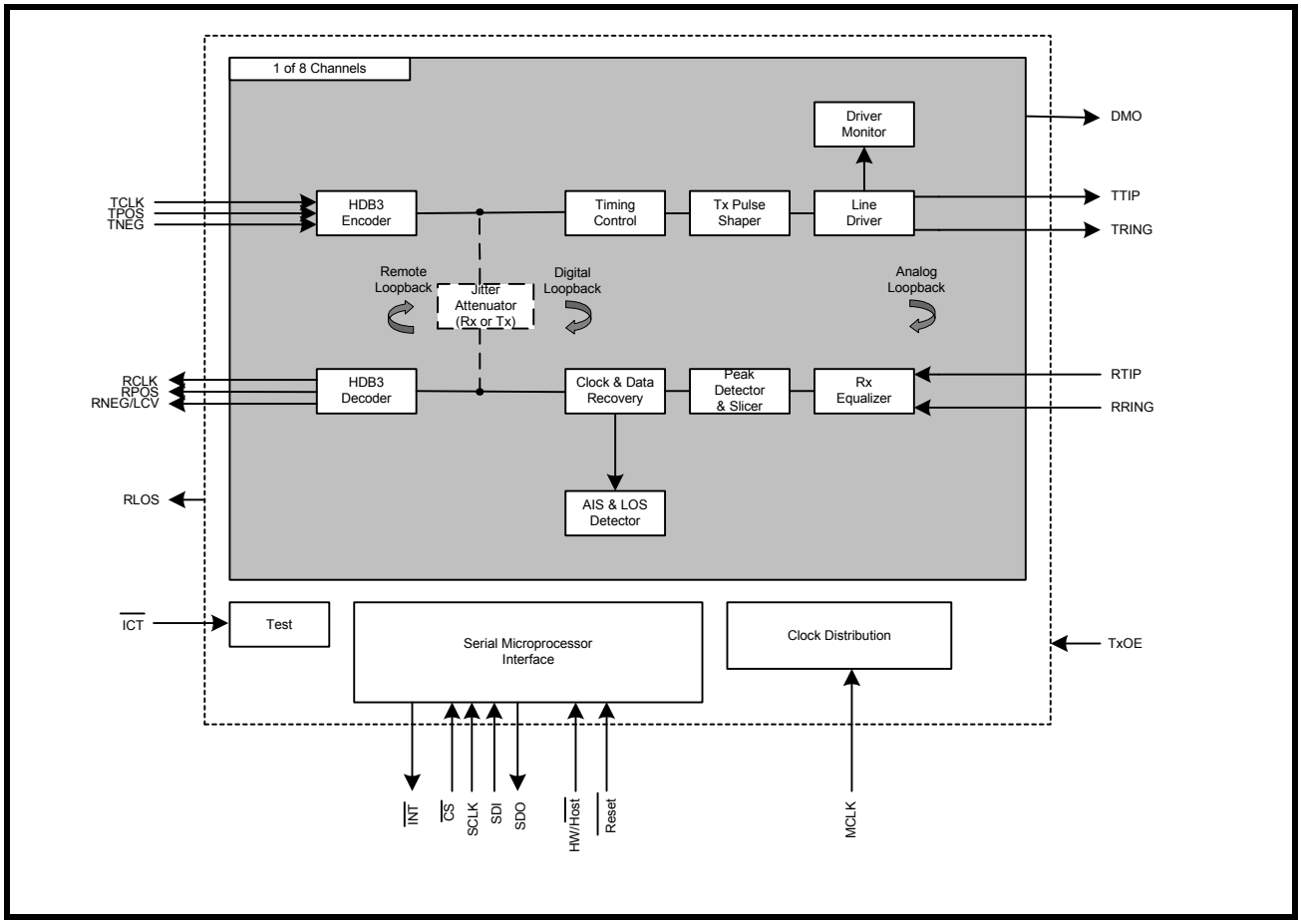
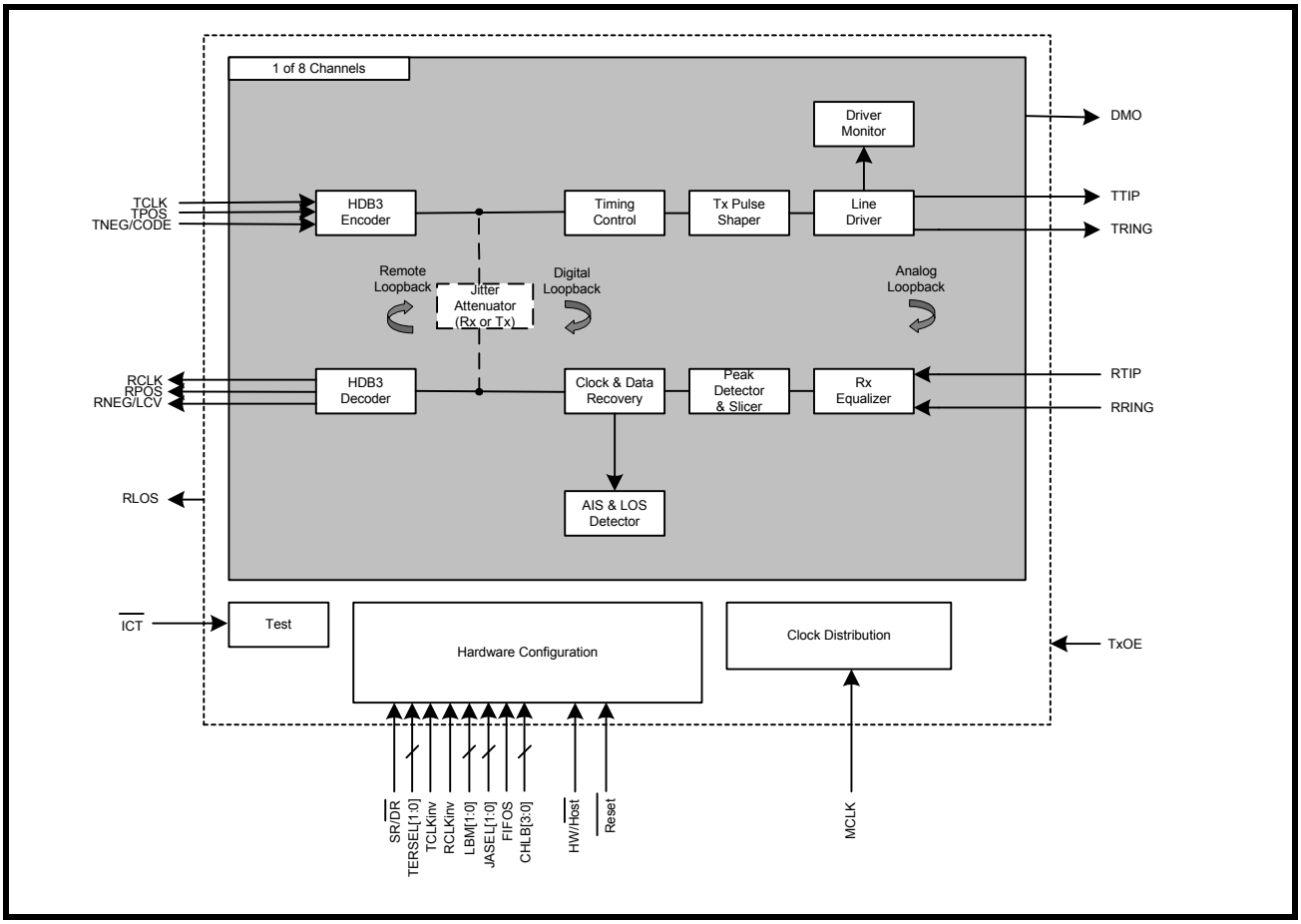


FIGURE 2. HARDWARE MODE BLOCK DIAGRAM OF THE XRT83SL28



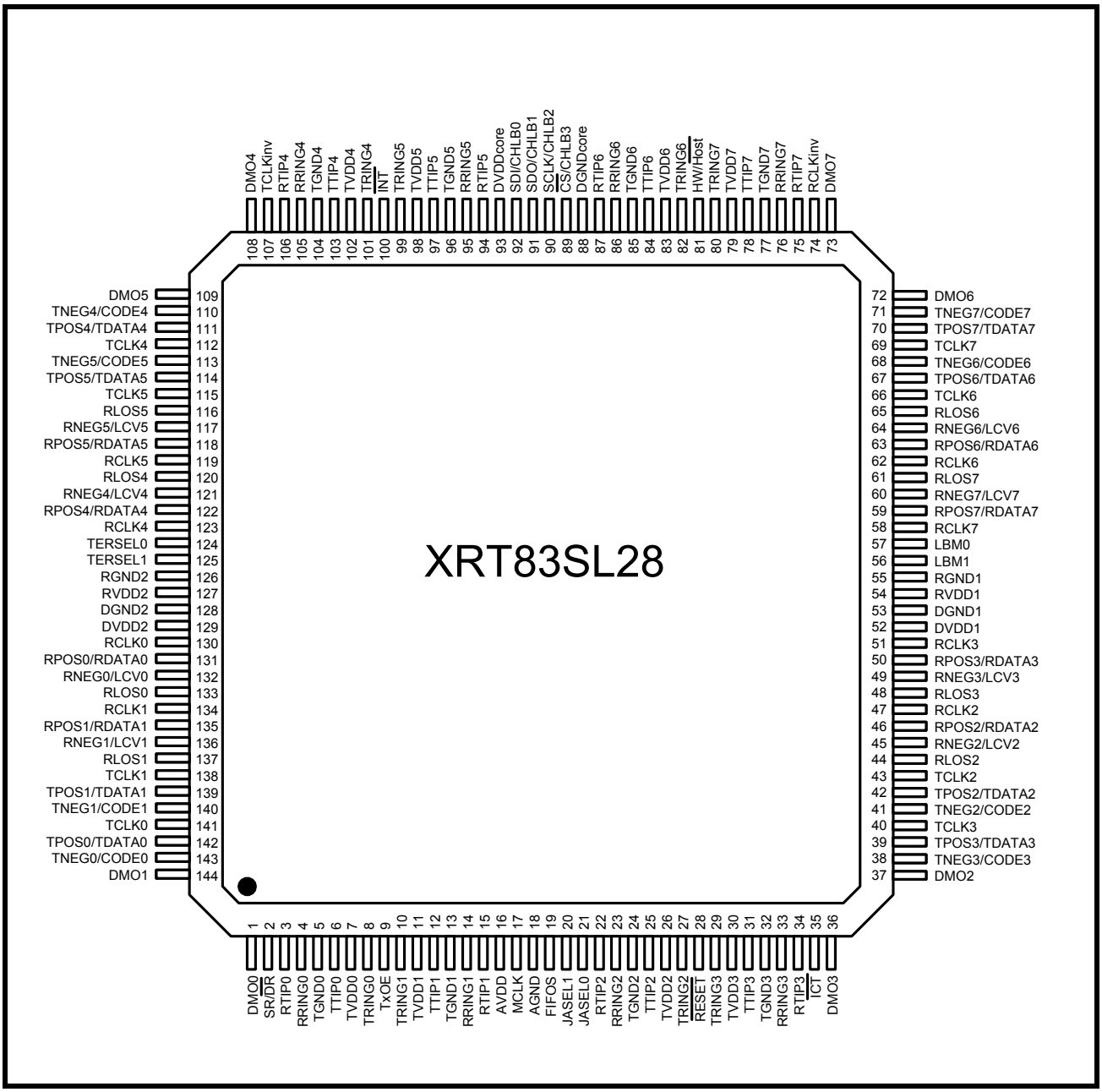
FEATURES

- Fully integrated 8-Channel short haul transceivers for E1 (2.048MHz) applications.
- Internal Impedance matching on both receive and transmit for 75Ω (E1) or 120Ω (E1) applications.
- Tri-State on a per channel basis for the transmit selection.
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis.
- Independent Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit paths
- Driver failure monitor output (DMO) alerts of possible system or external component problems.
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis.
- Support for automatic protection switching.
- 1:1 and 1+1 protection without relays.
- RLOS/AIS according to ITU-T G.775 or ETSI-300-233.
- On-Chip HDB3 encoder/decoder for each channel.
- On-Chip digital clock recovery circuit for high input jitter tolerance.
- Line code error and bipolar violation detection.
- Transmit all ones (TAOS) for the Transmit and Receive Outputs.
- Supports local analog, remote, and digital loopback modes.
- Supports gapped clocks for mapper/multiplexer applications.
- Low Power dissipation
- Single 3.3V supply operation (3V to 5V I/O tolerant).
- 144-Pin TQFP package
- -40°C to +85°C Temperature Range

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83SL28IV	144 Lead TQFP	-40°C to +85°C

FIGURE 3. PIN OUT OF THE XRT83SL28



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PIN DESCRIPTIONS

HOST MODE INTERFACE

SERIAL MICROPROCESSOR INTERFACE

NAME	PIN	TYPE	DESCRIPTION
$\overline{CS}$	89	I	**Chip Select Input** Active low signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial interface is disabled when the chip select signal returns "High".
SCLK	90	I	**Serial Clock Input** The serial clock input samples SDI on the rising edge and updates SDO on the falling edge. See the Serial Microprocessor section of this datasheet for more details.
SDI	92	I	**Serial Data Input** The serial data input pin is used to supply an address and data string to program the internal registers within the device. See the Serial Microprocessor section of this datasheet for more details.
SDO	91	O	**Serial Data Output** The serial data output pin is used to retrieve the internal contents of a selected register in readback mode. See the Microprocessor section of this datasheet for more details.
$\overline{Reset}$	28	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, all internal registers and state machines are set to their default state. ***NOTE:*** *This pin must be pulled "High" to VDD for normal operation.*
$\overline{INT}$	100	O	**Interrupt Output** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTE:*** *This pin is an open-drain output that requires an external 10KΩ pull-up resistor.*
HW/$\overline{Host}$	81	I	**Hardware / Host Mode Select Input** This pin is used to select the mode of operation. By default, the LIU is configured for Host mode. To select Hardware mode, this pin must be pulled "High". ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RLOS7 RLOS6 RLOS5 RLOS4 RLOS3 RLOS2 RLOS1 RLOS0	61 65 116 120 48 44 137 133	O	**Receive Loss of Signal** When a receive loss of signal occurs, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details.
RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	58 62 119 123 51 47 134 130	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent, RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKinv in the appropriate global register. ***NOTE:*** *RCLKinv is a global setting that applies to all 8 channels.*
RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	59 63 118 122 50 46 135 131	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.
RNEG/LCV7 RNEG/LCV6 RNEG/LCV5 RNEG/LCV4 RNEG/LCV3 RNEG/LCV2 RNEG/LCV1 RNEG/LCV0	60 64 117 121 49 45 136 132	O	**RNEG/LCV Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation indicator. If a line code violation or a bipolar violation occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	75 87 94 106 34 22 15 3	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	76 86 95 105 33 23 14 4	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TxOE	9	I	**Transmit Output Enable** Upon power up, the transmitters are tri-stated. Enabling the transmitters is selected through the serial microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxOE pin is pulled "Low", all 8 transmitters are tri-stated. ***NOTE:*** *TxOE is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.*
DMO7 DMO6 DMO5 DMO4 DMO3 DMO2 DMO1 DMO0	73 72 109 108 36 37 144 1	O	**Driver Monitor Output** When no transmit output pulse is detected for more than 128 TCLK cycles, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse.
TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	69 66 115 112 40 43 138 141	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLKinv in the appropriate global register. ***NOTE:*** *TCLKinv is a global setting that applies to all 8 channels.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	70 67 114 111 39 42 139 142	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input.
TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	71 68 113 110 38 41 140 143	I	**Transmit Negative Data Input** In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be tied to ground.
TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	78 84 97 103 31 25 12 6	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	80 82 99 101 29 27 10 8	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.

CONTROL FUNCTION

NAME	PIN	TYPE	DESCRIPTION
$\overline{\text{ICT}}$	35	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
MCLK	17	I	**Master Clock Input** This pin is used as the internal reference to the LIU. This clock must be 2.048MHz +/-50ppm.

POWER AND GROUND (HOST AND HARDWARE MODES)

NAME	PIN	TYPE	DESCRIPTION
TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0	79 83 98 102 30 26 11 7	PWR	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RVDD2 RVDD1	127 54	PWR	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
DVDD2 DVDD1 DVDDcore	129 52 93	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies except for TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.
AVDD	16	PWR	**Analog Power Supply (3.3V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	77 85 96 104 32 24 13 5	GND	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
RGND2 RGND1	126 55	GND	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND2 DGND1 DGNDcore	128 53 88	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.
AGND	18	GND	**Analog Ground** It's recommended that all ground pins of this device be tied together.

HARDWARE MODE INTERFACE

NAME	PIN	TYPE	DESCRIPTION
SR/$\overline{DR}$	2	I	**Single Rail / Dual Rail Select Input** This pin is used to select Single Rail or Dual Rail data formats. By default, Dual Rail is selected. To select Single Rail mode, this pin must be pulled "High". Once this pin is pulled "High", TNEGn/CODEn can be used to select between AMI and HDB3 Encoding/Decoding. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TERSEL1 TERSEL0	125 124	I	**Termination Impedance Select** TERSEL[1:0] are used to set the internal impedance of the LIU for the Receive and Transmit paths. "00" = 75Ω for Tx and "High-Z" for Rx "01" = 120Ω for Tx and "High-Z" for Rx "10" = 75Ω for Tx and Rx "11" = 120Ω for Tx and Rx
TCLKinv	107	I	**Transmit Clock Data** "Low" = TPOS/TNEG data is sampled on the falling edge of TCLK "High" = TPOS/TNEG data is sampled on the rising edge of TCLK ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
RCLKinv	74	I	**Receive Clock Data** "Low" = RPOS/RNEG data is updated on the rising edge of RCLK "High" = RPOS/RNEG data is updated on the falling edge of RCLK ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
LBM1 LBM0	56 57	I	**Loop Back Mode Select** LBM[1:0] are used to configure the LIU into diagnostic loopback modes. To select the channel number, see pins CHLB[3:0]. **LBM1 / LBM0 / Loopback Mode** 0 / 0 / No Loopback 0 / 1 / Analog Loopback 1 / 0 / Remote Loopback 1 / 1 / Digital Loopback ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
JASEL1 JASEL0	20 21	I	**Jitter Attenuator Select** JASEL[1:0] are used to configure the jitter attenuator into the Receive or Transmit path for all eight channels. **JASEL1 / JASEL0 / JA Select Mode** 0 / 0 / JA Disabled 0 / 1 / Transmit Path 1 / 0 / Receive Path 1 / 1 / JA Disabled ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

NAME	PIN	TYPE	DESCRIPTION
FIFOS	19	I	**FIFO Bit Depth Select Input** This pin is used to select the depth of the FIFO. By default, the FIFO is set to 32-Bit. To select a 64-Bit FIFO depth, this pin must be pulled "High". To meet TBR12/13 applications, the FIFO size must be set to 64-bit. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
HW/$\overline{\text{Host}}$	81	I	***Same as Host Mode.***
$\overline{\text{Reset}}$	28	I	***Same as Host Mode.***
CHLB3 CHLB2 CHLB1 CHLB0	89 90 91 92	I	**Channel Loop Back Select** CHLB[3:0] are used to select a particular channel or all eight channels simultaneously for Loop Back mode. See pins LBM[1:0] for selecting various types of Loop Back diagnostics. "0000" = Channel 0 "0001" = Channel 1 "0010" = Channel 2 "0011" = Channel 3 "0100" = Channel 4 "0101" = Channel 5 "0110" = Channel 6 "0111" = Channel 7 "1111" = All Eight Channels ***NOTE:*** *CHLB3 (Pin 89) is internally pulled "High" with a 50kΩ Resistor.*
RLOS7 RLOS6 RLOS5 RLOS4 RLOS3 RLOS2 RLOS1 RLOS0	61 65 116 120 48 44 137 133	O	***Same as Host Mode.***
RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	58 62 119 123 51 47 134 130	O	***Same as Host Mode.***
RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	59 63 118 122 50 46 135 131	O	***Same as Host Mode.***

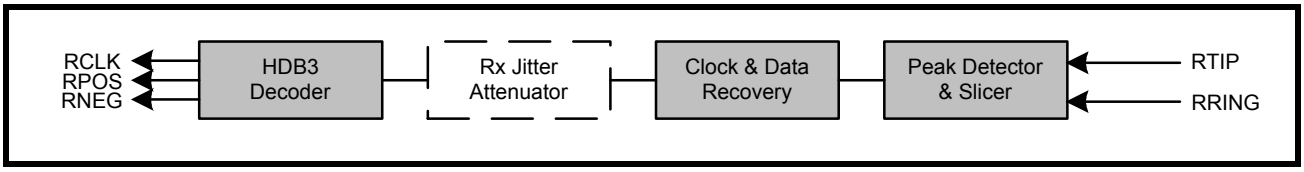
NAME	PIN	TYPE	DESCRIPTION
RNEG/LCV7 RNEG/LCV6 RNEG/LCV5 RNEG/LCV4 RNEG/LCV3 RNEG/LCV2 RNEG/LCV1 RNEG/LCV0	60 64 117 121 49 45 136 132	O	***Same as Host Mode.***
RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	75 87 94 106 34 22 15 3	I	***Same as Host Mode.***
RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	76 86 95 105 33 23 14 4	I	***Same as Host Mode.***
TXOE	9	I	**Transmit Output Enable (Global Pin for All 8 Channels)** Upon power up, the transmitters are tri-stated. Enabling the transmitters is controlled by pulling the TXOE hardware pin "High". If the TxOE pin is pulled "Low", all 8 transmitters are tri-stated. ***NOTE:*** *TxOE is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.*
DMO7 DMO6 DMO5 DMO4 DMO3 DMO2 DMO1 DMO0	73 72 109 108 36 37 144 1	O	***Same as Host Mode.***
TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	69 66 115 112 40 43 138 141	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is pulled "Low" for 16 MCLK cycles, the transmitter outputs at TTIP/TRING are tri-stated. If TCLK is pulled "High" for 16 MCLK cycles, the transmitter outputs at TTIP/TRING will send an All Ones pattern. TPOS/TNEG data can be sampled on either edge of TCLK selected by the TCLKinv pin. ***NOTE:*** *The TCLKinv pin is a global setting that applies to all 8 channels.*

NAME	PIN	TYPE	DESCRIPTION
TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	70 67 114 111 39 42 139 142	I	***Same as Host Mode.***
TNEG7/CODE7 TNEG6/CODE6 TNEG5/CODE5 TNEG4/CODE4 TNEG3/CODE3 TNEG2/CODE2 TNEG1/CODE1 TNEG0/CODE0	71 68 113 110 38 41 140 143	I	**Transmit Negative Data / CODE Select Input** TNEG has the same definition as Host Mode. However, in Hardware mode and Single Rail Data Format, this pin is used to select between AMI and HDB3 Encoder/Decoder. By default, HDB3 is selected. To select AMI, this pin must be pulled "High". ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	78 84 97 103 31 25 12 6	O	***Same as Host Mode.***
TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	80 82 99 101 29 27 10 8	O	***Same as Host Mode.***
$\overline{ICT}$	35	I	***Same as Host Mode.***
MCLK	17	I	***Same as Host Mode.***

1.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83SL28 LIU consists of 8 independent E1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in Figure 4.

FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH LINE TERMINATION (RTIP/RRING)



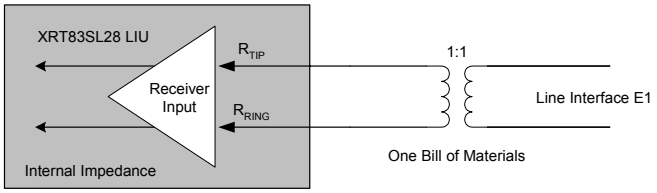
1.1 Internal Termination

The input stage of the receive path accepts standard E1 coaxial cable or E1 twisted pair inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance is selected by programming TERSEL[1:0] to match the line impedance. The XRT83SL28 has the ability to switch the internal termination to "High" impedance for redundancy applications. See Redundancy in the Applications Section of this datasheet. Selecting the internal impedance is shown in Table 1. A typical connection diagram is shown in Figure 5.

TABLE 1: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	75Ω for Tx and "High-Z" for Rx
1h (01)	120Ω for Tx and "High-Z" for Rx
2h (10)	75Ω for Tx and Rx
3h (11)	120Ω for Tx and Rx

FIGURE 5. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



1.2 Peak Detector/Data Slicer

In the receive path, the line signal is coupled into the RTIP and RRing pins via a 1:1 transformer and are converted into digital pulses by an adaptive data slicer. Clock and data signals are recovered from the output of the slicer with the help of a digital PLL that provides excellent jitter accommodation for high input jitter tolerance.

1.3 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. In the absence of an incoming signal, RCLK maintains its timing by using MCLK as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKinv to "1" in the appropriate global register. Figure 6 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 7 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 2.

FIGURE 6. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

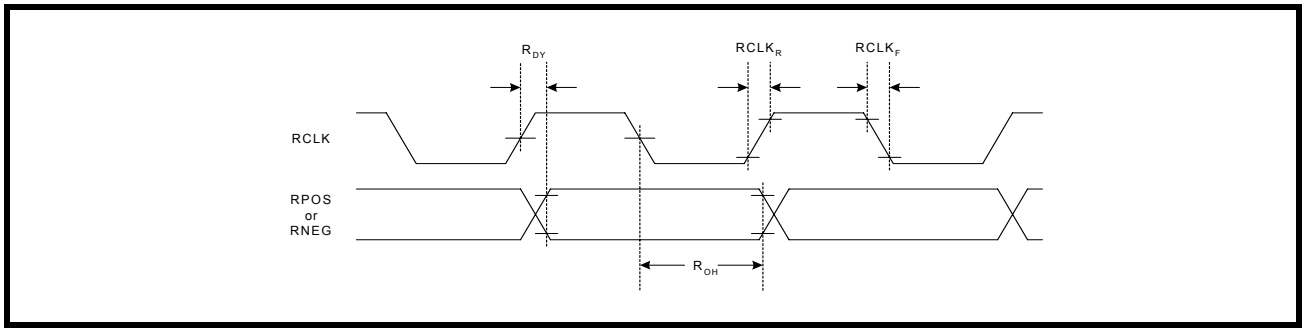


FIGURE 7. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

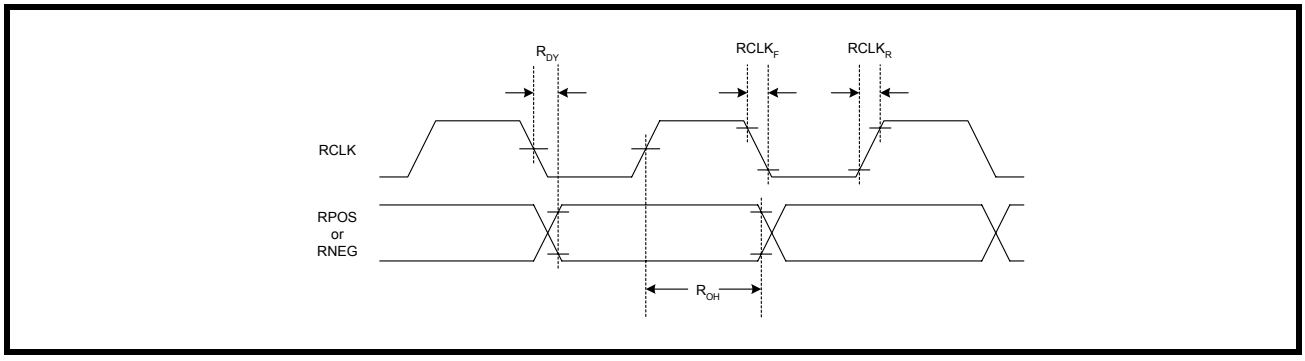


TABLE 2: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-	-	ns
Receive Data Hold Time	R_{HO}	150	-	-	ns
RCLK to Data Delay	R_{DY}	-	-	40	ns

TABLE 2: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

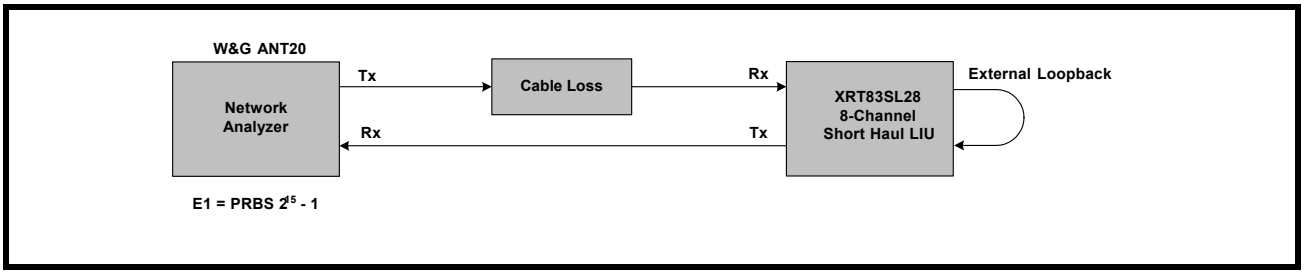
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

1.4 Receive Sensitivity

To meet short haul requirements, the XRT83SL28 can accept E1 signals that have been attenuated by 9dB of cable loss in E1 mode. The test configuration for measuring the receive sensitivity is shown in Figure 8.

FIGURE 8. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



1.5 General Alarm Detection and Interrupt Generation

The receive path detects RLOS and AIS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (if the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the $\overline{INT}$ pin will return "High". The status registers are Reset Upon Read (RUR).

NOTE: *The interrupt pin is an Open-Drain output that requires a 10kΩ pull-up resistor.*

1.5.1 RLOS (Receiver Loss of Signal)

The XRT83SL28 supports both G.775 or ETSI-300-233 RLOS detection scheme.

In G.775 mode, RLOS is declared when the received signal is less than 320mV for 32 consecutive pulse periods (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 550mV (typical).

In ETSI-300-233 mode the device declares RLOS when the input level drops below 320mV (typical) for more than 2048 pulse periods (1msec). The device exits RLOS when the input signal exceeds 550mV (typical) and has transitions for more than 32 pulse periods with 12.5% ones density with no more than 15 consecutive zero's in a 32 bit sliding window. ETSI-300-233 RLOSS detection method is only available in Host mode.

1.5.2 AIS (Alarm Indication Signal)

The XRT83SL28 adheres to ITU-T G.775 or ETSI-300-233 specifications for an all ones pattern detection by programming the appropriate channel register. The alarm indication signal is set to "1" if an all ones pattern is detected. In G.775 mode, AIS is defined as 2 or less zeros in 2 consecutive double frame (512-bit window) periods. AIS will clear when the incoming signal has 3 or more zeros in the same time period. In ETSI-300-233 mode, AIS is defined as less than 3 zeros in a 512-bit window. AIS detection scheme per ESTI-300-233 is only available in Host mode.

1.5.3 LCV (Line Code Violation Detection)

In HDB3 mode, the LCV pin will be set to "High" if the receiver detects excessive zero's, bipolar violations or HDB3 code violations. If the device is configured in AMI mode, any bipolar violations will cause the LCV pin to go "High".

1.6 Receive Jitter Attenuator

The jitter attenuator can be configured in the receive path to reduce phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. The bandwidth is set to 2Hz when the JA is configured in the Receive or Transmit path. The JA has a typical clock delay equal to ½ of the FIFO bit depth.

NOTE: *If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the JA can be configured in the transmit path to smooth out the gapped clock. See the Transmit Section of this datasheet.*

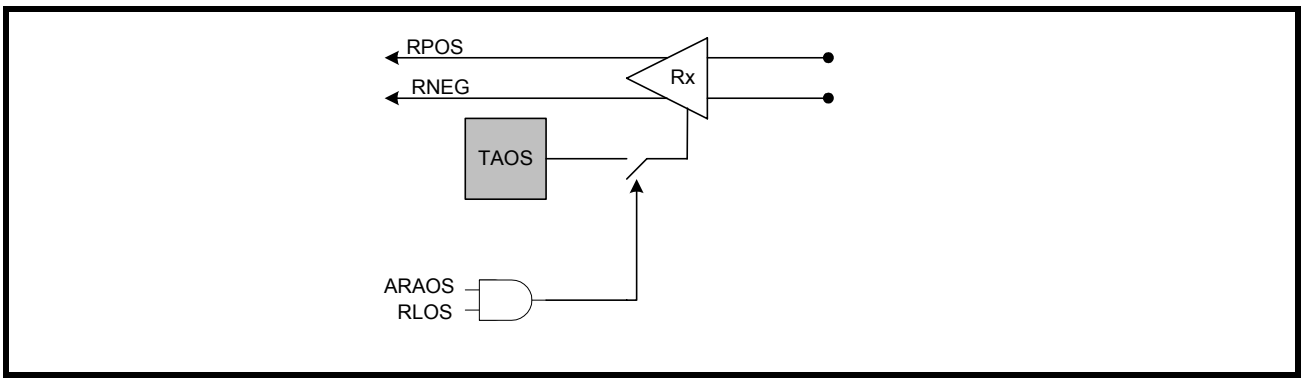
1.7 HDB3 Decoder

In single rail mode, RPOS is the output of decoded AMI or HDB3 signals and RNEG is the LCV output. HDB3 data is defined as any block of 4 successive zeros replaced with OOOV or BOOV, so that two successive V pulses are of opposite polarity to acheive zero DC offsey. If the HDB3 decoder is selected, the receive path removes the V and B pulses so that the original data is output to RPOS.

1.8 ARAOS (Automatic Receive All Ones)

The XRT83SL28 has the ability to send an All Ones signal to RPOS if ARAOS is enabled in the appropriate channel register. If ARAOS is enabled and an RLOS condition occurs, the Receiver outputs will generate a single rail All Ones pattern. When RLOS clears, the All Ones pattern ends and the Receive path returns to normal operation. For TAOS in the transmit direction, see the Transmit Section of this datasheet. A simplified block diagram of the ATAOS function is shown in Figure 9.

FIGURE 9. SIMPLIFIED BLOCK DIAGRAM OF THE ARAOS FUNCTION



1.9 RPOS/RNEG/RCLK

The digital output data can be programmed to either single rail or dual rail formats. Figure 10 is a timing diagram of a repeating "0011" pattern in single-rail mode. Figure 11 is a timing diagram of the same fixed pattern in dual rail mode.

FIGURE 10. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN

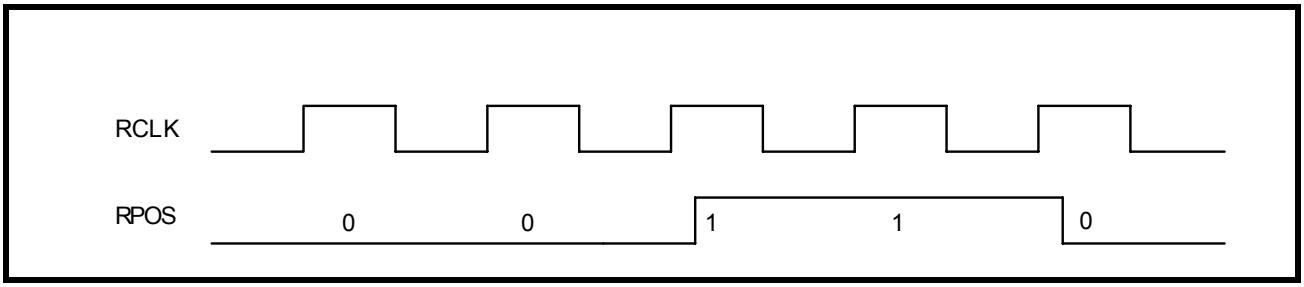
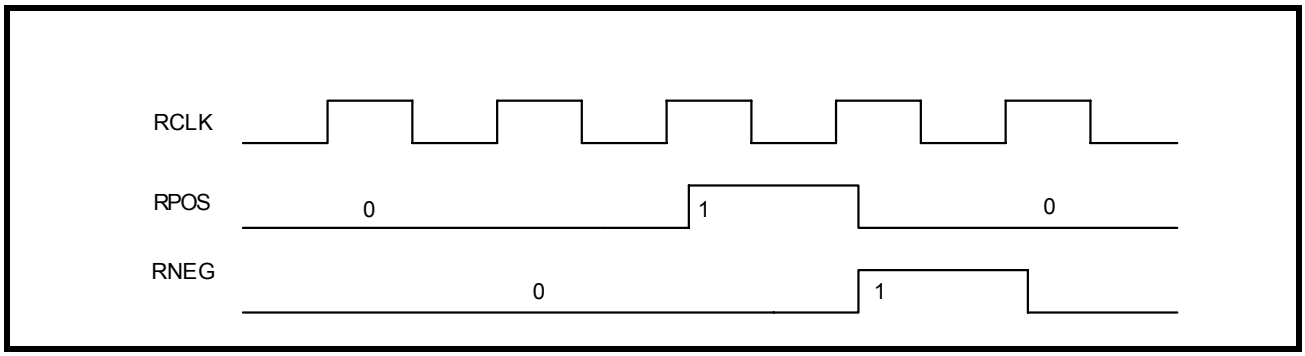


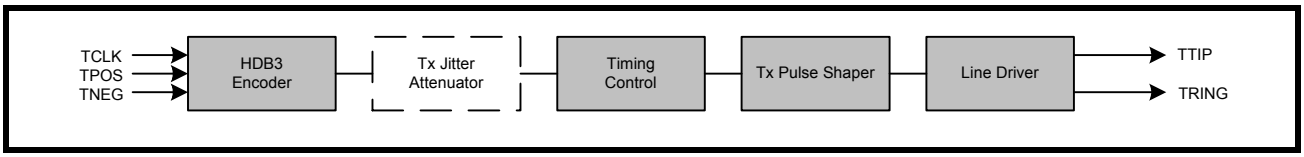
FIGURE 11. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN



2.0 TRANSMIT PATH LINE INTERFACE

The transmit path of the XRT83SL28 LIU consists of 8 independent E1 transmitters. The following section describes the complete transmit path from TCLK/TPOS/TNEG inputs to TTIP/TRING outputs. A simplified block diagram of the transmit path is shown in Figure 12.

FIGURE 12. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH



2.1 TCLK/TPOS/TNEG Digital Inputs

In dual rail mode, TPOS and TNEG are the digital inputs for the transmit path. In single rail mode, TNEG can be tied to ground unless Hardware mode is selected (see the Hardware Pin Description). The XRT83SL28 can be programmed to sample the inputs on either edge of TCLK. By default, data is sampled on the falling edge of TCLK. To sample data on the rising edge of TCLK, set TCLKinv to "1" in the appropriate global register. Figure 13 is a timing diagram of the transmit input data sampled on the falling edge of TCLK. Figure 14 is a timing diagram of the transmit input data sampled on the rising edge of TCLK. The timing specifications are shown in Table 3.

FIGURE 13. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK

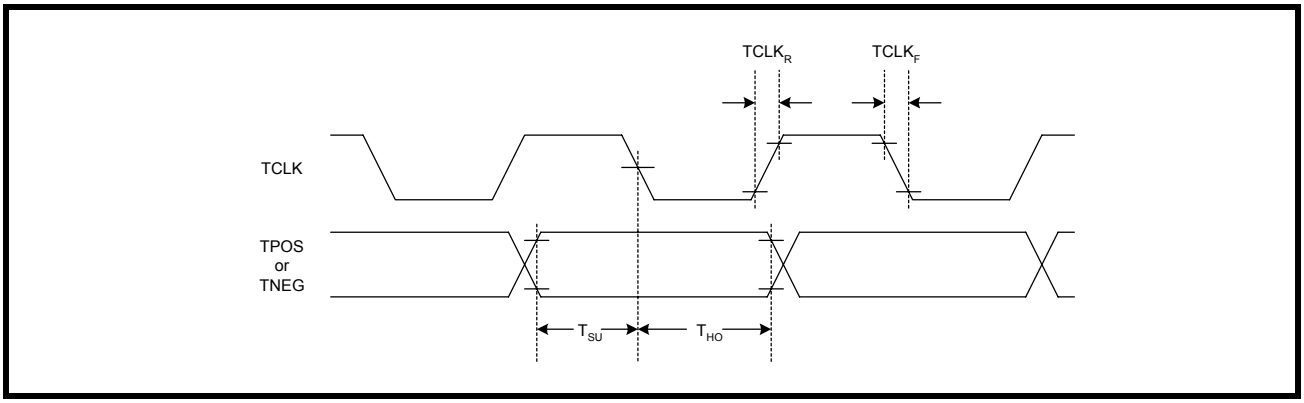


FIGURE 14. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK

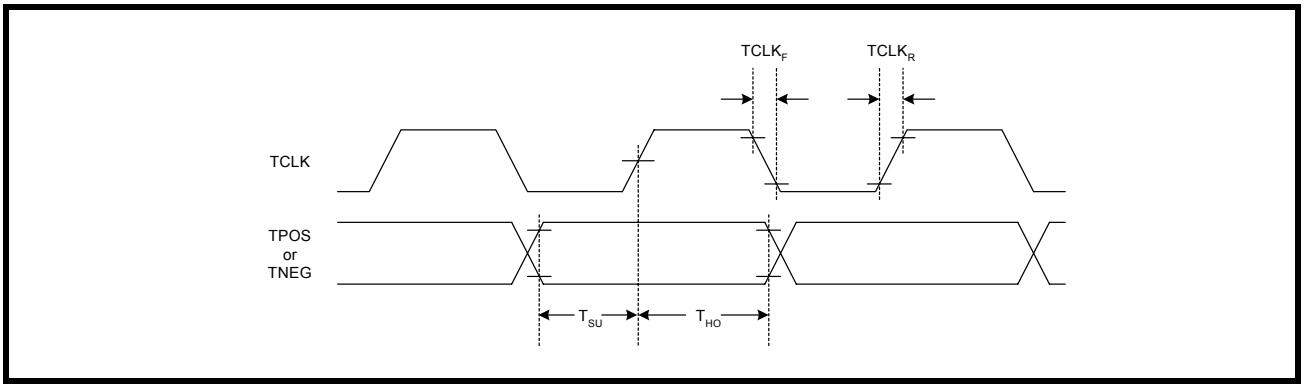


TABLE 3: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Duty Cycle	T_{CDU}	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	30	-	-	ns
TCLK Rise Time (10% to 90%)	$TCLK_R$	-	-	40	ns
TCLK Fall Time (90% to 10%)	$TCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

2.2 HDB3 Encoder

In single rail mode, the LIU can encode the TPOS input signal to AMI or HDB3 data. If HDB3 encoding is selected, any sequence with four or more consecutive zeros in the input will be replaced with 000V or B00V, where "B" indicates a pulse conforming to the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 encoding is shown in Table 4.

TABLE 4: EXAMPLES OF HDB3 ENCODING

	NUMBER OF PULSES BEFORE NEXT 4 ZEROS	
Input		0000
HDB3 (Case 1)	Odd	000V
HDB3 (Case 2)	Even	B00V

2.3 Transmit Jitter Attenuator

The XRT83SL28 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed to E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The JA can be configured in the transmit path with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady E1 output. The maximum gap width the JA in the Transmit path can tolerate is shown in Table 5.

TABLE 5: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

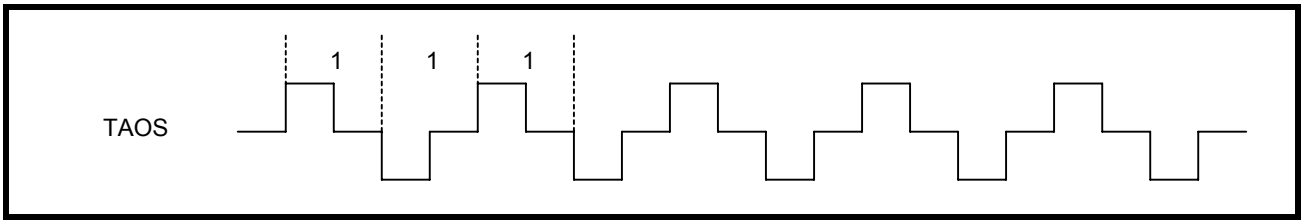
FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the JA should be configured in the receive path. See the Receive Section of this datasheet.*

2.4 TAOS (Transmit All Ones)

The XRT83SL28 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. If TAOS is enabled, the Transmitter outputs will generate an All Ones pattern regardless of the Transmit Input data. The Remote Loop Back mode has priority over TAOS. Figure 15 is a diagram showing the all ones signal at TTIP and TRING.

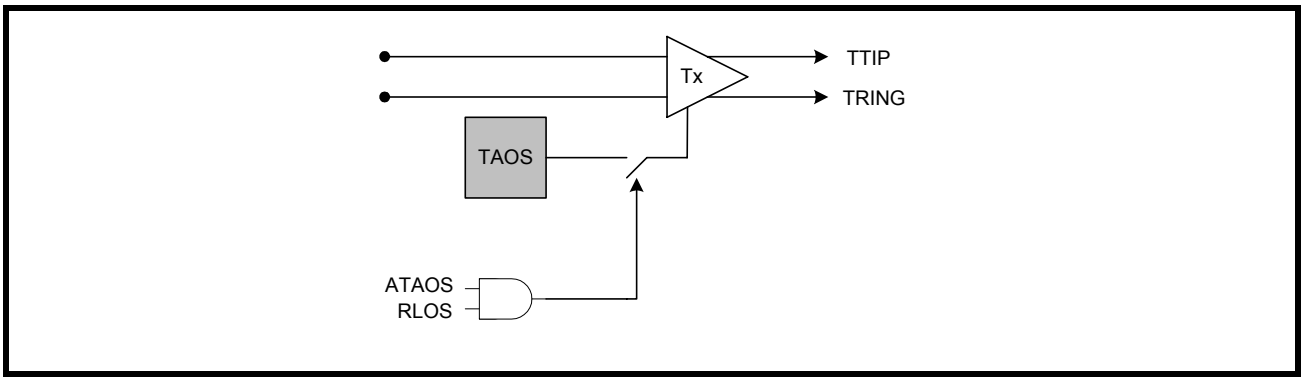
FIGURE 15. TAOS (TRANSMIT ALL ONES)ATAOS (AUTOMATIC TRANSMIT ALL ONES)



2.5 ATAOS (Automatic Transmit All Ones)

Unlike TAOS, ATAOS is used to generate an All Ones signal only when an RLOS condition occurs. If ATAOS is enabled, any channel that experiences an RLOS condition will automatically cause the transmitter on that channel to send an all ones pattern to the line. When RLOS clears, the All Ones pattern ends and the Transmit path returns to normal operation. For TAOS on the receive output pins, see ARAOS in the Receive Section of this datasheet. A simplified block diagram of the ATAOS function is shown in Figure 16.

FIGURE 16. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



2.6 Transmitter Power down in Hardware mode

In Hardware mode, if TCLK is pulled "Low" for 16 MCLK cycles the transmitter outputs at TTIP/TRING are tri-stated. If TCLK is pulled "High" for 16 MCLK cycles the transmitter will send an All Ones signal to the line, using MCLK as reference.

2.7 DMO (Driver Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 TCLK cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

2.8 Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard bipolar signals to the line for both E1 (75 Ohm) coaxial cable and E1 (120 Ohm) twisted pair. The XRT83L28 has built-in output impedance matching for both 75 Ohm and 120 Ohm operations. This eliminates the need to change any external components while switching from 75 Ohm to 120 Ohm operation. The transmitter interface only requires one 0.68μF DC blocking capacitor with a 1:2 transformer as shown in Figure 17.

FIGURE 17. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION