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GENERAL DESCRIPTION

The XRT83SL314 is a fully integrated 14-channel short-haul line interface unit (LIU) that operates from a single 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode independently on a per channel basis with minimum external components. The LIU features are programmed through a standard microprocessor interface. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

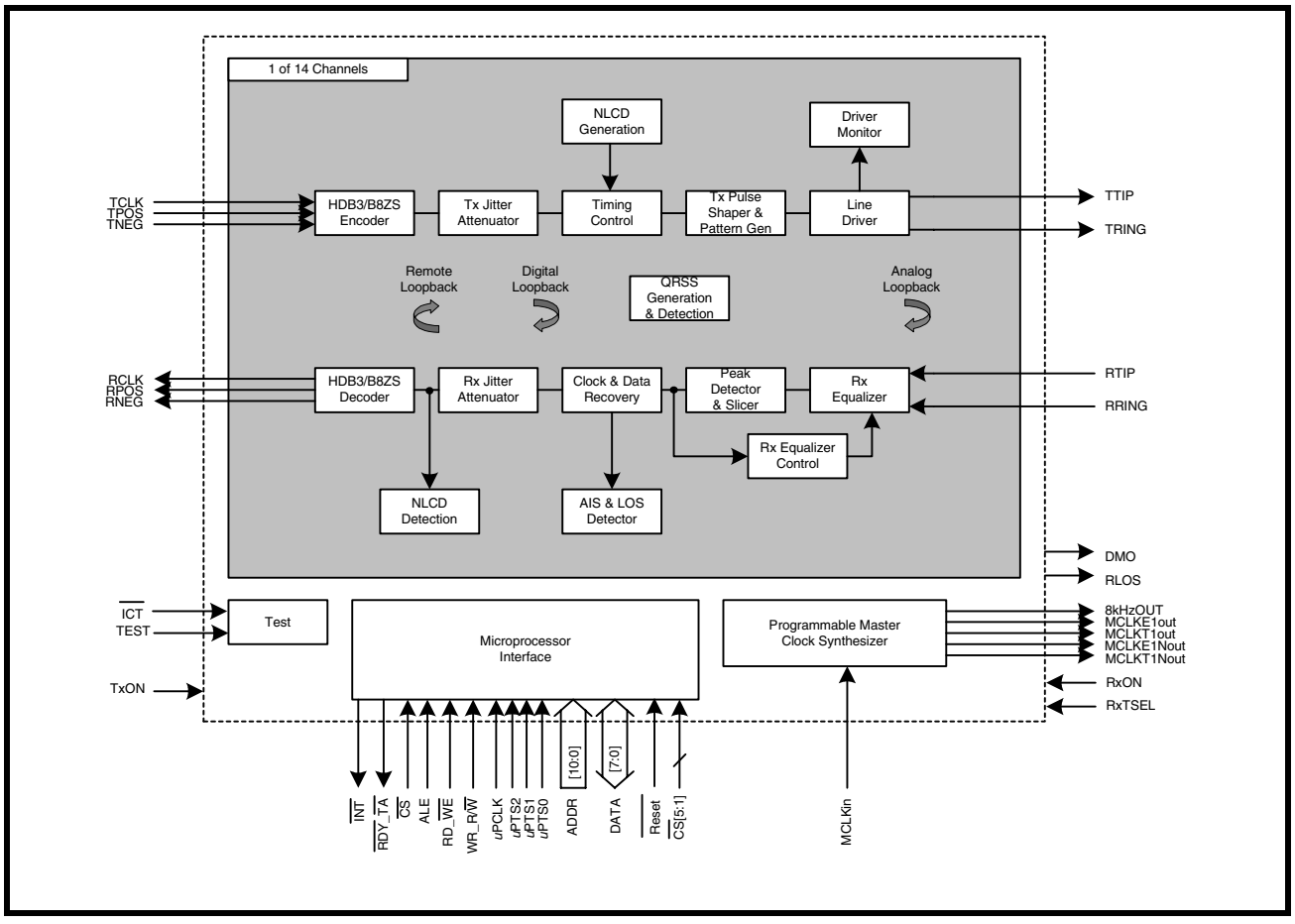
The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and has five output clock references that can be used for external timing (8kHz, 1.544Mhz, 2.048Mhz, nxT1/J1, nxE1).

Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/detection, Network Loop Code generation/detection, TAOS, DMO, and diagnostic loopback modes.

APPLICATIONS

- T1 Digital Cross Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA)
- Wireless Base Stations

FIGURE 1. BLOCK DIAGRAM OF THE XRT83SL314



FEATURES

- Fully integrated 14-Channel short haul transceivers for T1/J1 (1.544MHz) and E1 (2.048MHz) applications.
- T1/E1/J1 short haul and clock rate are per port selectable through software without changing components.
- Internal Impedance matching on both receive and transmit for 75Ω (E1), 100Ω (T1), 110Ω (J1), and 120Ω (E1) applications are per port selectable through software without changing components.
- Power down on a per channel basis with independent receive and transmit selection.
- Five pre-programmed transmit pulse settings for T1 short haul applications.
- Arbitrary Pulse Generators for both T1 and E1 modes.
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis.
- Independent Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive and transmit paths
- On-Chip frequency multiplier generates T1 or E1 master clocks from a variety of external clock sources (8, 16, 56, 64, 128, 256kHz and 1X, 2X, 4X, 8X T1 or E1)
- Driver failure monitor output (DMO) alerts of possible system or external component problems.
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis.
- Support for automatic protection switching.
- 1:1 and 1+1 protection without relays.
- Receive monitor mode handles 0 to 29dB resistive attenuation (flat loss) along with 0 to 6dB cable loss for both T1 and E1.
- Receiver line attenuation indication output in 1dB steps.
- Loss of signal (RLOS) according to ITU-T G.775/ ETS300233 (E1) and ANSI T1.403 (T1/J1).
- Programmable receive slicer threshold (45%, 50%, 55%, or 68%) for improved receiver interference immunity.
- Programmable data stream muting upon RLOS detection.
- On-Chip HDB3/B8ZS encoder/decoder with an internal 16-bit LCV counter for each channel.
- On-Chip digital clock recovery circuit for high input jitter tolerance.
- QRSS pattern generator and detection for testing and monitoring.
- Error and bipolar violation insertion and detection.
- Transmit all ones (TAOS) and in-band network loop up and loop down code generation.
- Automatic loop code detection for remote loopback activation.
- Supports local analog, remote, digital, and dual loopback modes.
- Low Power dissipation: 170mW per channel (50% density).
- 250mW per channel maximum power dissipation (100% density).
- Single 3.3V supply operation (3V to 5V I/O tolerant).
- 304-Pin TBGA package
- -40°C to +85°C Temperature Range
- Supports gapped clocks for mapper/multiplexer applications.

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83SL314IB	304 Lead TBGA	-40°C to +85°C

PIN OUT OF THE XRT83SL314

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A[10]	CSB	CSB4	WRB_RWB	TCLK_8	TPOS_10	TPOS_7	DGND_DRV	RVDD_7	RTIP_7	RRING_7	RGND_7	RGND_6	RRING_6	RTIP_6	RVDD_6	MCLKOUT_T1	MCLKIN	MCLKOUT_E1	MCLKE1xN	TCLK_5	ICTB	unnamed.12	A
unnamed.2	RESETB	CSB1	CSB5	TPOS_8	TNEG_9	TNEG_10	TCLK_7	VDDPLL_21	RCLK_7	TVDD_7	TRING_7	TRING_6	TVDD_6	RCLK_6	MCLKT1xN	TPOS_6	TCLK_3	TCLK_4	TPOS_4	INTB	DGND_DRV	unnamed.17	B
RGND_8	A[8]	DVDD_DRV	CSB3	ALE_AS	TNEG_8	TCLK_9	TNEG_7	VDDPLL_22	RNEG_7	TTIP_7	DGND_6_7	TTIP_6	RNEG_6	GNDPLL_22	GNDPLL_21	TNEG_6	TNEG_3	TNEG_4	TPOS_5	DVDD_PRE	TRING_5	RGND_5	C
RRING_8	TRING_8	unnamed.7	DVDD_PRE	CSB2	RDB_DSB	TPOS_9	TCLK_10	DGND_PRE	RPOS_7	TGND_7	DVDD_6_7	TGND_6	RPOS_6	DVDD_DRV	EIGHT_KHZ	TCLK_6	TPOS_3	TNEG_5	TEST	unnamed.13	TVDD_5	RRING_5	D
RTIP_8	RVDD_8	TVDD_8	A[9]																unnamed.11	TTIP_5	RVDD_5	RTIP_5	E
RVDD_9	RCLK_8	TTIP_8	TGND_8																TGND_5	RNEG_5	RCLK_5	RVDD_4	F
RTIP_9	RCLK_9	RNEG_8	RPOS_8																RPOS_5	RNEG_4	RCLK_4	RTIP_4	G
RRING_9	TVDD_9	RNEG_9	RPOS_9																RPOS_4	TTIP_4	TRING_4	RRING_4	H
RGND_9	TRING_9	TTIP_9	TGND_9																TGND_4	TVDD_4	DVDD_3_4_5	RGND_4	J
DVDD_8_9_10	unnamed.1	unnamed.3	unnamed.4																AVDD_BIAS	DVDD_DRV	unnamed.14	unnamed.16	K
DGND_8_9_10	unnamed.6	DGND_DRV	DGND_PRE																DGND_PRE	AGND_BIAS	DGND_3_4_5	unnamed.10	L
RGND_10	TRING_10	TTIP_10	TGND_10								Bottom View								TGND_3	TTIP_3	TRING_3	RGND_3	M
RRING_10	TVDD_10	RNEG_10	RPOS_10																RPOS_3	RNEG_3	TVDD_3	RRING_3	N
RTIP_10	RCLK_10	RNEG_11	RPOS_11																RPOS_2	RNEG_2	RCLK_3	RTIP_3	P
RVDD_10	RCLK_11	TTIP_11	TGND_11																TGND_2	TTIP_2	RCLK_2	RVDD_3	R
RTIP_11	RVDD_11	TVDD_11	TRING_11																DGND_1_2	TVDD_2	RVDD_2	RTIP_2	T
RRING_11	DVDD_DRV	DVDD_11_12	DGND_11_12																TVDD_1	DGND_DRV	TRING_2	RRING_2	U
RGND_11	TRING_12	TVDD_12	TGND_12																TGND_1	TRING_1	DVDD_1_2	RGND_2	V
RRING_12	RGND_12	TTIP_12	RPOS_12																RPOS_1	TTIP_1	RGND_1	RRING_1	W
RTIP_12	RCLK_12	RNEG_12	DVDD_PRE	A[1]	A[7]	TCLK_12	TCLK_13	RXTSEL	RPOS_13	TGND_13	DGND_13_0	TGND_0	RPOS_0	GNDPLL_12	TPOS_0	TNEG_1	D[3]	DVDD_PRE	DMO	RNEG_1	RVDD_1	RTIP_1	Y
RVDD_12	unnamed.5	UPTS0	A[2]	A[6]	TPOS_12	TNEG_11	DVDD_DRV	DVDD_UP	RNEG_13	TTIP_13	DVDD_13_0	TTIP_0	RNEG_0	RCLK_0	DGND_DRV	TNEG_2	TPOS_1	D[4]	D[7]	RDY_DTACKB	RCLK_1	unnamed.9	AA
DGND_DRV	UPTS1	A[3]	A[5]	RXOFF	TPOS_11	TPOS_13	VDDPLL_12	DGND_UP	RCLK_13	TVDD_13	TRING_13	TRING_0	TVDD_0	RVDD_0	DGND_PRE	TNEG_0	TPOS_2	D[0]	D[2]	D[6]	UPCLK	RLOS	AB
UPTS2	A[0]	A[4]	TXOFF	TNEG_12	TCLK_11	TNEG_13	VDDPLL_11	RVDD_13	RTIP_13	RRING_13	RGND_13	RGND_0	RRING_0	RTIP_0	GNDPLL_11	TCLK_0	TCLK_2	TCLK_1	D[1]	D[5]	DVDD_DRV	unnamed.0	AC

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PIN DESCRIPTIONS BY FUNCTION

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
$\overline{CS}$	A22	I	**Chip Select Input** Active low signal. This signal enables the microprocessor interface by pulling chip select "Low". The microprocessor interface is disabled when the chip select signal returns "High".
ALE_TS	C19	I	**Address Latch Enable Input (Transfer Start)** See the Microprocessor section of this datasheet for a description.
$\overline{WR}$_R/$\overline{W}$	A20	I	**Write Strobe Input (Read/Write)** See the Microprocessor section of this datasheet for a description.
$\overline{RD}$_$\overline{WE}$	D18	I	**Read Strobe Input (Write Enable)** See the Microprocessor section of this datasheet for a description.
$\overline{RDY}$_$\overline{TA}$	AA3	O	**Ready Output (Transfer Acknowledge)** See the Microprocessor section of this datasheet for a description.
$\overline{INT}$	B3	O	**Interrupt Output** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTE:*** *This pin is internally pulled "High" with a 50KΩ resistor.*
µPCLK	AB2	I	**Micro Processor Clock Input** In a synchronous microprocessor interface, µPCLK is used as the internal timing reference for programming the LIU.
ADDR10 ADDR9 ADDR8 ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0	A23 E20 C22 Y18 AA19 AB20 AC21 AB21 AA20 Y19 AC22	I	**Address Bus Input** ADDR[10:8] is used as a chip select decoder. The LIU has 5 chip select output pins for enabling up to 5 additional devices for accessing internal registers. The LIU has the option to select itself (master device), up to 5 additional devices, or all 6 devices simultaneously by setting the ADDR[10:8] pins specified below. ADDR[7:0] is a direct address bus for permitting access to the internal registers. **ADDR[10:8]** 000 = Master Device 001 = Chip Select Output 1 (Pin B21) 010 = Chip Select Output 2 (Pin D19) 011 = Chip Select Output 3 (Pin C20) 100 = Chip Select Output 4 (Pin A21) 101 = Chip Select Output 5 (Pin B20) 110 = Reserved 111 = All Chip Selects Active Including the Master Device

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0	AA4 AB3 AC3 AA5 Y6 AB4 AC4 AB5	I/O	**Bi-directional Data Bus** DATA[7:0] is a bi-directional data bus used for read and write operations.
µPTS2 µPTS1 µPTS0	AC23 AB22 AA21	I	**Microprocessor Type Select Input** µPTS[2:0] are used to select the microprocessor type interface. 000 = Intel 68HC11, 8051, 80C188 (Asynchronous) 001 = Motorola 68K (Asynchronous) 111 = Motorola MPC8260, MPC860 Power PC (Synchronous)
$\overline{\text{Reset}}$	B22	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
$\overline{\text{CS5}}$ $\overline{\text{CS4}}$ $\overline{\text{CS3}}$ $\overline{\text{CS2}}$ $\overline{\text{CS1}}$	B20 A21 C20 D19 B21	O	**Chip Select Output** The XRT83SL314 can be used to provide the necessary chip selects for up to 5 additional devices by using the 3 MSBs ADDR[10:8] from the 11-Bit address bus. The LIU allows up to 84-channel applications with only using one chip select. See the ADDR[10:0] definition in the pin description.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RxON	AB19	I	**Receive On/Off Input** Upon power up, the receivers are powered off. Turning the receivers On or Off can be selected through the microprocessor interface by programming the appropriate channel register if the hardware pin is pulled "High". If the hardware pin is pulled "Low", all channels are automatically turned off. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
RxTSEL	Y15	I	**Receive Termination Control** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register. Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RLOS	AB1	O	**Receive Loss of Signal (Global Pin for All 14-Channels)** When a receive loss of signal occurs for any one of the 14-channels according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel RLOS, see the register map.*
RCLK13 RCLK12 RCLK11 RCLK10 RCLK9 RCLK8 RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	AB14 Y22 R22 P22 G22 F22 B14 B9 F2 G2 P2 R2 AA2 AA9	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RxON is pulled "Low", RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKE in the appropriate global register. ***NOTE:*** *RCLKE is a global setting that applies to all 14 channels.*
RPOS13 RPOS12 RPOS11 RPOS10 RPOS9 RPOS8 RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	Y14 W20 P20 N20 H20 G20 D14 D10 G4 H4 N4 P4 W4 Y10	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RNEG13 RNEG12 RNEG11 RNEG10 RNEG9 RNEG8 RNEG7 RNEG6 RNEG5 RNEG4 RNEG3 RNEG2 RNEG1 RNEG0	AA14 Y21 P21 N21 H21 G21 C14 C10 F3 G3 N3 P3 Y3 AA10	O	**RNEG/LCV_OF Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation / Counter Overflow indicator. If LCV is selected by programming the appropriate global register and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. However, if OF is selected the LCV pin will pull "High" if the internal LCV counter is saturated. The LCV pin will remain "High" until the LCV counter is reset.
RTIP13 RTIP12 RTIP11 RTIP10 RTIP9 RTIP8 RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	AC14 Y23 T23 P23 G23 E23 A14 A9 E1 G1 P1 T1 Y1 AC9	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING13 RRING12 RRING11 RRING10 RRING9 RRING8 RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	AC13 W23 U23 N23 H23 D23 A13 A10 D1 H1 N1 U1 W1 AC10	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TxON	AC20	I	**Transmit On/Off Input** Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 14 transmitters are powered off. ***NOTE:*** *TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.*
DMO	Y4	O	**Digital Monitor Output (Global Pin for All 14-Channels)** When no transmit output pulse is detected for more than 128 TCLK cycles on one of the 14-channels, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel DMO, see the register map.*
TCLK13 TCLK12 TCLK11 TCLK10 TCLK9 TCLK8 TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	Y16 Y17 AC18 D16 C17 A19 B16 D7 A3 B5 B6 AC6 AC5 AC7	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING can be selected to send an all ones or an all zero signal by programming TCLKCNL in the appropriate global register. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLKE in the appropriate global register. ***NOTE:*** *TCLKE is a global setting that applies to all 14 channels.*
TPOS13 TPOS12 TPOS11 TPOS10 TPOS9 TPOS8 TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	AB17 AA18 AB18 A18 D17 B19 A17 B7 C4 B4 D6 AB6 AA6 Y8	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TNEG13 TNEG12 TNEG11 TNEG10 TNEG9 TNEG8 TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	AC17 AC19 AA17 B17 B18 C18 C16 C7 D5 C5 C6 AA7 Y7 AB7	I	**Transmit Negative Data Input** In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
TTIP13 TTIP12 TTIP11 TTIP10 TTIP9 TTIP8 TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	AA13 W21 R21 M21 J21 F21 C13 C11 E3 H3 M3 R3 W3 AA11	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING13 TRING12 TRING11 TRING10 TRING9 TRING8 TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	AB12 V22 T20 M22 J22 D22 B12 B11 C2 H2 M2 U2 V3 AB11	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.

CONTROL FUNCTION

NAME	PIN	TYPE	DESCRIPTION
TEST	D4	I	**Factory Test Mode** For normal operation, the TEST pin should be tied to ground. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{ICT}$	A2	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*

CLOCK SECTION

NAME	PIN	TYPE	DESCRIPTION
MCLKin	A6	I	**Master Clock Input** The master clock input can accept a wide range of inputs that can be used to generate T1 or E1 clock rates on a per channel basis. See the register map for details.
8kHzOUT	D8	O	**8kHz Output Clock**
MCLKE1out	A5	O	**2.048MHz Output Clock**
MCLKE1Nout	A4	O	**2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz Output Clock** See the register map for programming details.
MCLKT1out	A7	O	**1.544MHz Output Clock**
MCLKT1Nout	B8	O	**1.544MHz, 3.088MHz, 6.176MHz, or 12.352MHz Output Clock** See the register map for programming details.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
TVDD13 TVDD12 TVDD11 TVDD10 TVDD9 TVDD8 TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0	AB13 V21 T21 N22 H22 E21 B13 B10 D2 J3 N2 T3 U4 AB10	PWR	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RVDD13 RVDD12 RVDD11 RVDD10 RVDD9 RVDD8 RVDD7 RVDD6 RVDD5 RVDD4 RVDD3 RVDD2 RVDD1 RVDD0	AC15 AA23 T22 R23 F23 E22 A15 A8 E2 F1 R1 T2 Y2 AB9	PWR	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
DVDD DVDD DVDD DVDD DVDD DVDD	J2 V2 D12 AA12 U21 K23	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.
DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV DVDD_PRE DVDD_PRE DVDD_PRE DVDD_PRE DVDD_UP	C21 AC2 K3 D9 AA16 U22 C3 Y5 D20 Y20 AA15	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
AVDD_BIAS AVDD_PLL22 AVDD_PLL21 AVDD_PLL12 AVDD_PLL11	K4 C15 B15 AB16 AC16	PWR	**Analog Power Supply (3.3V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
TGND13 TGND12 TGND11 TGND10 TGND9 TGND8 TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	Y13 V20 R20 M20 J20 F20 D13 D11 F4 J4 M4 R4 V4 Y11	GND	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
RGND13 RGND12 RGND11 RGND10 RGND9 RGND8 RGND7 RGND6 RGND5 RGND4 RGND3 RGND2 RGND1 RGND0	AC12 W22 V23 M23 J23 C23 A12 A11 C1 J1 M1 V1 W2 AC11	GND	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND DGND DGND DGND DGND DGND	L2 T4 C12 Y12 U20 L23	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
DGND_DRV	B2	GND	**Digital Ground**
DGND_DRV	U3		It's recommended that all ground pins of this device be tied together.
DGND_DRV	A16		
DGND_DRV	AA8		
DGND_DRV	L21		
DGND_DRV	AB23		
DGND_PRE	L4		
DGND_PRE	D15		
DGND_PRE	AB8		
DGND_PRE	L20		
DGND_UP	AB15		
AGND_BIAS	L3	GND	**Analog Ground**
AGND_PLL22	C9		It's recommended that all ground pins of this device be tied together.
AGND_PLL21	C8		
AGND_PLL12	Y9		
AGND_PLL11	AC8		

NO CONNECTS

NAME	PIN	TYPE	DESCRIPTION
NC	A1	NC	**No Connect**
NC	B1		This pin can be left floating or tied to ground.
NC	K1		
NC	L1		
NC	AA1		
NC	AC1		
NC	K2		
NC	D3		
NC	E4		
NC	K20		
NC	D21		
NC	K21		
NC	K22		
NC	L22		
NC	AA22		
NC	B23		

1.0 CLOCK SYNTHESIZER

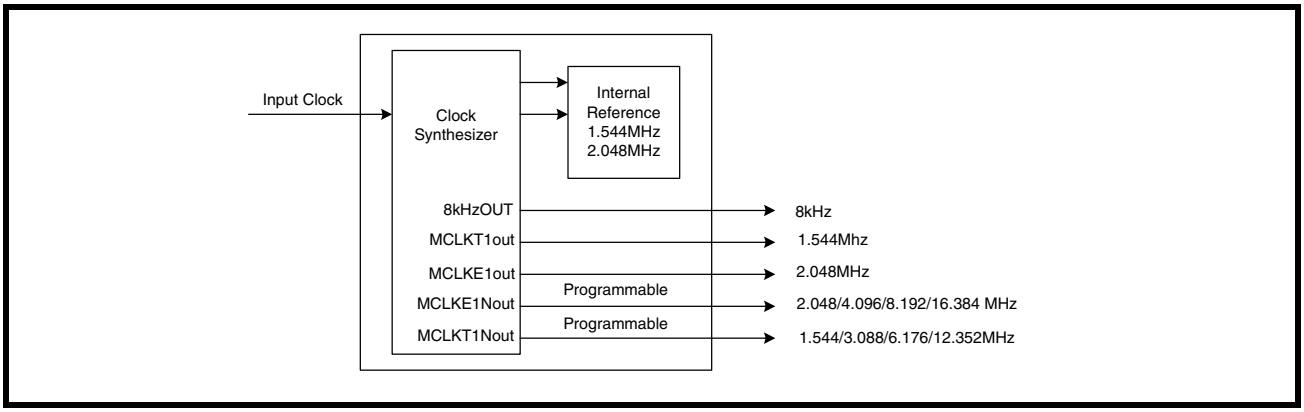
In system design, fewer clocks on the network card could reduce noise and interference. Common clock references such as 8kHz are readily available to network designers. Network cards that support both T1 and E1 modes must be able to produce 1.544MHz and 2.048MHz transmission data. The XRT83SL314 has a built in clock synthesizer that requires only one input clock reference by programming CLKSEL[3:0] in the appropriate global register. A list of the input clock options is shown in Table 1.

TABLE 1: INPUT CLOCK SOURCE SELECT

CLKSEL[3:0]	INPUT CLOCK REFERENCE
0h (0000)	2.048 MHz
1h (0001)	1.544MHz
2h (0010)	8 kHz
3h (0011)	16 kHz
4h (0100)	56 kHz
5h (0101)	64 kHz
6h (0110)	128 kHz
7h (0111)	256 kHz
8h (1000)	4.096 MHz
9h (1001)	3.088 MHz
Ah (1010)	8.192 MHz
Bh (1011)	6.176 MHz
Ch (1100)	16.384 MHz
Dh (1101)	12.352 MHz
Eh (1110)	2.048 MHz
Fh (1111)	1.544 MHz

The single input clock reference is used to generate multiple timing references. The first objective of the clock synthesizer is to generate 1.544MHz and 2.048MHz for each of the 14 channels. This allows each channel to operate in either T1 or E1 mode independent from the other channels. The state of the equalizer control bits in the appropriate channel registers determine whether the LIU operates in T1 or E1 mode. The second objective is to generate additional output clock references for system use. The available output clock references are shown in Figure 2.

FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE CLOCK SYNTHESIZER



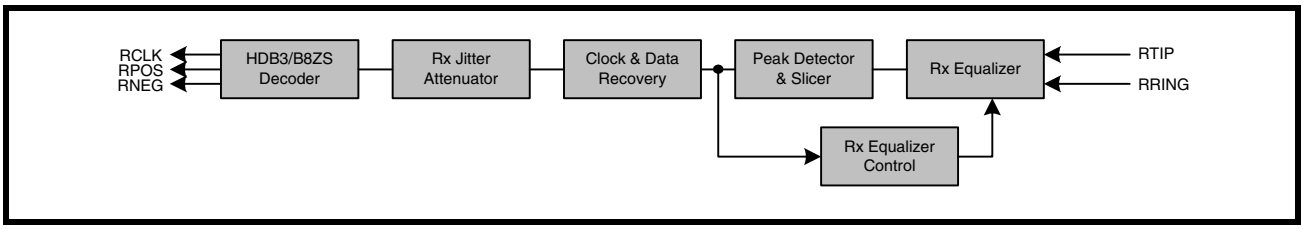
1.1 ALL T1/E1 Mode

To reduce system noise and power consumption, the XRT83SL314 offers an ALL T1/E1 mode. Since most line card designs are configured to operate in T1 or E1 only, the LIU can be selected to shut off the timing references for the mode not being used by programming the appropriate global register. By default the ALL T1/E1 mode is enabled (ALLT1/E1 bit = "0"). If the LIU is configured for T1, all E1 clock references and the 8kHz reference are shut off internally to the chip. This reduces the amount of internal clocks switching within the LIU, hence reducing noise and power consumption. In E1 mode, the T1 clock references are internally shut off, however the 8kHz reference is available. To disable this feature, the ALLT1/E1 bit must be set to a "1" in the appropriate global register.

2.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83SL314 LIU consists of 14 independent T1/E1/J1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in Figure 3.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



2.1 Line Termination (RTIP/RRING)

2.1.1 CASE 1: Internal Termination

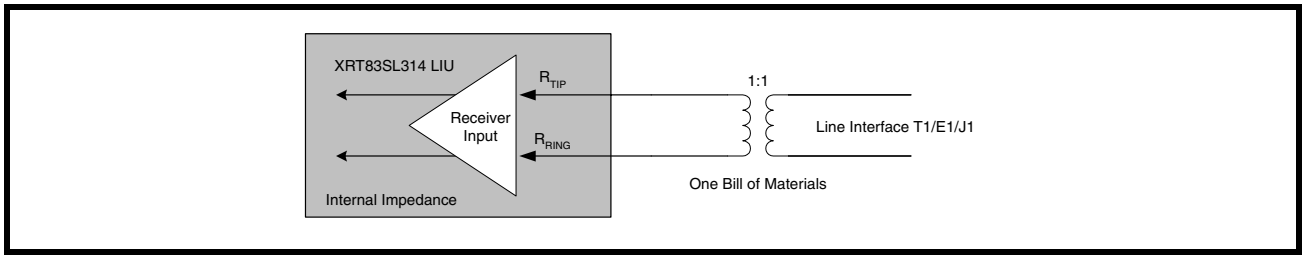
The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination (along with the transmit termination) impedance is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 2.

TABLE 2: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT83SL314 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See Figure 4 for a typical connection diagram using the internal termination.

FIGURE 4. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



2.1.2 CASE 2: Internal Termination With One External Fixed Resistor for All Modes

Along with the internal termination, a high precision external fixed resistor can be used to optimize the return loss. This external resistor can be used for all modes of operation ensuring one bill of materials. There are three resistor values that can be used by setting the RxRES[1:0] bits in the appropriate channel register. Selecting the value for the external fixed resistor is shown in Table 3.

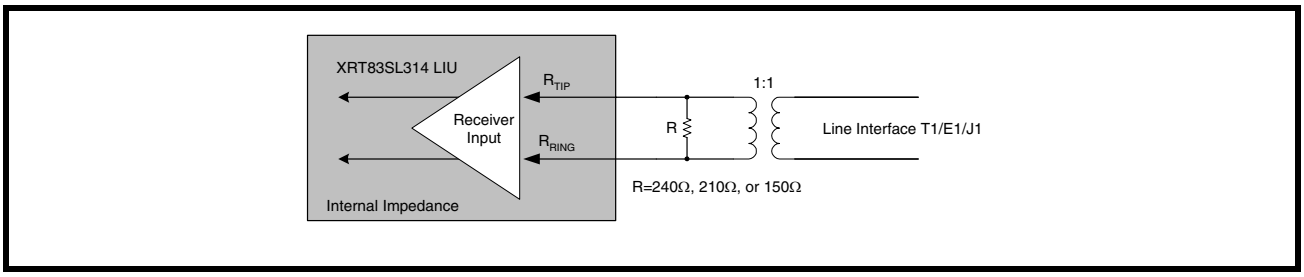
TABLE 3: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR

RxRES[1:0]	EXTERNAL FIXED RESISTOR
0h (00)	None
1h (01)	240Ω
2h (10)	210Ω
3h (11)	150Ω

By default, RxRES[1:0] is set to "None" for no external fixed resistor. If an external fixed resistor is used, the XRT83SL314 uses the parallel combination of the external fixed resistor and the internal termination as the input impedance. See Figure 5 for a typical connection diagram using the external fixed resistor.

NOTE: *Without the external resistor, the XRT83SL314 meets all return loss specifications. This mode was created to add flexibility for optimizing return loss by using a high precision external resistor.*

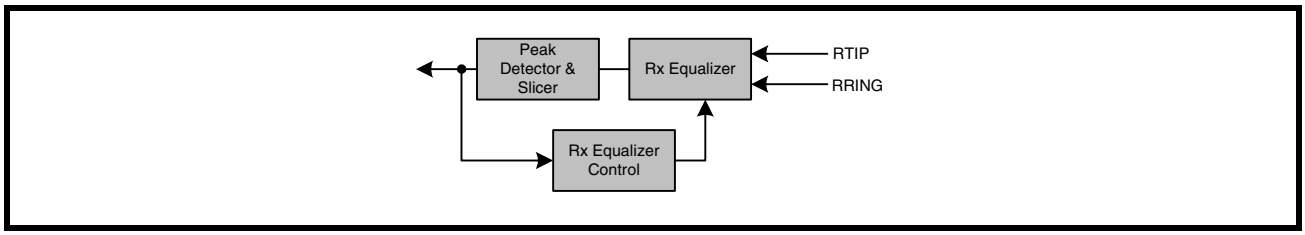
FIGURE 5. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR



2.2 Equalizer Control

The main objective of the equalizer is to amplify an input attenuated signal to a pre-determined amplitude that is acceptable to the peak detector circuit. Using feedback from the peak detector, the equalizer will gain the input up to the maximum value specified by the equalizer control bits, in the appropriate channel register, normalizing the signal. Once the signal has reached the pre-determined amplitude, the signal is then processed within the peak detector and slicer circuit. A simplified block diagram of the equalizer and peak detector is shown in Figure 6.

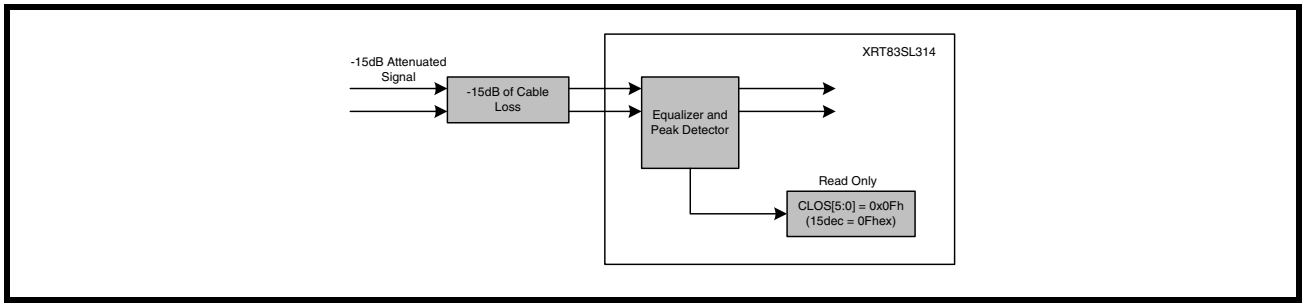
FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER AND PEAK DETECTOR



2.3 Cable Loss Indicator

The ability to monitor the cable loss attenuation of the receiver inputs is a valuable feature. The XRT83SL314 contains a per channel, read only register for cable loss indication. CLOS[5:0] is a 6-Bit binary word that reports the value of cable loss in 1dB steps. An example of -15dB cable loss attenuation is shown in Figure 7.

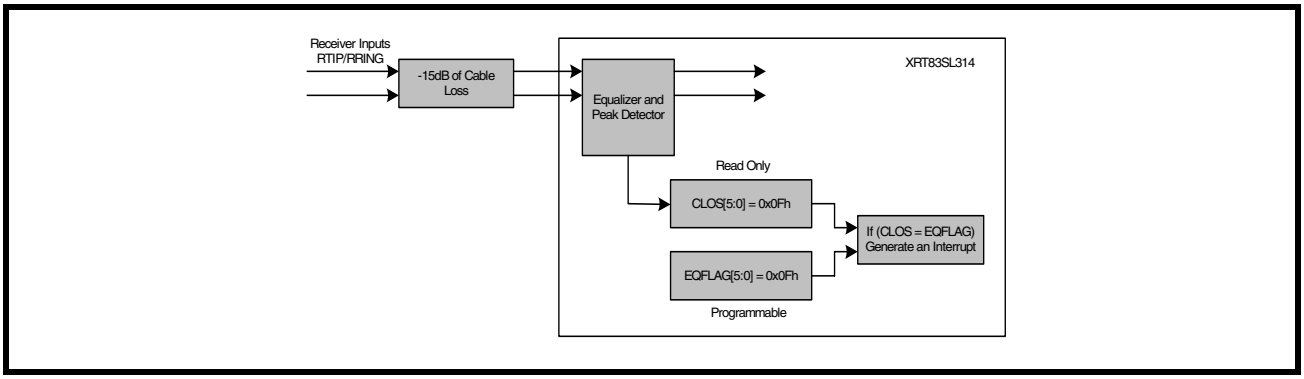
FIGURE 7. SIMPLIFIED BLOCK DIAGRAM OF THE CABLE LOSS INDICATOR



2.4 Equalizer Attenuation Flag

The ability to detect the amount of cable loss on the receiver inputs is enhanced by having the ability to generate an interrupt by programming a pre-determined value for cable loss into the EQFLAG[5:0] global register. This is particularly useful in applications where it is necessary for the LIU to generate an interrupt for a cable loss which is lower than the declaration of the RLOS feature (see the RLOS section in this datasheet). If the contents of the EQFLAG[5:0] register bits are equal to or less than the contents in the cable loss indicator bits CLOS[5:0] for a given channel, an interrupt will be generated (if enabled in the appropriate channel register and GIE is to "1"). Using the same example in Figure 7, a simplified block diagram of the equalizer flag is shown in Figure 8.

FIGURE 8. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER ATTENUATION FLAG



2.5 Peak Detector and Slicer

The peak detector provides feedback to the equalizer control circuit until the amplitude of the incoming signal is at an appropriate level. Once this level is obtained, the slicer identifies the incoming signal as a "1" and passes the raw data to the clock and data recovery circuit. The slicer threshold is selected by programming SL[1:0] in the appropriate global register. Selecting the slicer level is shown in Table 4.

TABLE 4: SELECTING THE SLICER LEVEL FOR THE PEAK DETECTOR

SL[1:0]	SLICER LEVEL
0h (00)	50%
1h (01)	45%
2h (10)	55%
3h (11)	68%

2.6 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1/J1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. Figure 9 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 10 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 5.

FIGURE 9. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

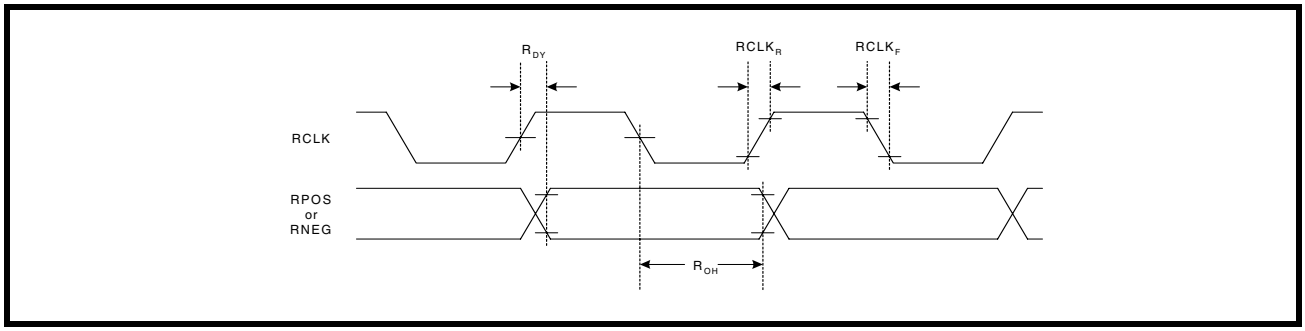


FIGURE 10. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

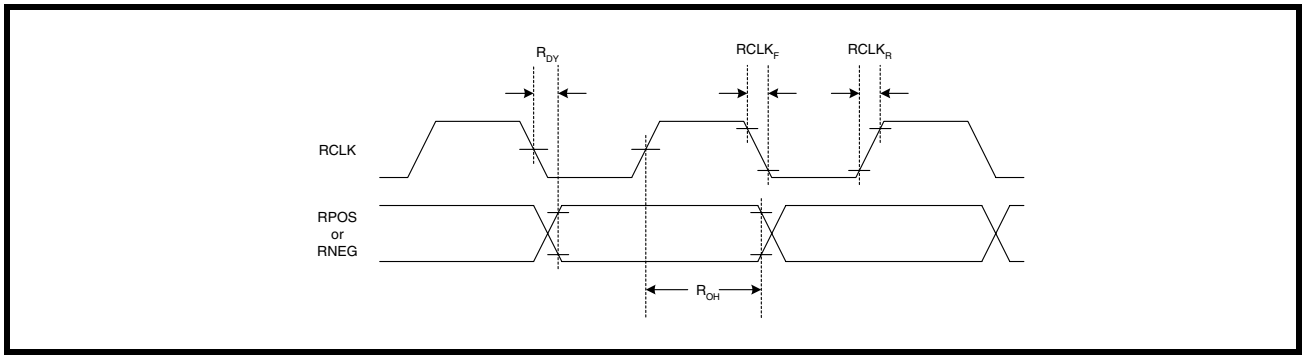


TABLE 5: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

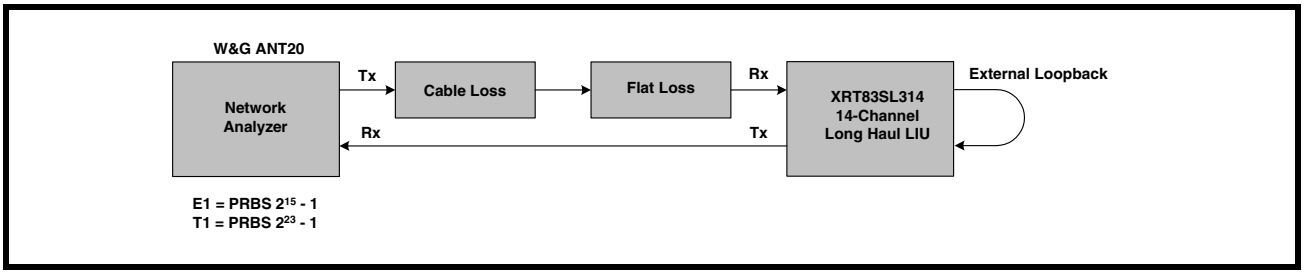
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-	-	ns
Receive Data Hold Time	R_{HO}	150	-	-	ns
RCLK to Data Delay	R_{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

2.6.1 Receive Sensitivity

To meet short haul requirements, the XRT83SL314 can accept T1/E1/J1 signals that have been attenuated by 12dB of flat loss in E1 mode or by 655 feet of cable loss along with 6dB of flat loss in T1 mode. However, the XRT83SL314 can tolerate cable loss and flat loss beyond the industry specifications. The receive sensitivity in the short haul mode is approximately 4,000 feet without experiencing bit errors, LOF, pattern synchronization, etc. Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in Figure 11.

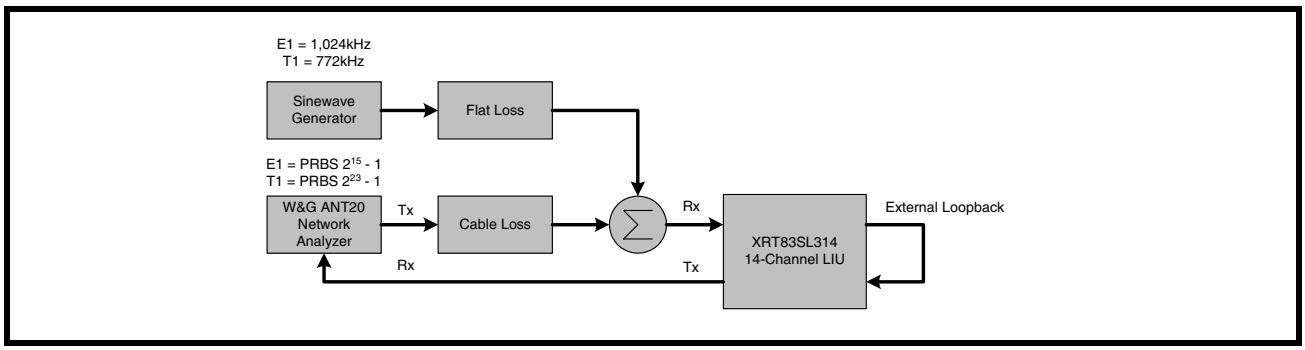
FIGURE 11. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



2.6.2 Interference Margin

The interference margin for the XRT83SL314 will be added when the first revision of silicon arrives. The test configuration for measuring the interference margin is shown in Figure 12.

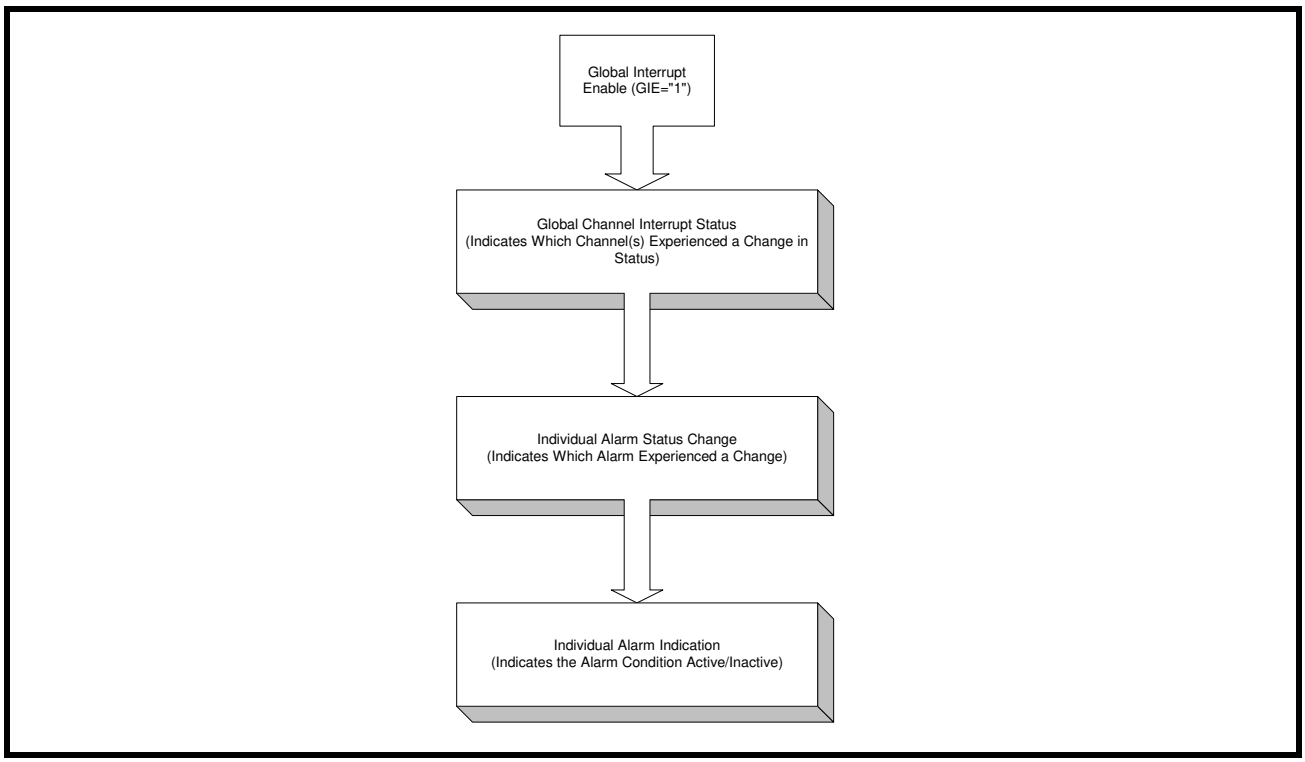
FIGURE 12. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN



2.6.3 General Alarm Detection and Interrupt Generation

The receive path detects EQFLAG, RLOS, AIS, QRPD, NCLD, and FLS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (it the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the INT pin will return "High". The status registers are Reset Upon Read (RUR). The interrupts are categorized in a hierarchical process block. Figure 13 is a simplified block diagram of the interrupt generation process.

FIGURE 13. INTERRUPT GENERATION PROCESS BLOCK



NOTE: *The interrupt pin is internally pulled "High" with a 50KΩ resistor.*

2.6.3.1 RLOS (Receiver Loss of Signal)