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QUAD T1/E1/J1 SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

MAY 2004 *REV. 1.0.0*

GENERAL DESCRIPTION

The XRT83SL34 is a fully integrated Quad (four channel) short-haul line interface unit for T1 (1.544Mbps) 100Ω, E1 (2.048Mbps) 75Ω or 120Ω, or J1 110Ω applications.

In T1 applications, the XRT83SL34 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83SL34 provides both a parallel **Host** microprocessor interface as well as a **Hardware** mode for programming and control.

Both the B8ZS and HDB3 encoding and decoding functions are selectable as well as AMI. An on-chip crystal-less jitter attenuator with a 32 or 64 bit FIFO can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83SL34 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. In the absence of the power supply, the transmit outputs and receive inputs are tri-stated allowing for redundancy applications The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

Features (See Page 2)

FIGURE 1. BLOCK DIAGRAM OF THE XRT83SL34 T1/E1/J1 LIU (HOST MODE)

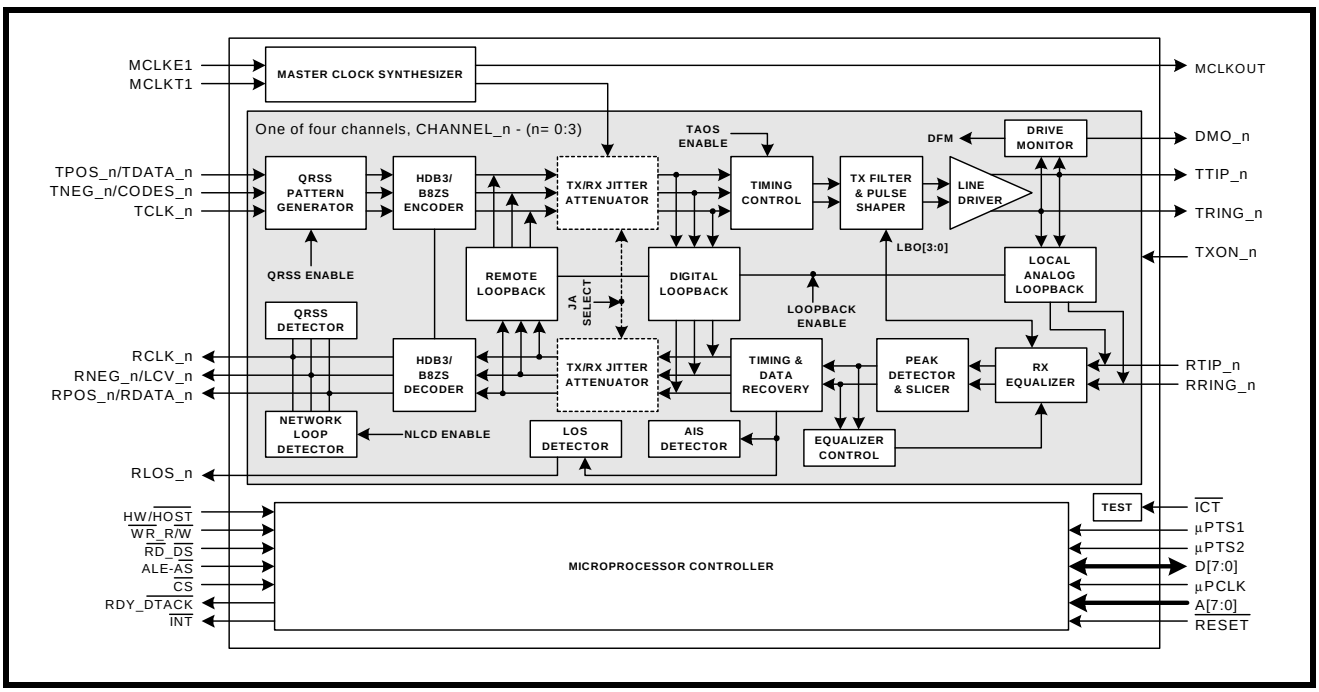
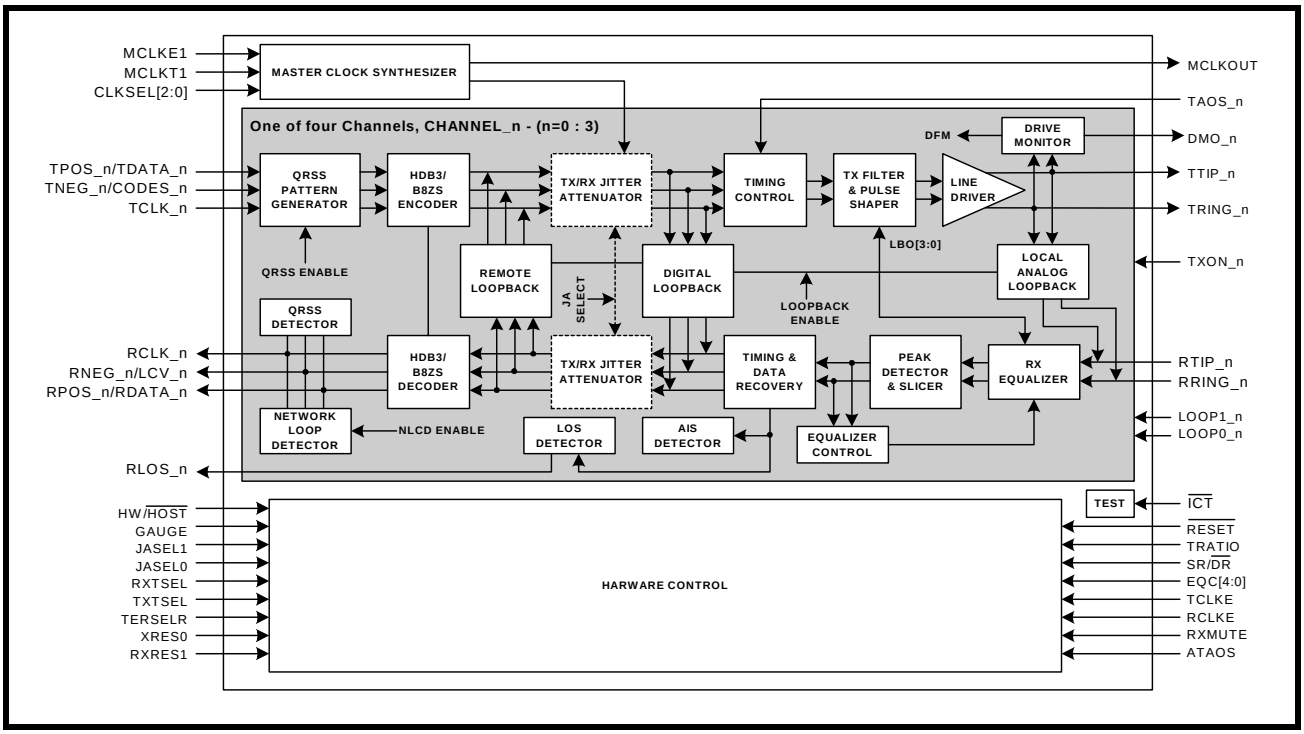


FIGURE 2. BLOCK DIAGRAM OF THE XRT83SL34 T1/E1/J1 LIU (HARDWARE MODE)



FEATURES

- Fully integrated eight channel short-haul transceivers for E1,T1 or J1 applications
- Programable Transmit Pulse Shaper for E1,T1 or J1 short-haul interfaces
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping for both T1 and E1 modes.
- Selectable receiver sensitivity from 0 to 36dB cable loss
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for E1 and 0 to 3dB of cable attenuation for T1 modes
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications
- Internal and/or external impedance matching for 75Ω, 100Ω, 110Ω and 120Ω
- Tri-State transmit output and receive input capability for redundancy applications
- Provides High Impedance for Tx and Rx during power off
- Transmit return loss meets or exceeds ETSI 300-166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- High receiver interference immunity
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder functions
- QRSS pattern generator and detection for testing and monitoring
- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Local Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul network access specifications in ITU G.703, G.775, G.736

and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411

- Supports both **Hardware** and **Host** (parallel Microprocessor) interface for programming
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Single 3.3V Supply Operation
- 128 pin TQFP package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83SL34IV	128 Lead TQFP (14 x 20 x 1.4mm)	-40°C to +85°C

FIGURE 3. PIN OUT OF THE XRT83SL34

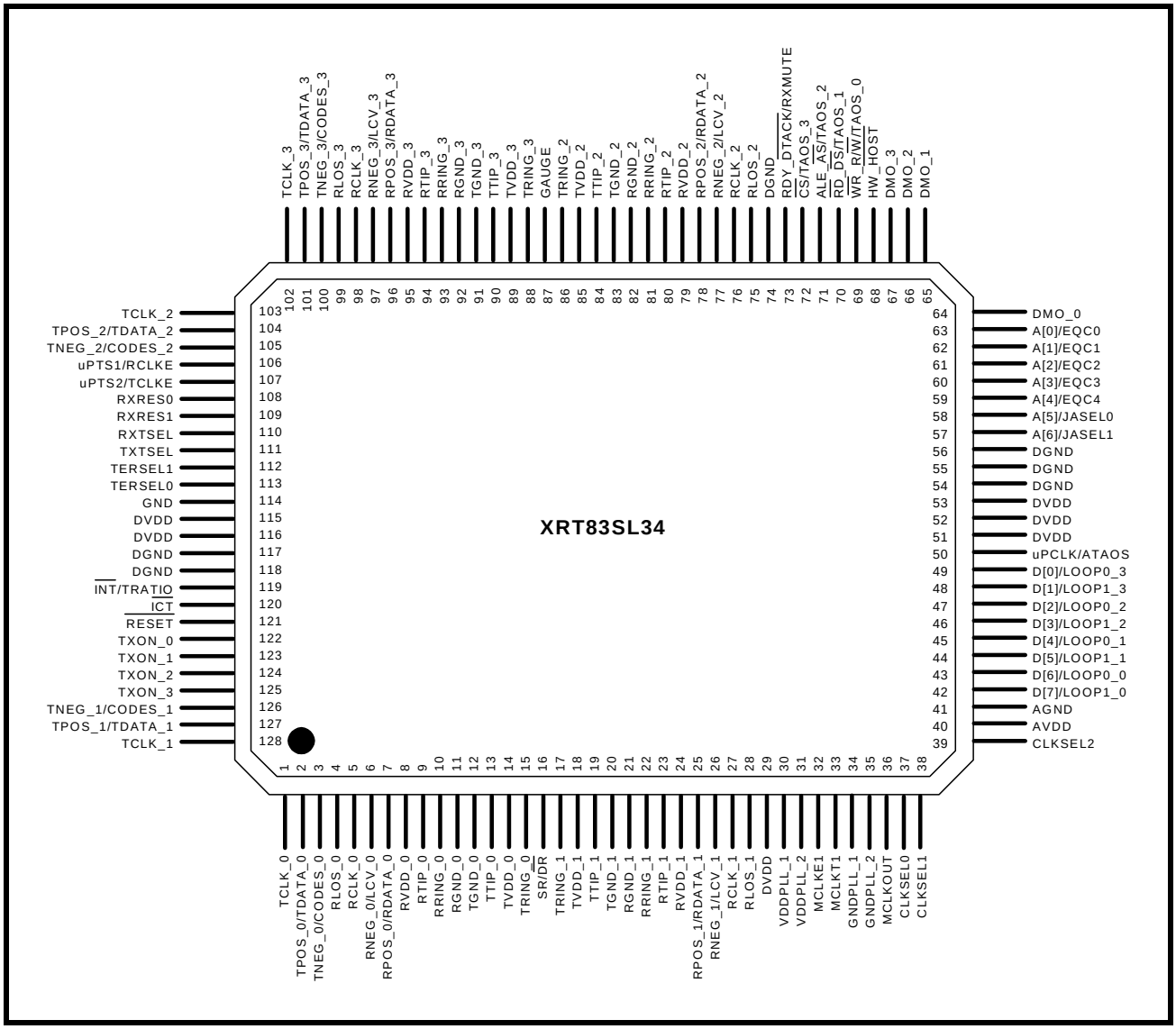


TABLE OF CONTENTS

PIN DESCRIPTION BY FUNCTION

RECEIVE SECTIONS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RLOS_0	4	**O**	**Receiver Loss of Signal for Channel _0** This output signal goes 'High' for at least one RCLK_0 cycle to indicate loss of signal at the receive 0 input. RLOS will remain "High" for the entire duration of the loss of signal detected by the receiver logic. See "Receiver Loss of Signal (RLOS)" on page 20.
RLOS_1	28		**Receiver Loss of Signal for Channel _1**
RLOS_2	75		**Receiver Loss of Signal for Channel _2**
RLOS_3	99		**Receiver Loss of Signal for Channel _3**
RCLK_0	5	**O**	**Receiver Clock Output for Channel _0**
RCLK_1	27		**Receiver Clock Output for Channel _1**
RCLK_2	76		**Receiver Clock Output for Channel _2**
RCLK_3	98		**Receiver Clock Output for Channel _3**
RNEG_0	6	**O**	**Receiver Negative Data Output for Channel _0 - Dual-Rail mode** This signal is the receiver negative-rail output data.
LCV_0			**Line Code Violation Output for Channel _0 - Single-Rail mode** This signal goes 'High' for one RCLK_0 cycle to indicate a code violation is detected in the received data of Channel _0. If AMI coding is selected, every bipolar violation received will cause this pin to go "High".
RNEG_1	26		**Receiver Negative Data Output for Channel _1**
LCV_1			**Line Code Violation Output for Channel _1**
RNEG_1	77		**Receiver Negative Data Output for Channel _2**
LCV_2			**Line Code Violation Output for Channel _2**
RNEG_1	97		**Receiver Negative Data Output for Channel _3**
LCV_3			**Line Code Violation Output for Channel _3**
RPOS_0	7	**O**	**Receiver Positive Data Output for Channel _0 - Dual-Rail mode** This signal is the receive positive-rail output data sent to the Framer.
RDATA_0			**Receiver NRZ Data Output for Channel _0 - Single-Rail mode** This signal is the receive output data.
RPOS_1	25		**Receiver Positive Data Output for Channel _1**
RDATA_1			**Receiver NRZ Data Output for Channel _1**
RPOS_2	78		**Receiver Positive Data Output for Channel _2**
RDATA_2			**Receiver NRZ Data Output for Channel _2**
RPOS_3	96		**Receiver Positive Data Output for Channel _3**
RDATA_3			**Receiver NRZ Data Output for Channel _3**
RTIP_0	9	**I**	**Receiver Differential Tip Positive Input for Channel _0** Positive differential receive input from the line.
RTIP_1	23		**Receiver Differential Tip Positive Input for Channel _1**
RTIP_2	80		**Receiver Differential Tip Positive Input for Channel _2**
RTIP_3	94		**Receiver Differential Tip Positive Input for Channel _3**

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RRING_0	10	**I**	**Receiver Differential Ring Negative Input for Channel _0** Negative differential receive input from the line.
RRING_1	22		**Receiver Differential Ring Negative Input for Channel _1**
RRING_2	81		**Receiver Differential Ring Negative Input for Channel _2**
RRING_3	93		**Receiver Differential Ring Negative Input for Channel _3**
RXMUTE	73	**I**	**Receive Muting - Hardware mode** Connecting this pin 'High' will mute (force to ground) the outputs RPOS_n/ RNEG_n when a LOS condition occurs, to prevent data chattering. This pin is internally pulled "low" consequently muting is normally disabled. ***NOTES:*** *1. Internally pulled "Low" with 50kΩ resistor.* *2. In Hardware mode, all receive channels share the same RXMUTE control function.*
RDY_$\overline{\text{DTACK}}$	73	**O**	**Ready Output (Data Transfer Acknowledge Output) - Host mode** See "Ready Output (Data Transfer Acknowledge Output) - Host Mode" on page 8.
			Receive External Resistor Control Pins - Hardware mode
RXRES0	108	**I**	**Receive External Resistor Control Pin 0**
RXRES1	109		**Receive External Resistor Control Pin 1** These pins are used to determine the value of the external Receive fixed resistor according to the following table: **RXRES1 / RXRES0 / Required Fixed External RX Resistor** **0 / 0 / No External Fixed Resistor** **0 / 1 / 240Ω** **1 / 0 / 210Ω** **1 / 1 / 150Ω** ***NOTE:*** *These pins are internally pulled "Low" with 50kΩ resistor.*
RCLKE	106	**I**	**Receive Clock Edge - Hardware Mode** Set this pin "High" to sample RPOS_N/RNEG_n on the falling edge of RCLK_n. With this pin tied "Low", output data are updated on the rising edge of RCLK_n.
µPTS1			**Microprocessor Type Select Input pin 1 - Host mode** This pin along with µPTS2 (pin 107) is used to select the microprocessor type. See "Microprocessor Type Select Input Pins - Host Mode:" on page 9. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*

TRANSMITTER SECTIONS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCLKE	107	**I**	**Transmit Clock Edge - Hardware Mode** With this pin set to a "High", transmit input data of all channels are sampled at the rising edge of TCLK_n. With this pin tied "Low", input data are sampled at the falling edge of TCLK_n.
µPTS2			**Microprocessor Type Select Input pin 2 - Host Mode** This pin along with µPTS1 (pin 106) selects the microprocessor type. See "Microprocessor Type Select Input Pins - Host Mode:" on page 9. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TTIP_0	13	**O**	**Transmitter Tip Output for Channel _0** Positive differential transmit output to the line.
TTIP_1	19		**Transmitter Tip Output for Channel _1**
TTIP_2	84		**Transmitter Tip Output for Channel _2**
TTIP_3	90		**Transmitter Tip Output for Channel _3**
TRING_0	15	**O**	**Transmitter Ring Output for Channel _0** Negative differential transmit output to the line.
TRING_1	17		**Transmitter Ring Output for Channel _1**
TRING_2	86		**Transmitter Ring Output for Channel _2**
TRING_3	88		**Transmitter Ring Output for Channel _3**
TPOS_0	2	**I**	**Transmitter Positive Data Input for Channel _0 - Dual-rail mode** This signal is the positive-rail input data for transmitter 0.
TDATA_0			**Transmitter 0 Data Input - Single-Rail mode** This pin is used as the NRZ input data for transmitter 0.
TPOS_1	127		**Transmitter Positive Data Input for Channel _1**
TDATA_1			**Transmitter 1 Data Input**
TPOS_2	104		**Transmitter Positive Data Input for Channel _2**
TDATA_2			**Transmitter 2 Data Input**
TPOS_3	101		**Transmitter Positive Data Input for Channel _3**
TDATA_3			**Transmitter 3 Data Input** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for each channels.*
TNEG_0	3	**I**	**Transmitter Negative NRZ Data Input for Channel _0** **Dual-Rail mode** This signal is the negative-rail input data for transmitter 0. **Single-Rail mode** This pin can be left unconnected.
CODES_0			**Coding Select for Channel _0 - Hardware mode and Single-Rail mode** Connecting this pin "Low" enables HDB3 in E1 or B8ZS in T1 encoding and decoding for Channel _0. Connecting this pin "High" selects AMI data format.
TNEG_1	126		**Transmitter Negative NRZ Data Input for Channel _1** **Coding Select for Channel _1**
CODES_1			**Transmitter Negative NRZ Data Input for Channel _2**
TNEG_2	105		**Coding Select for Channel _2**
CODES_2			**Transmitter Negative NRZ Data Input for Channel _3**
TNEG_3	100		**Coding Select for Channel _3**
CODES_3			***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for channel _n*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCLK_0	1	**I**	**Transmitter Clock Input for Channel _0 - Host mode and Hardware mode** **E1** rate at 2.048MHz ± 50ppm. **T1** rate at 1.544MHz ± 32ppm. During normal operation TCLK_0 is used for sampling input data at TPOS_0/ TDATA_0 and TNEG_0/CODES_0 while MCLK is used as the timing reference for the transmit pulse shaping circuit.
			Transmitter Clock Input for Channel _1
TCLK_1	128		**Transmitter Clock Input for Channel _2**
TCLK_2	103		**Transmitter Clock Input for Channel _3**
TCLK_3	102		***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
TAOS_0	69	**I**	**Transmit All Ones for Channel _0 - Hardware mode** Setting this pin "High" enables the transmission of an "All Ones" Pattern from Channel _0. A "Low" level stops the transmission of the "All Ones" Pattern.
TAOS_1	70		**Transmit All Ones for Channel _1**
TAOS_2	71		**Transmit All Ones for Channel _2**
TAOS_3	72		**Transmit All Ones for Channel _3**
$\overline{WR}$_R/$\overline{W}$	69		**Host mode:** these pins act as various microprocessor functions. See "Microprocessor Interface" on page 8.
RD_$\overline{DS}$	70		***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
ALE_$\overline{AS}$	71		
$\overline{CS}$	72		
TXON_0	122	**I**	**Transmitter Turn On for Channel _0** **Hardware mode** Setting this pin "High" turns on the Transmit Section of Channel _0 and has no control of the Channel_0 receiver. When TXON_0 = "0" then TTIP_0 and TRING_0 driver outputs will be tri-stated. ***NOTE:*** *In **Hardware** mode only, all receiver channels will be turned on upon power-up and there is no provision to power them off. The receive channels can only be independently powered on or off in **Host** mode.* **In Host mode** The TXON_n bits in the channel control registers turn each channel Transmit section ON or OFF. However, control of the transmit on/off function can be transferred to the **Hardware** pins by setting the TXONCTL bit (bit 6) to "1" in the register at address hex 0x42.
TXON_1	123		**Transmitter Turn On for Channel _1**
TXON_2	124		**Transmitter Turn On for Channel _2**
TXON_3	125		**Transmitter Turn On for Channel _3** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
HW_$\overline{\text{HOST}}$	68	**I**	**Mode Control Input** This pin selects **Hardware** or **Host mode**. Leave this pin unconnected or tie "High" to select **Hardware mode**. For **Host mode**, this pin must be tied "Low". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
$\overline{\text{WR}}$_R/$\overline{\text{W}}$	69	**I**	**Write Input (Read/Write)** - **Host mode** **Intel bus timing:** A "Low" pulse on $\overline{\text{WR}}$ selects a write operation when $\overline{\text{CS}}$ pin is "Low". **Motorola bus timing:** A "High" pulse on R/$\overline{\text{W}}$ selects a read operation and a "Low" pulse on R/$\overline{\text{W}}$ selects a write operation when $\overline{\text{CS}}$ is "Low".
TAOS_0	69		**Transmit All "Ones" Channel_0 - Hardware Mode** See "Transmit All Ones for Channel _0 - Hardware mode" on page 7. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{RD}}$_$\overline{\text{DS}}$	70	**I**	**Read Input (Data Strobe) - Host Mode** **Intel bus timing:** A "Low" pulse on $\overline{\text{RD}}$ selects a read operation when the $\overline{\text{CS}}$ pin is "Low". **Motorola bus timing:** A "Low" pulse on $\overline{\text{DS}}$ indicates a read or write operation when the $\overline{\text{CS}}$ pin is "Low".
TAOS_1	70		**Transmit All "Ones" Channel_1 - Hardware Mode** See "Transmit All Ones for Channel _0 - Hardware mode" on page 7. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
ALE_$\overline{\text{AS}}$	71	**I**	**Address Latch Input (Address Strobe) - Host Mode** **Intel bus timing:** The address inputs are latched into the internal register on the falling edge of ALE. **Motorola bus timing:** The address inputs are latched into the internal register on the falling edge of $\overline{\text{AS}}$.
TAOS_2	71		**Transmit All "Ones" Channel_2 - Hardware Mode** See "Transmit All Ones for Channel _0 - Hardware mode" on page 7. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{CS}}$	72	**I**	**Chip Select Input - Host Mode** This signal must be "Low" in order to access the parallel port.
TAOS_3	72		**Transmit All "Ones" Channel_3 - Hardware Mode** See "Transmit All Ones for Channel _0 - Hardware mode" on page 7. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
RDY_$\overline{\text{DTACK}}$	73	**O**	**Ready Output (Data Transfer Acknowledge Output) - Host Mode** **Intel bus timing**: RDY is asserted "High" to indicate the device has completed a read or write operation. **Motorola bus timing:** $\overline{\text{DTACK}}$ is asserted "Low" to indicate the device has completed a read or write cycle.
RXMUTE	73	**I**	**Receive Muting - Hardware mode** See "Receive Muting - Hardware mode" on page 5. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>µPTS1
µPTS2

RCLKE

TCLKE</td><td>106
107

106

107</td><td>I</td><td>Microprocessor Type Select Input Pins - Host Mode:
Microprocessor Type Select Input Bit 1
Microprocessor Type Select Input Bit 2
<table><tr><th>µPTS2</th><th>µPTS1</th><th>µP Type</th></tr><tr><td>0</td><td>0</td><td>68HC11, 8051, 80C188 (async.)</td></tr><tr><td>0</td><td>1</td><td>Motorola 68K (async.)</td></tr><tr><td>1</td><td>0</td><td>Intel x86 (sync.)</td></tr><tr><td>1</td><td>1</td><td>Motorola 860 (sync.)</td></tr></table>Receive Clock Edge select - Hardware mode
See “Receive Clock Edge - Hardware Mode” on page 5.
Transmit Clock Edge select - Hardware mode
See “Transmit Clock Edge - Hardware Mode” on page 6.
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>D[7]
D[6]
D[5]
D[4]
D[3]
D[2]/
D[1]/
D[0]/
LOOP1_0
LOOP0_0
LOOP1_1
LOOP0_1
LOOP1_2
LOOP0_2
LOOP1_3
LOOP0_3</td><td>42
43
44
45
46
47
48
49
42
43
44
45
46
47
48
49</td><td>I/O</td><td>Microprocessor Read/Write Data Bus Pins - Host Mode
Data Bus[7]
Data Bus[6]
Data Bus[5]
Data Bus[4]
Data Bus[3]
Data Bus[2]
Data Bus[1]
Data Bus[0]
Loop-back Control pin, Bits [1:0]_Channel_n - Hardware Mode
Pins 42 - 49 control which Loop-Back mode is selected per channel. See “Loop-Back Control Pins - Hardware Mode:” on page 14.
NOTE: Internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>µPCLK

ATAOS</td><td>50</td><td>I</td><td>Microprocessor Clock Input - Host Mode
Input clock for synchronous microprocessor operation. Maximum clock rate is 54 MHz.
NOTE: This pin is internally pulled “Low” for asynchronous microprocessor interface when no clock is present.
Automatic Transmit "All Ones” - Hardware mode
This pin functions as an Automatic Transmit “All Ones”. See “Automatic Transmit “All Ones” Pattern - Hardware Mode” on page 13.</td></tr>
</table>

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
			Microprocessor Address Pins - Host mode:
A[6]	57	**I**	**Microprocessor Interface Address Bus[6]**
A[5]	58		**Microprocessor Interface Address Bus[5]**
A[4]	59		**Microprocessor Interface Address Bus[4]**
A[3]	60		**Microprocessor Interface Address Bus[3]**
A[2]	61		**Microprocessor Interface Address Bus[2]**
A[1]	62		**Microprocessor Interface Address Bus[1]**
A[0]	63		**Microprocessor Interface Address Bus[0]**
			Jitter Attenuator Select Pins - Hardware Mode
JASEL1	57		**Jitter Attenuator select pin 1**
JASEL0	58		**Jitter Attenuatore select pin 0** See "Jitter Attenuator" on page 11.
			Equalizer Control Pins - Hardware Mode
EQC4	59		**Equalizer Control Input pin 4**
EQC3	60		**Equalizer Control Input pin 3**
EQC2	61		**Equalizer Control Input pin 2**
EQC1	62		**Equalizer Control Input pin 1**
EQC0	63		**Equalizer Control Input pin 0** Pins EQC[4:0] select the Receive Equalizer and Transmitter Line Build Out. See "Alarm Function//Redundancy Support" on page 13. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{INT}$	119	**I**	**Interrupt Output - Host Mode** This pin goes "Low" to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to "0" in the command control register.
TRATIO	119		**Transmitter Transformer Ratio Select - Hardware mode** The function of this pin is to select the transmitter transformer ratio. See "Alarm Function//Redundancy Support" on page 13. ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*

JITTER ATTENUATOR

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>JASEL0
JASEL1</td><td>58
57</td><td>I</td><td>Jitter Attenuator Select Pins - Hardware Mode
Jitter Attenuator select pin 0
Jitter Attenuator select pin 1
JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it.

<table>
<tr><th rowspan="2">JASEL1</th><th rowspan="2">JASEL0</th><th rowspan="2">JA Path</th><th colspan="2">JA BW Hz</th><th rowspan="2">FIFO Size</th></tr>
<tr><th>T1</th><th>E1</th></tr>
<tr><td>0</td><td>0</td><td>Disabled</td><td>-----</td><td>-----</td><td>--------</td></tr>
<tr><td>0</td><td>1</td><td>Transmit</td><td>3</td><td>10</td><td>32/32</td></tr>
<tr><td>1</td><td>0</td><td>Receive</td><td>3</td><td>10</td><td>32/32</td></tr>
<tr><td>1</td><td>1</td><td>Receive</td><td>3</td><td>1.5</td><td>64/64</td></tr>
</table>
</td></tr>
<tr><td>A[6]
A[5]</td><td>57
58</td><td></td><td>Microprocessor Address Bits A[6:5] -Host Mode
See “Microprocessor Address Pins - Host mode:” on page 10.
NOTE: Internally pulled “Low” with a 50kΩ resistor.</td></tr>
</table>

CLOCK SYNTHESIZER

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
MCLKE1	32	**I**	**E1 Master Clock Input** A 2.048MHz clock for with an accuracy of better than ±50ppm and a duty cycle of 40% to 60% can be provided at this pin. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. ***NOTES:*** *1. All channels of the XRT83SL34 must be operated at the same clock rate, either T1, E1 or J1.* *2. Internally pulled "Low" with a 50kΩ resistor.*
CLKSEL0 **CLKSEL1** **CLKSEL2**	37 38 39	**I**	**Clock Select inputs for Master Clock Synthesizer - Hardware mode** CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an accurate external clock source according to the following table. The MCLKRATE control signal is generated from the state of EQC[4:0] inputs. See Table 4 for description of Transmit Equalizer Control bits. **Host Mode:** The state of these pins are ignored and the master frequency PLL is controlled by the corresponding interface bits. See Table 35, register address 1000001.

MCLKE1 (kHz)	MCLKT1 (kHz)	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	CLKOUT (KHz)
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544
8	X	0	1	0	0	2048
8	X	0	1	0	1	1544
16	X	0	1	1	0	2048
16	X	0	1	1	1	1544
56	X	1	0	0	0	2048
56	X	1	0	0	1	1544
64	X	1	0	1	0	2048
64	X	1	0	1	1	1544
128	X	1	1	0	0	2048
128	X	1	1	0	1	1544
256	X	1	1	1	0	2048
256	X	1	1	1	1	1544

NOTE: *These pins are internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
MCLKT1	33	**I**	**T1 Master Clock Input** This signal is an independent 1.544MHz clock for T1 systems with required accuracy of better than ±50ppm and duty cycle of 40% to 60%. MCLKT1 input is used in the T1 mode. ***NOTES:*** *1. All channels of the XRT83SL34 must be operated at the same clock rate, either T1, E1 or J1.* *2. See pin 32 description for further explanation for the usage of this pin.* *3. Internally pulled "Low" with a 50kΩ resistor.*
MCLKOUT	36	**O**	**Synthesized Master Clock Output** This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.

ALARM FUNCTION//REDUNDANCY SUPPORT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
GAUGE	87	**I**	**Twisted Pair Cable Wire Gauge Select - Hardware mode** Connect this pin "High" to select 26 Gauge wire. Connect this pin "Low" to select 22 and 24 gauge wire for all channels. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
DMO_0	64	**O**	**Driver Failure Monitor Channel _0** This pin transitions "High" if a short circuit condition is detected in the transmit driver of Channel _0, or no transmit output pulse is detected for more than 128 TCLK_0 cycles.
DMO_1	65		**Driver Failure Monitor Channel _1**
DMO_2	66		**Driver Failure Monitor Channel _2**
DMO_3	67		**Driver Failure Monitor Channel _3**
ATAOS	50	**I**	**Automatic Transmit "All Ones" Pattern - Hardware Mode** A "High" level on this pin enables the automatic transmission of an "All Ones" AMI pattern from the transmitter of any channel that the receiver of that channel has detected an LOS condition. A "Low" level on this pin disables this function. ***NOTE:*** *All channels share the same ATAOS input control function.*
μPCLK			**Microprocessor Clock Input - Host Mode** See "Microprocessor Clock Input - Host Mode" on page 9. ***NOTE:*** *This pin is internally pulled "Low" for asynchronous microprocessor interface when no clock is present.*

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>TRATIO</td><td>119</td><td>I</td><td>Transmitter Transformer Ratio Select - Hardware Mode
In external termination mode (TXSEL = 0), setting this pin "High" selects a transformer ratio of 1:2 for the transmitter. A "Low" on this pin sets the transmitter transformer ratio to 1:2.45. In the internal termination mode the transmitter transformer ratio is permanently set to 1:2 and the state of this pin is ignored.</td></tr>
<tr><td>$\overline{\text{INT}}$</td><td>O</td><td>Interrupt Output - Host Mode
This pin is asserted “Low” to indicate an alarm condition. See “Microprocessor Interface” on page 8.
NOTE: This pin is an open drain output and requires an external 10kΩ pull-up resistor.</td></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>121</td><td>I</td><td>Hardware Reset (Active "Low")
When this pin is tied “Low” for more than 10µs, the device is put in the reset state.
Pulling $\overline{\text{RESET}}$ and $\overline{\text{ICT}}$ pins “Low” simultaneously will put the chip in factory test mode. This condition should not be permitted during normal operation.
NOTE: Internally pulled “High” with a 50kΩ resistor.</td></tr>
<tr><td>SR/$\overline{\text{DR}}$</td><td>16</td><td>I</td><td>Single-Rail/Dual-Rail Data Format
Connect this pin "Low" to select transmit and receive data format in Dual-rail mode. In this mode, HDB3 or B8ZS encoder and decoder are not available.
Connect this pin "High" to select single-rail data format.
NOTE: Internally pulled "Low" with a 50kΩ resistor.</td></tr>
<tr><td>LOOP1_0
LOOP0_0
LOOP1_1
LOOP0_1
LOOP1_2
LOOP0_2
LOOP1_3
LOOP0_3</td><td>42
43
44
45
46
47
48
49</td><td>I/O</td><td>Loop-Back Control Pins - Hardware Mode:
Loop-back control pin 1 - Channel _0
Loop-back control pin 0 - Channel _0
Loop-back control pin 1 - Channel _1
Loop-back control pin 0 - Channel _1
Loop-back control pin 1 - Channel _2
Loop-back control pin 0 - Channel _2
Loop-back control pin 1 - Channel _3
Loop-back control pin 0 - Channel _3
<table><tr><th>LOOP1_n</th><th>LOOP0_n</th><th>MODE</th></tr><tr><td>0</td><td>0</td><td>Normal Mode No Loop-back Channel_n</td></tr><tr><td>0</td><td>1</td><td>Local Loop-Back Channel_n</td></tr><tr><td>1</td><td>0</td><td>Remote Loop-Back Channel_n</td></tr><tr><td>1</td><td>1</td><td>Digital Loop-Back Channel_n</td></tr></table></td></tr>
<tr><td>D[7]
D[6]
D[5]
D[4]
D[3]
D[2]
D[1]
D[0]</td><td>42
43
44
45
46
47
48
49</td><td></td><td>Microprocessor R/W Data bits [7:0] - Host Mode
These pins are microprocessor data bus pins. See “Microprocessor Read/Write Data Bus Pins - Host Mode” on page 9.
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
</table>

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
EQC4 **EQC3** **EQC2** **EQC1** **EQC0** **A[4]** **A[3]** **A[2]** **A[1]** **A[0]**	59 60 61 62 63 59 60 61 62 63	**I**	**Equalizer Control Input 4 - Hardware Mode** This pin together with EQC[3:0] are used for controlling the transmit pulse shaping, transmit line build-out (LBO), receive monitoring and also to select T1, E1 or J1 Modes of operation. See Table 4 for description of Transmit Equalizer Control bits. **Equalizer Control Input 3** **Equalizer Control Input 2** **Equalizer Control Input 1** **Equalizer Control Input 0** ***NOTES:*** 1. *In **Hardware mode** all transmit channels share the same pulse setting controls function.* 2. *All channels of an XRT83SL34 must operate at the same clock rate, either the T1, E1 or J1 modes.* **Microprocessor Address bits [4:0] - Host Mode** See "Microprocessor Address Pins - Host mode:" on page 10. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
RXTSEL	110	**I**	**Receiver Termination Select** In Hardware mode, when this pin is "Low" the receive line termination is determined only by the external resistor. When "High", the receive termination is realized by internal resistors or the combination of internal and external resistors. These conditions are described in the table below. ***NOTE:*** *In **Hardware mode** all channels share the same RXTSEL control function.* **RXTSEL** / **RX Termination** **0** / **External** **1** / **Internal** In **Host mode**, the RXTSEL_n bits in the channel control registers determines if the receiver termination is external or internal. However the function of RXTSEL can be transferred to the Hardware pin by setting the TERCNTL bit (bit 4) to "1" in the register 66 address hex 0x42. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TXTSEL	111	**I**	**Transmit Termination Select - Hardware Mode** When this pin is "Low" the transmit line termination is determined only by an external resistor. When "High", the transmit termination is realized only by the internal resistor. **TXTSEL** / **TX Termination** **0** / **External** **1** / **Internal** ***NOTES:*** 1. *This pin is internally pulled "Low" with a 50kΩ resistor.* 2. *In **Hardware Mode** all channels share the same TXTSEL control function.*

<table>
<tr><th>SIGNAL NAME</th><th>PIN #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>TERSEL0
TERSEL1</td><td>113
112</td><td>I</td><td>
Termination Impedance Select pin 0
Termination Impedance Select pin 1
In the Hardware mode and in the internal termination mode (TXTSEL="1" and RXTSEL="1"), TERSEL[1:0] control the transmit and receive termination impedance according to the following table.
<table>
<tr><th>TERSEL1</th><th>TERSEL0</th><th>Termination</th></tr>
<tr><td>0</td><td>0</td><td>100Ω</td></tr>
<tr><td>0</td><td>1</td><td>110Ω</td></tr>
<tr><td>1</td><td>0</td><td>75Ω</td></tr>
<tr><td>1</td><td>1</td><td>120Ω</td></tr>
</table>
In the internal termination mode, the receiver termination of each receiver is realized completely by internal resistors or by the combination of internal and one fixed external resistor (see description of RXRES[1:0] pins).
In the internal termination mode the transformer ratio of 1:2 and 1:1 is required for transmitter and receiver respectively with the transmitter output AC coupled to the transformer.
NOTES:
1. This pin is internally pulled "Low" with a 50kΩ resistor.
2. In Hardware Mode all channels share the same TERSEL control function.
</td></tr>
<tr><td>$\overline{\text{ICT}}$</td><td>120</td><td>I</td><td>
In-Circuit Testing (active "Low"):
When this pin is tied “Low”, all output pins are forced to a “High” impedance state for in-circuit testing.
Pulling $\overline{\text{RESET}}$ and $\overline{\text{ICT}}$ pins “Low” simultaneously will put the chip in factory test mode. This condition should not be permitted during normal operation.
NOTE: Internally pulled “High” with a 50kΩ resistor.
</td></tr>
</table>

POWER AND GROUND

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TGND_0	12	****	**Transmitter Analog Ground for Channel _0**
TGND_1	20		**Transmitter Analog Ground for Channel _1**
TGND_2	83		**Transmitter Analog Ground for Channel _2**
TGND_3	91		**Transmitter Analog Ground for Channel _3**
TVDD_0	14	****	**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _0**
TVDD_1	18		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _1**
TVDD_2	85		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _2**
TVDD_3	89		**Transmitter Analog Positive Supply (3.3V ± 5%) for Channel _3**
RVDD_0	8	****	**Receiver Analog Positive Supply (3.3V± 5%) for Channel _0**
RVDD_1	24		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _1**
RVDD_2	79		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _2**
RVDD_3	95		**Receiver Analog Positive Supply (3.3V± 5%) for Channel _3**
RGND_0	11	****	**Receiver Analog Ground for Channel _0**
RGND_1	21		**Receiver Analog Ground for Channel _1**
RGND_2	82		**Receiver Analog Ground for Channel _2**
RGND_3	92		**Receiver Analog Ground for Channel _3**
VDDPLL_1	30	****	**Analog Positive Supply for Master Clock Synthesizer PLL (3.3V± 5%)**
VDDPLL_2	31		**Analog Positive Supply for Master Clock Synthesizer PLL (3.3V± 5%)**
AVDD	40		**Analog Positive Supply (3.3V± 5%)**
GNDPLL_1	34	****	**Analog Ground for Master Clock Synthesizer PLL**
GNDPLL_2	35		**Analog Ground for Master Clock Synthesizer PLL**
AGND	41		**Analog Ground**
DVDD	29	****	**Digital Positive Supply (3.3V± 5%)**
DVDD	51		**Digital Positive Supply (3.3V± 5%)**
DVDD	52		**Digital Positive Supply (3.3V± 5%)**
DVDD	53		**Digital Positive Supply (3.3V± 5%)**
DVDD	115		**Digital Positive Supply (3.3V± 5%)**
DVDD	116		**Digital Positive Supply (3.3V± 5%)**
DGND	54	****	**Digital Ground**
DGND	55		**Digital Ground**
DGND	56		**Digital Ground**
DGND	74		**Digital Ground**
GND	114		**Ground**
DGND	117		**Digital Ground**
DGND	118		**Digital Ground**

FUNCTIONAL DESCRIPTION

The XRT83SL34 is a fully integrated four chnnel short-haul transceiver intended for T1, J1 or E1 systems. Simplified block diagrams of the device are shown in Figure 1, **Host** mode and Figure 2, **Hardware** mode.

In T1 applications, the XRT83SL34 can generate five transmit pulse shapes to meet the short-haul Digital Cross-connect (DSX-1) template requirement. The operation and configuration of the XRT83SL34 can be controlled through a parallel microprocessor **Host** interface or **Hardware** control.

MASTER CLOCK GENERATOR

Using a variety of external clock sources, the on-chip frequency synthesizer generates the T1 (1.544MHz) or E1 (2.048MHz) master clocks necessary for the transmit pulse shaping and receive clock recovery circuit.

There are two master clock inputs MCLKE1 and MCLKT1. In systems where both T1 and E1 master clocks are available these clocks can be connected to the respective pins. All channels of a given XRT83SL34 must be operated at the same clock rate, either T1, E1 or J1 modes.

In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. T1 or E1 master clocks can be generated from 8kHz, 16kHz, 56kHz, 64kHz, 128kHz and 256kHz external clocks under the control of CLKSEL[2:0] inputs according to Table 1.

NOTE: *EQC[4:0] determine the T1/E1 operating mode. See* ***Table 5*** *for details.*

FIGURE 4. TWO INPUT CLOCK SOURCE

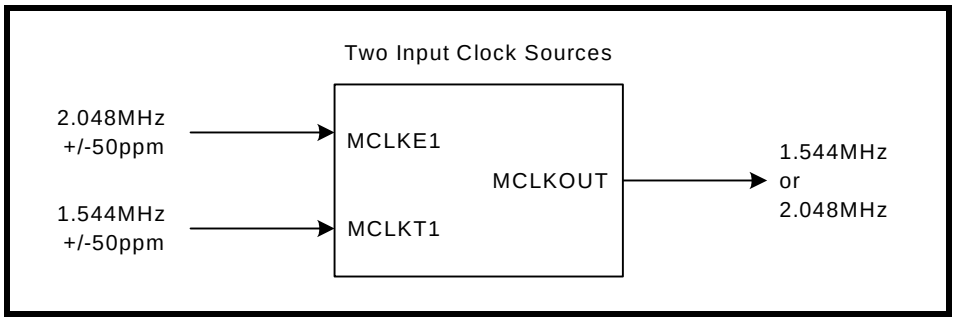


FIGURE 5. ONE INPUT CLOCK SOURCE

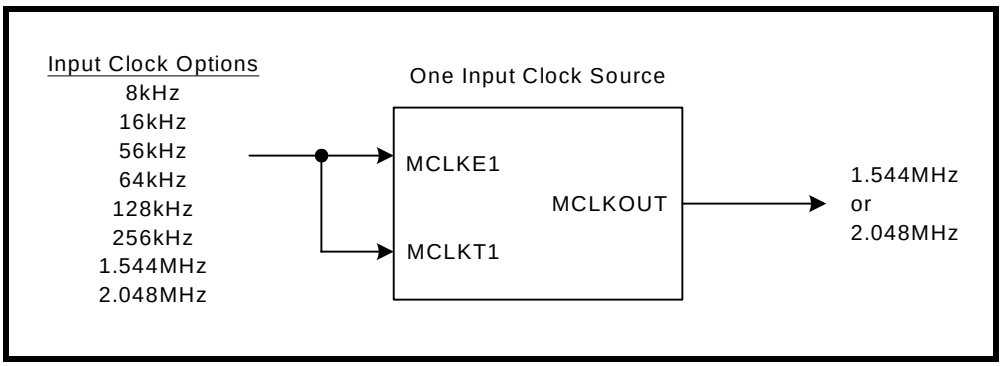


TABLE 1: MASTER CLOCK GENERATOR

MCLKE1 kHz	MCLKT1 kHz	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	MASTER CLOCK kHz
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544
8	x	0	1	0	0	2048
8	x	0	1	0	1	1544
16	x	0	1	1	0	2048
16	x	0	1	1	1	1544
56	x	1	0	0	0	2048
56	x	1	0	0	1	1544
64	x	1	0	1	0	2048
64	x	1	0	1	1	1544
128	x	1	1	0	0	2048
128	x	1	1	0	1	1544
256	x	1	1	1	0	2048
256	x	1	1	1	1	1544

In **Host** mode the programming is achieved through the corresponding interface control bits, the state of the CLKSEL[2:0] control bits and the state of the MCLKRATE interface control bit.

RECEIVER

In **Hardware** mode all receive channels are turned on upon power-up and there is no provision supplied to power them off. In **Host** mode, each receiver channel can be individually powered on or off with its respective channel RXON_n bit. See “Microprocessor Register #0, Bit Description” on page 45.

RECEIVER INPUT

At the receiver input, a cable attenuated AMI signal can be coupled to the receiver through a capacitor or a 1:1 transformer. The input signal is first applied to a selective equalizer for signal conditioning. The maximum equalizer gain is up to 36 dB for both T1 and E1 modes. The equalized signal is subsequently applied to a peak detector which in turn controls the equalizer settings and the data slicer. The slicer threshold for both E1 and T1 is typically set at 50% of the peak amplitude at the equalizer output. After the slicers, the digital representation of the AMI signals are applied to the clock and data recovery circuit. The recovered data subsequently goes through the jitter attenuator and decoder (if selected) for HDB3 or B8ZS decoding before being applied to the RPOS_n/RDATA_n and RNEG_n/LCV_n pins. Clock recovery is accomplished by a digital phase-locked loop (DPLL) which does not require any external components and can tolerate high levels of input jitter that meets or exceeds the ITU-G.823 and TR-TSY000499 standards.

RECEIVE MONITOR MODE

In applications where Monitor mode is desired, the equalizer can be configured in a gain mode which handles input signals attenuated resistively up to 29dB, along with 0 to 6dB cable attenuation for both T1 and E1 applications, refer to Table 5 for details. This feature is available in both **Hardware** and **Host** modes.

RECEIVER LOSS OF SIGNAL (RLOS)

For compatibility with ITU G.775 requirements, the RLOS monitoring function is implemented using both analog and digital detection schemes. If the analog RLOS condition occurs, a digital detector is activated to count for 32 consecutive zeros in E1 (4096 bits in Extended Los mode, EXLOS = "1") or 175 consecutive zeros in T1 before RLOS is asserted. RLOS is cleared when the input signal rises +3dB (built in hysteresis) above the point at which it was declared and meets 12.5% ones density of 4 ones in a 32 bit window, with no more than 16 consecutive zeros for E1. In T1 mode, RLOS is cleared when the input signal rises +3dB (built in hysteresis) above the point at which it was declared and contains 16 ones in a 128 bit window with no more than 100 consecutive zeros in the data stream. When loss of signal occurs, RLOS register indication and register status will change. If the RLOS register enable is set high (enabled), the alarm will trigger an interrupt causing the interrupt pin (INT) to go low. Once the alarm status register has been read, it will automatically reset upon read (RUR), and the INT pin will return high.

Analog RLOS

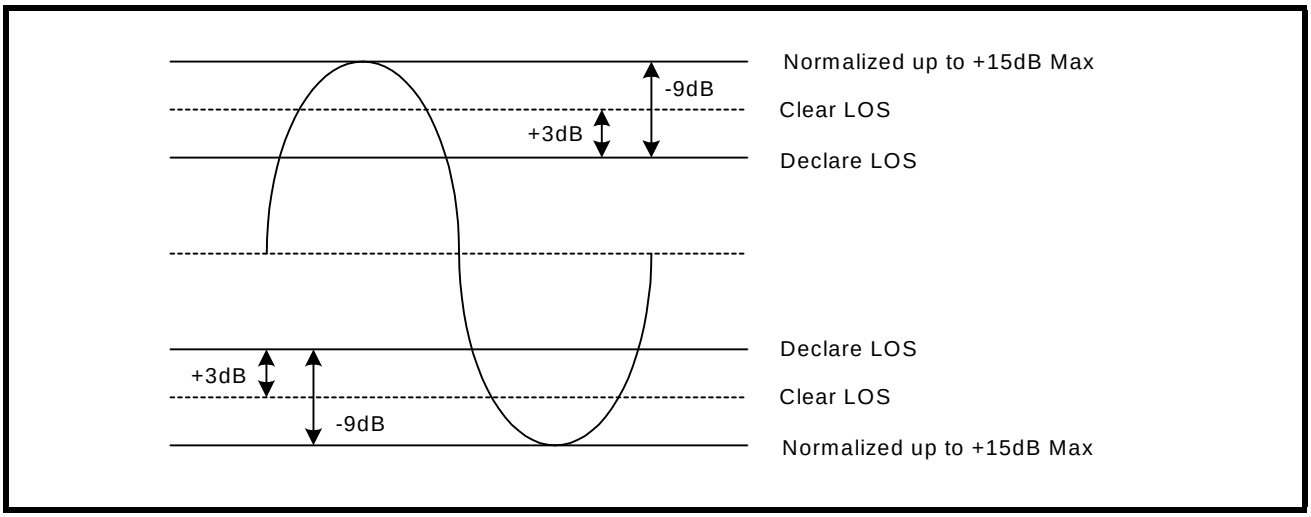
Setting the Receiver Inputs to -15dB T1/E1 Short Haul Mode

By setting the receiver inputs to -15dB T1/E1 short haul mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +15dB normalizing the T1/E1 input signal.

NOTE: *This is the only setting that refers to cable loss (frequency), not flat loss (resistive).*

Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+15dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -24dB (-15dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total cable attenuation of -21dB. See Figure 6 for a simplified diagram.

FIGURE 6. SIMPLIFIED DIAGRAM OF -15dB T1/E1 SHORT HAUL MODE AND RLOS CONDITION



Setting the Receiver Inputs to -29dB T1/E1 Gain Mode

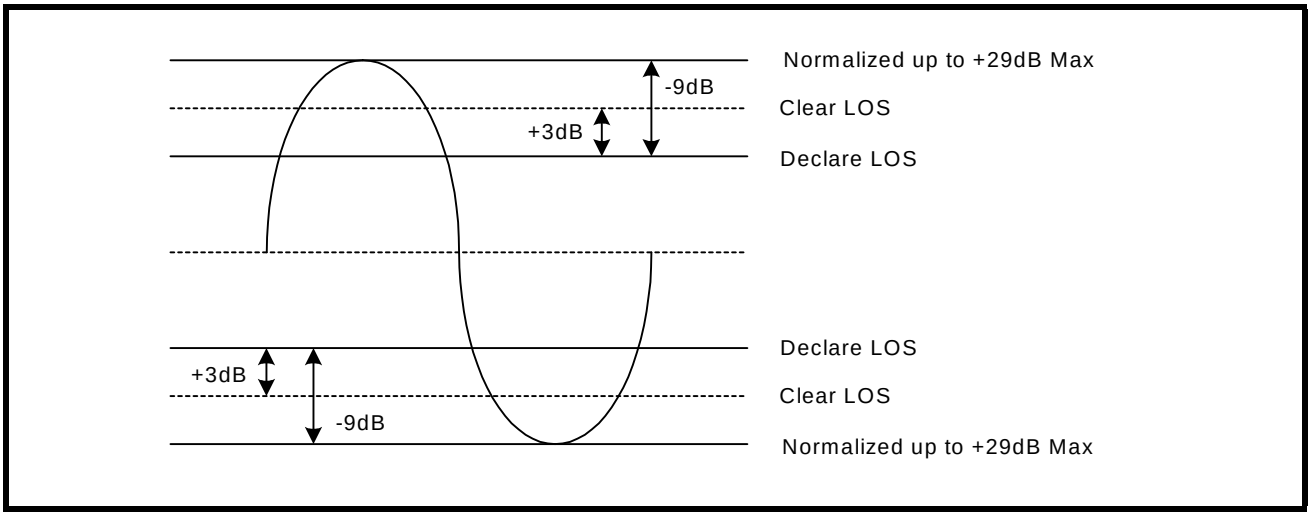
By setting the receiver inputs to -29dB T1/E1 gain mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +29dB normalizing the T1/E1 input signal.

NOTE: *This is the only setting that refers to flat loss (resistive). All other modes refer to cable loss (frequency).*

Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+29dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is

typically -38dB (-29dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total flat loss of -35dB. See Figure 7 for a simplified diagram.

FIGURE 7. SIMPLIFIED DIAGRAM OF -29dB T1/E1 GAIN MODE AND RLOS CONDITION



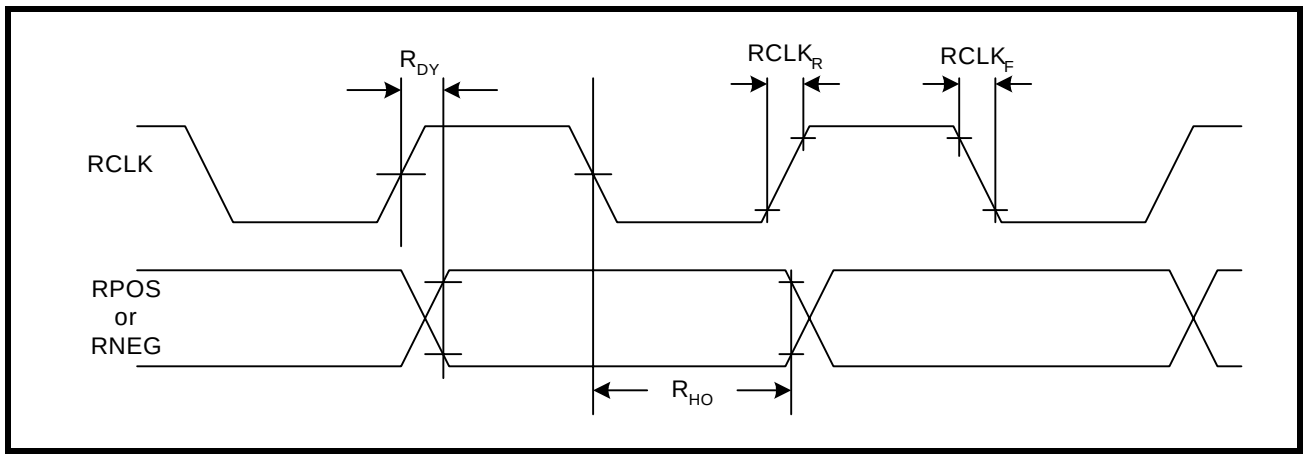
RECEIVE HDB3/B8ZS DECODER

The Decoder function is available in both **Hardware** and **Host** modes on a per channel basis by controlling the TNEG_n/CODES_n pin or the CODES_n interface bit. The decoder function is only active in single-rail Mode. When selected, receive data in this mode will be decoded according to HDB3 rules for E1 and B8ZS for T1 systems. Bipolar violations that do not conform to the coding scheme will be reported as Line Code Violation at the RNEG_n/LCV_n pin of each channel. The length of the LCV pulse is one RCLK cycle for each code violation. In E1mode only, an excessive number of zeros in the receive data stream is also reported as an error at the same output pin. If AMI decoding is selected in single rail mode, every bipolar violation in the receive data stream will be reported as an error at the RNEG_n/LCV_n pin.

RECOVERED CLOCK (RCLK) SAMPLING EDGE

This feature is available in both **Hardware** and **Host** modes on a global basis. In **Host** mode, the sampling edge of RCLK output can be changed through the interface control bit RCLKE. If a “1” is written in the RCLKE interface bit, receive data output at RPOS_n/RDATA_n and RNEG_n/LCV_n are updated on the falling edge of RCLK for all eight channels. Writing a “0” to the RCLKE register, updates the receive data on the rising edge of RCLK. In **Hardware** mode the same feature is available under the control of the RCLKE pin.

FIGURE 8. RECEIVE CLOCK AND OUTPUT DATA TIMING



JITTER ATTENUATOR

To reduce phase and frequency jitter in the recovered clock, the jitter attenuator can be placed in the receive signal path. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth that can vary between 2x32 and 2x64. The jitter attenuator can also be placed in the transmit signal path or disabled altogether depending upon system requirements. The jitter attenuator, other than using the master clock as reference, requires no external components. With the jitter attenuator selected, the typical throughput delay from input to output is 16 bits for 32 bit FIFO size or 32 bits for 64 bit FIFO size. When the read and write pointers of the FIFO in the jitter attenuator are within two bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this situation occurs, the jitter attenuator will not attenuate input jitter until the read/write pointer's position is outside the two bits window. Under normal condition, the jitter transfer characteristic meets the narrow bandwidth requirement as specified in ITU- G.736, ITU- I.431 and AT&T Pub 62411 standards.

In T1 mode the Jitter Attenuator Bandwidth is always set to 3Hz. In E1 mode, the bandwidth can be reduced through the JABW control signal. When JABW is set "High" the bandwidth of the jitter attenuator is reduced from 10Hz to 1.5Hz. Under this condition the FIFO length is automatically set to 64 bits and the 32 bits FIFO length will not be available in this mode. Jitter attenuator controls are available on a per channel basis in the **Host** mode and on a global basis in the **Hardware** mode.

GAPPED CLOCK (JA MUST BE ENABLED IN THE TRANSMIT PATH)

The XRT83SL34 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to T1 or E1 data, stuffing bits are removed which can leave gaps in the incoming data stream. If the jitter attenuator is enabled in the transmit path, the 32-Bit or 64-Bit FIFO is used to smooth the gapped clock into a steady T1 or E1 output. The maximum gap width of the 8-Channel LIU is shown in Table 2.

TABLE 2: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the jitter attenuator should be enabled in the receive path.*