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GENERAL DESCRIPTION

The XRT83VL38 is a fully integrated Octal (eight channel) long-haul and short-haul line interface unit for T1 (1.544Mbps) 100Ω, E1 (2.048Mbps) 75Ω or 120Ω, J1 110Ω or BITS Timing applications.

In long-haul applications the XRT83VL38 accepts signals that have been attenuated from 0 to 36dB at 772kHz in T1 mode (equivalent of 0 to 6000 feet of cable loss) or 0 to 43dB at 1024kHz in E1 mode.

In T1 applications, the XRT83VL38 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions (The arbitrary pulse generators are available in both T1 and E1 modes).

The XRT83VL38 provides both a parallel/serial **Host** microprocessor interface as well as a **Hardware** mode for programming and control.

Both the B8ZS and HDB3 encoding and decoding functions are selectable as well as AMI. Two on-chip crystal-less jitter attenuators with a 32 or 64 bit FIFO can be placed in the receive and the transmit paths with loop bandwidths of less than 3Hz. The XRT83VL38 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. In the absence of the power supply, the transmit outputs and receive inputs are tri-stated allowing for redundancy applications The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master.

APPLICATIONS

- BITS Timing
- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

Features (See Page 2)

FIGURE 1. BLOCK DIAGRAM OF THE XRT83VL38 T1/E1/J1 LIU (HOST MODE)

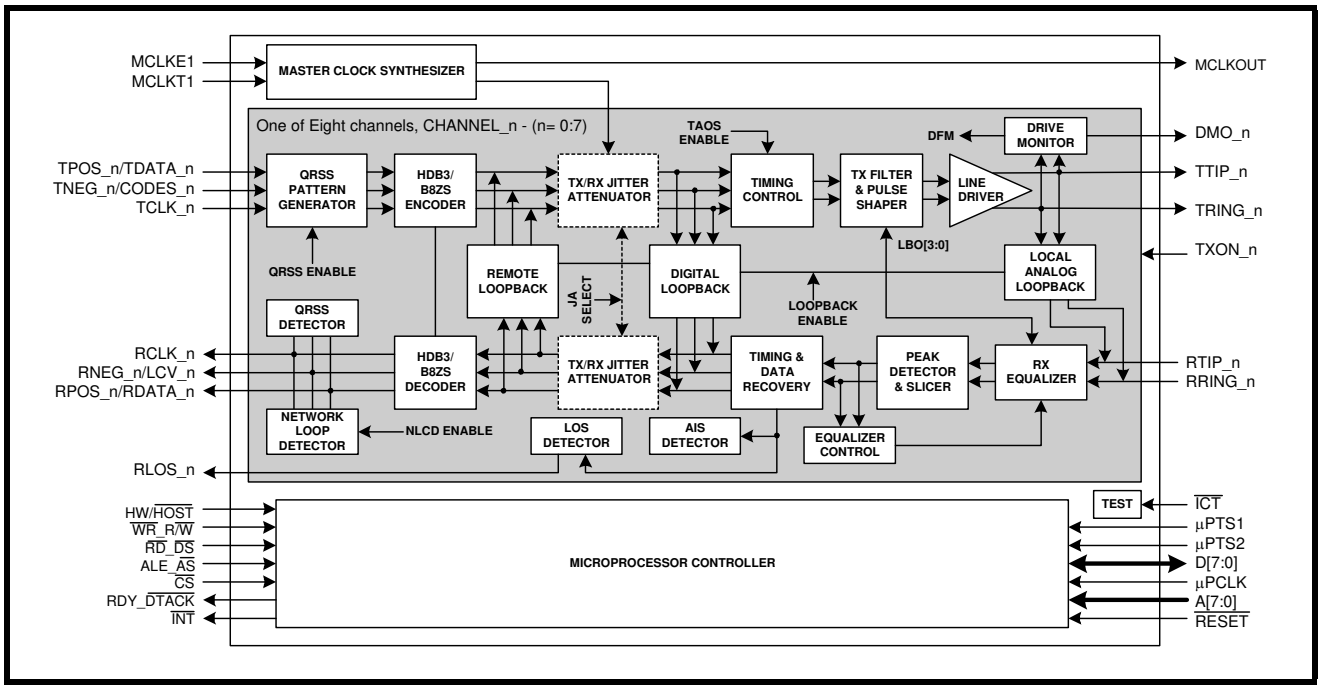
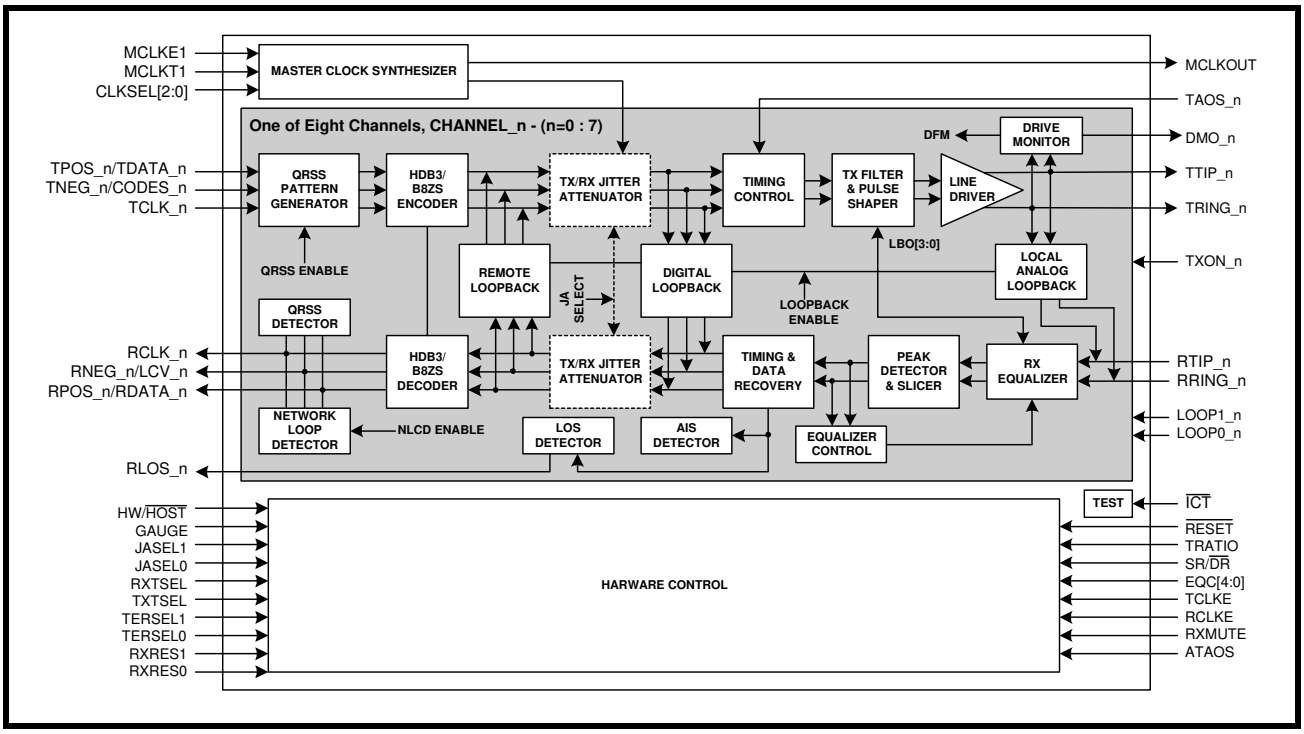


FIGURE 2. BLOCK DIAGRAM OF THE XRT83VL38 T1/E1/J1 LIU (HARDWARE MODE)



FEATURES

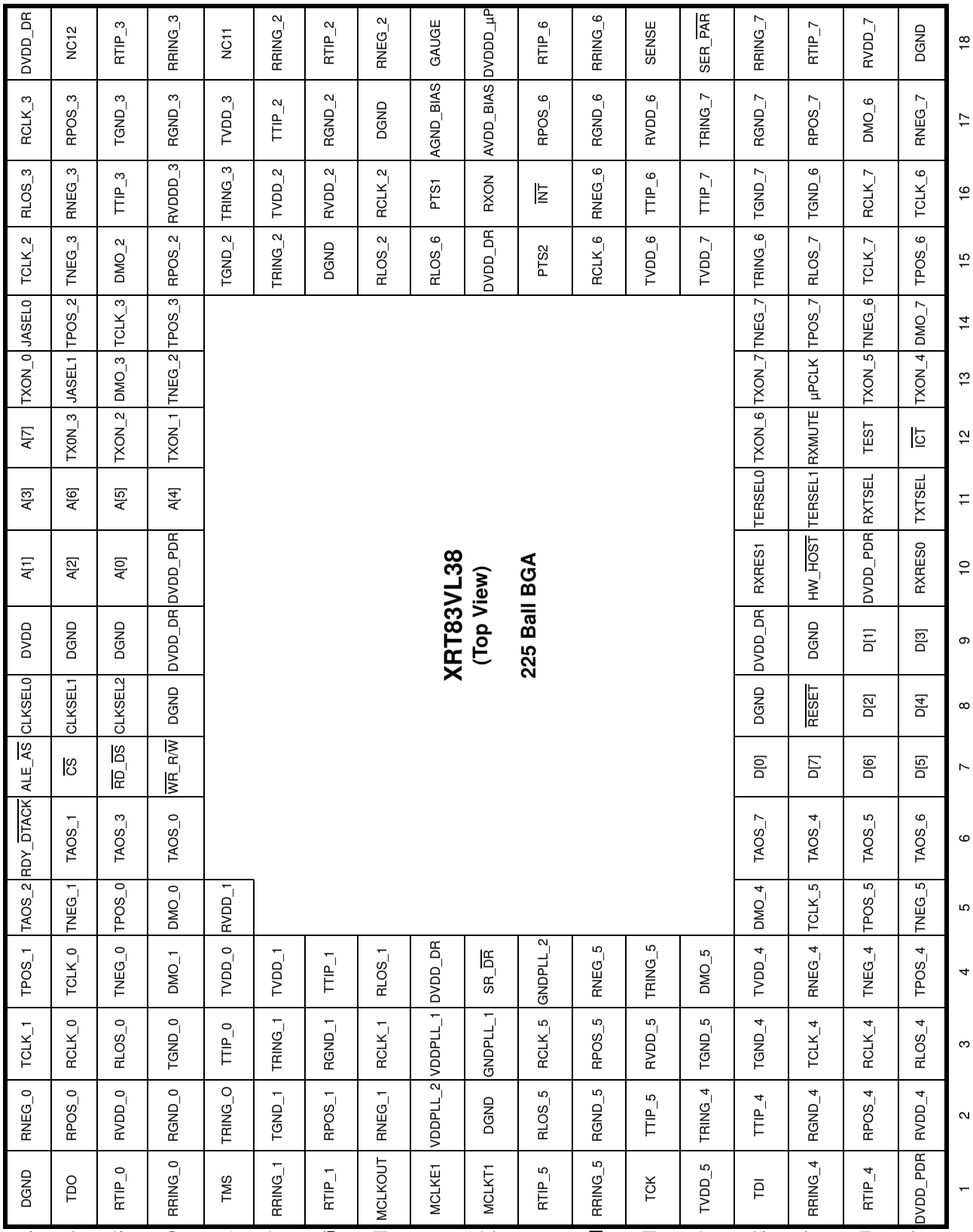
- Supports Section 13 - Synchronization Interface in ITU G.703 for both Transmit and Receive Paths
- Fully integrated eight channel long-haul or short-haul transceivers for E1,T1 or J1 applications
- Adaptive Receive Equalizer for up to 36dB cable attenuation
- Programable Transmit Pulse Shaper for E1,T1 or J1 short-haul interfaces
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping available for both T1 and E1 modes
- Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps
- Selectable receiver sensitivity from 0 to 36dB cable loss for T1 @772kHz and 0 to 43dB for E1 @1024kHz
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for E1 and 0 to 3dB of cable attenuation for T1 modes
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications
- Internal and/or external impedance matching for 75Ω, 100Ω, 110Ω and 120Ω
- Tri-State transmit output and receive input capability for redundancy applications
- Provides High Impedance for Tx and Rx during power off
- Transmit return loss meets or exceeds ETSI 300-166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO selectable in transmit or receive paths
- On-chip frequency multiplier generates T1 or E1 Master clocks
- High receiver interference immunity
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)

- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder functions
- QRSS pattern generator and detection for testing and monitoring
- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Local Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both **Hardware** and **Host** (parallel or serial) Microprocessor interface for programming
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Dual 3.3V and 1.8V Supply Operation
- 225 ball BGA package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83VL38IB	225 Ball BGA	-40°C to +85°C

FIGURE 3. PACKAGE PIN OUT



PIN DESCRIPTION BY FUNCTION

RECEIVE SECTIONS

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RxON	K16	**I**	**Receiver On - Harware Mode** Writing a "1" to this pin in **Hardware** mode turns on the Receive Sections of all channels. Writing a "0" shuts off the Receiver Sections of all channels.
RLOS_0	C3	**O**	**Receiver Loss of Signal for Channel_ 0:** This output signal goes "High" for at least one RCLK_0 cycle to indicate loss of signal at the receive 0 input. RLOS will remain "High" for the entire duration of the Loss of Signal detected by the receiver logic. **SEE"RECEIVER LOSS OF SIGNAL (RLOS)" ON PAGE 25.**
RLOS_1	H4		**Receiver Loss of Signal for Channel _1**
RLOS_2	H15		**Receiver Loss of Signal for Channel _2**
RLOS_3	A16		**Receiver Loss of Signal for Channel _3**
RLOS_4	V3		**Receiver Loss of Signal for Channel _4**
RLOS_5	L2		**Receiver Loss of Signal for Channel_ 5**
RLOS_6	J15		**Receiver Loss of Signal for Channel _6**
RLOS_7	T15		**Receiver Loss of Signal for Channel _7**
RCLK_0	B3	**O**	**Receiver Clock Output for Channel _0**
RCLK_1	H3		**Receiver Clock Output for Channel _1**
RCLK_2	H16		**Receiver Clock Output for Channel _2**
RCLK_3	A17		**Receiver Clock Output for Channel _3**
RCLK_4	U3		**Receiver Clock Output for Channel _4**
RCLK_5	L3		**Receiver Clock Output for Channel _5**
RCLK_6	M15		**Receiver Clock Output for Channel _6**
RCLK_7	U16		**Receiver Clock Output for Channel _7**
RNEG_0	A2	**O**	**Receiver Negative Data Output for Channel_0 - Dual-Rail mode** This signal is the receive negative-rail output data.
LCV_0	A2		**Line Code Violation Output for Channel_0 - Single-Rail mode** This signal goes "High" for one RCLK_0 cycle to indicate a code violation is detected in the received data of Channel _0. If AMI coding is selected, every bipolar violation received will cause this pin to go "High".
RNEG_1	H2		**Receiver Negative Data Output for Channel _1**
LCV_1			**Line Code Violation Output for Channel _1**
RNEG_2	H18		**Receiver Negative Data Output for Channel _2**
LCV_2			**Line Code Violation Output for Channel _2**
RNEG_3	B16		**Receiver Negative Data Output for Channel _3**
LCV_3			**Line Code Violation Output for Channel _3**
RNEG_4	T4		**Receiver Negative Data Output for Channel _4**
LCV_4			**Line Code Violation Output for Channel _4**
RNEG_5	M4		**Receiver Negative Data Output for Channel _5**
LCV_5			**Line Code Violation Output for Channel _5**
RNEG_6	M16		**Receiver Negative Data Output for Channel _6**
LCV_6			**Line Code Violation Output for Channel _6**
RNEG_7	V17		**Receiver Negative Data Output for Channel _7**
LCV_7			**Line Code Violation Output for Channel _7**

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RPOS_0	B2	**O**	**Receiver Positive Data Output for Channel _0 - Dual-Rail mode** This signal is the receive positive-rail output data sent to the Framer. **Receiver NRZ Data Output for Channel _0 - Single-Rail mode** This signal is the receive output data.
RDATA_0	B2		
RPOS_1	G2		**Receiver Positive Data Output for Channel _1** **Receiver NRZ Data Output for Channel _1**
RDATA_1			**Receiver Positive Data Output for Channel _2**
RPOS_2	D15		**Receiver NRZ Data Output for Channel _2**
RDATA_2			**Receiver Positive Data Output for Channel _3**
RPOS_3	B17		**Receiver NRZ Data Output for Channel _3**
RDATA_3			**Receiver Positive Data Output for Channel _4**
RPOS_4	U2		**Receiver NRZ Data Output for Channel _4**
RDATA_4			**Receiver Positive Data Output for Channel _5**
RPOS_5	M3		**Receiver NRZ Data Output for Channel _5**
RDATA_5			**Receiver Positive Data Output for Channel _6**
RPOS_6	L17		**Receiver NRZ Data Output for Channel 6**
RDATA_6			**Receiver Positive Data Output for Channel _7**
RPOS_7	T17		**Receiver NRZ Data Output for Channel _7**
RDATA_7			
RTIP_0	C1	**I**	**Receiver Differential Tip Input for Channel _0** Positive differential receive input from the line
RTIP_1	G1		**Receiver Differential Tip Input for Channel _1**
RTIP_2	G18		**Receiver Differential Tip Input for Channel _2**
RTIP_3	C18		**Receiver Differential Tip Input for Channel _3**
RTIP_4	U1		**Receiver Differential Tip Input for Channel _4**
RTIP_5	L1		**Receiver Differential Tip Input for Channel _5**
RTIP_6	L18		**Receiver Differential Tip Input for Channel _6**
RTIP_7	T18		**Receiver Differential Tip Input for Channel _7**
RRING_0	D1	**I**	**Receiver Differential Ring Input for Channel _0** Negative differential receive input from the line
RRING_1	F1		**Receiver Differential Ring Input for Channel _1**
RRING_2	F18		**Receiver Differential Ring Input for Channel _2**
RRING_3	D18		**Receiver Differential Ring Input for Channel _3**
RRING_4	T1		**Receiver Differential Ring Input for Channel _4**
RRING_5	M1		**Receiver Differential Ring Input for Channel _5**
RRING_6	M18		**Receiver Differential Ring Input for Channel _6**
RRING_7	R18		**Receiver Differential Ring Input for Channel _7**
RXMUTE	T12	**I**	**Receive Data Muting** When a LOS condition occurs, the outputs RPOS_n/RNEG_n will be muted, (forced to ground) to prevent data chattering. Tie this pin “Low” to disable the muting function. ***NOTES:*** 1. *This pin is internally pulled “High” with a 50kΩ resistor.* 2. *In **Hardware mode**, all receive channels share the same RXMUTE control function.*

<table>
<tr><th>SIGNAL NAME</th><th>LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RXRES1
RXRES0</td><td>R10
V10</td><td>I</td><td>Receive External Resistor Control Pins - Hardware mode
Receive External Resistor Control Pin 1:
Receive External Resistor Control Pin 0:
These pins determine the value of the external Receive fixed resistor according to the following table:
<table><tr><th>RXRES1</th><th>RXRES0</th><th>Required Fixed External RX Resistor</th></tr><tr><td>0</td><td>0</td><td>No External Fixed Resistor</td></tr><tr><td>0</td><td>1</td><td>240Ω</td></tr><tr><td>1</td><td>0</td><td>210Ω</td></tr><tr><td>1</td><td>1</td><td>150Ω</td></tr></table>
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>RCLKE

µPTS1</td><td>J16

J16</td><td>I</td><td>Receive Clock Edge - Hardware mode
Set this pin “High” to sample RPOS_N/RNEG_n on the falling edge of RCLK_n. With this pin tied “Low”, output data are updated on the rising edge of RCLK_n.
Microprocessor Type Select Input pin 1 - Host mode
This pin along with µPTS2 (pin 128) is used to select the microprocessor type. SEE”MICROPROCESSOR TYPE SELECT INPUT PINS - HOST MODE:” ON PAGE 12.
NOTE: This pin is internally pulled “Low” with a 50kΩ resistor.</td></tr>
</table>

TRANSMITTER SECTIONS

<table>
<tr><th>SIGNAL NAME</th><th>LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>E

µPTS2</td><td>L15

L15</td><td>I</td><td>Transmit Clock Edge - Hardware mode
Set this pin “High” to sample transmit input data on the rising edge of TCLK_n. With this pin tied “Low”, input data are sampled on the falling edge of TCLK_n.
Microprocessor Type Select Input pin 2 - Host mode
This pin along with µPTS1 (pin 133) selects the microprocessor type. SEE”MICROPROCESSOR TYPE SELECT INPUT PINS - HOST MODE:” ON PAGE 12.
NOTE: This pin is internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>TTIP_0</td><td>E3</td><td>O</td><td>Transmitter Tip Output for Channel _0
Positive differential transmit output to the line.</td></tr>
<tr><td>TTIP_1</td><td>G4</td><td></td><td>Transmitter Tip Output for Channel _1</td></tr>
<tr><td>TTIP_2</td><td>F17</td><td></td><td>Transmitter Tip Output for Channel _2</td></tr>
<tr><td>TTIP_3</td><td>C16</td><td></td><td>Transmitter Tip Output for Channel _3</td></tr>
<tr><td>TTIP_4</td><td>R2</td><td></td><td>Transmitter Tip Output for Channel _4</td></tr>
<tr><td>TTIP_5</td><td>N2</td><td></td><td>Transmitter Tip Output for Channel _5</td></tr>
<tr><td>TTIP_6</td><td>N16</td><td></td><td>Transmitter Tip Output for Channel _6</td></tr>
<tr><td>TTIP_7</td><td>P16</td><td></td><td>Transmitter Tip Output for Channel _7</td></tr>
</table>

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TRING_0	E2	**O**	**Transmitter Ring Output for Channel _0** Negative differential transmit output to the line.
TRING_1	F3		**Transmitter Ring Output for Channel _1**
TRING_2	F15		**Transmitter Ring Output for Channel _2**
TRING_3	E16		**Transmitter Ring Output for Channel _3**
TRING_4	P2		**Transmitter Ring Output for Channel _4**
TRING_5	N4		**Transmitter Ring Output for Channel _5**
TRING_6	R15		**Transmitter Ring Output for Channel _6**
TRING_7	P17		**Transmitter Ring Output for Channel _7**
TPOS_0	C5	**I**	**Transmitter Positive Data Input for Channel _0 - Dual-Rail mode** This signal is the positive-rail input data for transmitter 0.
TDATA_0			**Transmitter 0 Data Input - Single-Rail mode** This pin is used as the NRZ input data for transmitter 0.
TPOS_1	A4		**Transmitter Positive Data Input for Channel _1**
TDATA_1			**Transmitter 1 Data Input**
TPOS_2	B14		**Transmitter Positive Data Input for Channel _2**
TDATA_2			**Transmitter 2 Data Input**
TPOS_3	D14		**Transmitter Positive Data Input for Channel _3**
TDATA_3			**Transmitter 3 Data Input**
TPOS_4	V4		**Transmitter Positive Data Input for Channel _4**
TDATA_4			**Transmitter 4 Data Input**
TPOS_5	U5		**Transmitter Positive Data Input for Channel _5**
TDATA_5			**Transmitter 5 Data Input**
TPOS_6	V15		**Transmitter Positive Data Input for Channel _6**
TDATA_6			**Transmitter 6 Data Input**
TPOS_7	T14		**Transmitter Positive Data Input for Channel _7**
TDATA_7			**Transmitter 7 Data Input** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for each channel.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TNEG_0	C4	**I**	**Transmitter Negative NRZ Data Input for Channel _0** **Dual-Rail mode** This signal is the negative-rail input data for transmitter 0. **Single-Rail mode** This pin can be left unconnected.
CODES_0	C4		**Coding Select for Channel _0 - Hardware mode and Single-Rail mode** Connecting this pin "Low" enables HDB3 in E1 or B8ZS in T1 encoding and decoding for Channel _0. Connecting this pin "High" selects AMI data format.
TNEG_1	B5		**Transmitter Negative NRZ Data Input for Channel _1**
CODES_1			**Coding Select for Channel _1**
TNEG_2	D13		**Transmitter Negative NRZ Data Input for Channel _2**
CODES_2			**Coding Select for Channel _2**
TNEG_3	B15		**Transmitter Negative NRZ Data Input for Channel _3**
CODES_3			**Coding Select for Channel _3**
TNEG_4	U4		**Transmitter Negative NRZ Data Input for Channel _4**
CODES_4			**Coding Select for Channel _4**
TNEG_5	V5		**Transmitter Negative NRZ Data Input for Channel _5**
CODES_5			**Coding Select for Channel _5**
TNEG_6	U14		**Transmitter Negative NRZ Data Input for Channel _6**
CODES_6			**Coding Select for Channel _6**
TNEG_7	R14		**Transmitter Negative NRZ Data Input for Channel _7**
CODES_7			**Coding Select for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for each channel.*
TCLK_0	B4	**I**	**Transmitter Clock Input for Channel _0 - Host mode and Hardware mode** **E1** rate at 2.048MHz ± 50ppm. **T1** rate at 1.544MHz ± 32ppm. During normal operation TCLK_0 is used for sampling input data at TPOS_0/ TDATA_0 and TNEG_0/CODES_0 while MCLK is used as the timing reference for the transmit pulse shaping circuit.
			Transmitter Clock Input for Channel _1
TCLK_1	A3		**Transmitter Clock Input for Channel _2**
TCLK_2	A15		**Transmitter Clock Input for Channel _3**
TCLK_3	C14		**Transmitter Clock Input for Channel _4**
TCLK_4	T3		**Transmitter Clock Input for Channel _5**
TCLK_5	T5		**Transmitter Clock Input for Channel _6**
TCLK_6	V16		**Transmitter Clock Input for Channel _7**
TCLK_7	U15		***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TAOS_0	D6	**I**	**Transmit All Ones for Channel _0 - Hardware mode** Setting this pin "High" enables the transmission of an "All Ones" Pattern from Channel _0. A "Low" level stops the transmission of the "All Ones" Pattern. **Transmit All Ones for Channel _1** **Transmit All Ones for Channel _2** **Transmit All Ones for Channel _3** **Transmit All Ones for Channel _4** **Transmit All Ones for Channel _5** **Transmit All Ones for Channel _6** **Transmit All Ones for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
TAOS_1	B6		
TAOS_2	A5		
TAOS_3	C6		
TAOS_4	T6		
TAOS_5	U6		
TAOS_6	V6		
TAOS_7	R6		
TXON_0	A13	**I**	**Transmitter Turn On for Channel _0** **Hardware mode** Setting this pin "High" turns on the Transmit and Receive Sections of Channel _0. When TXON_0 = "0" then TTIP_0 and TRING_0 driver outputs will be tri-stated. **In Host mode** The TXON_n bits in the channel control registers turn each channel Transmit and Receive section ON or OFF. However, control of the on/off function can be transferred to the **Hardware** pins by setting the TXONCNTL bit (bit 7) to "1" in the register at address hex 0x82. **Transmitter Turn On for Channel _1** **Transmitter Turn On for Channel _2** **Transmitter Turn On for Channel _3** **Transmitter Turn On for Channel _4** **Transmitter Turn On for Channel _5** **Transmitter Turn On for Channel _6** **Transmitter Turn On for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
TXON_1	D12		
TXON_2	C12		
TXON_3	B12		
TXON_4	V13		
TXON_5	U13		
TXON_6	R12		
TXON_7	R13		

MICROPROCESSOR INTERFACE

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
HW_HOST	T10	I	**Mode Control Input** This pin selects **Hardware** or **Host mode**. Leave this pin unconnected or tie "High" to select **Hardware mode**. For **Host mode**, this pin must be tied "Low". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
WR_R/W	D7	I	**Write Input (Read/Write) - Host mode:** **Intel bus timing**: A "Low" pulse on WR selects a write operation when CS pin is "Low". **Motorola bus timing:** A "High" pulse on R/W selects a read operation and a "Low" pulse on R/W selects a write operation when CS is "Low".
EQC0	D7		**Equalizer Control Input pin 0 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
RD_DS	C7	I	**Read Input (Data Strobe) - Host mode** **Intel bus timing:** A "Low" pulse on RD selects a read operation when the CS pin is "Low". **Motorola bus timing:** A "Low" pulse on DS indicates a read or write operation when the CS pin is "Low".
EQC1	C7		**Equalizer Control Input pin 1 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
ALE_AS	A7	I	**Address Latch Input (Address Strobe) - Host mode** **Intel bus timing:** The address inputs are latched into the internal register on the falling edge of ALE. **Motorola bus timing:** The address inputs are latched into the internal register on the falling edge of AS.
EQC2	A7		**Equalizer Control Input pin 2 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
CS	B7	I	**Chip Select Input - Host mode:** This signal must be "Low" in order to access the parallel port.
EQC3	B7		**Equalizer Control Input pin 3 - Hardware mode:** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RDY_DTACK	A6	**O**	**Ready Output (Data Transfer Acknowledge Output) - Host mode** **Intel bus timing**: RDY is asserted "High" to indicate the device has completed a read or write operation. **Motorola bus timing**: $\overline{\text{DTACK}}$ is asserted "Low" to indicate the device has completed a read or write cycle.
EQC4	A6	**I**	**Equalizer Control Input pin 4 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
µPTS1 **µPTS2**	J16 L15	**I**	**Microprocessor Type Select Input Pins - Host Mode:** **Microprocessor Type Select Input Bit 1** **Microprocessor Type Select Input Bit 2** µPTS2 / µPTS1 / µP Type: 0 / 0 / Intel 8051 Asynchronous 0 / 1 / Motorola Asynchronous 1 / 0 / Power PC Synchronous 1 / 1 / MPC8xx Motorola Synchronous
RCLKE	J16		**Receive Clock Edge - Hardware mode** **SEE"RECEIVE CLOCK EDGE - HARDWARE MODE" ON PAGE 7.**
TCLKE	L15		**Transmit Clock Edge - Hardware mode** **SEE"TRANSMIT CLOCK EDGE - HARDWARE MODE" ON PAGE 7.** ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
			Microprocessor Read/Write Data Bus Pins - Host mode
D[7]	T7	**I/O**	**Data Bus[7]**
D[6]	U7		**Data Bus[6]**
D[5]	V7		**Data Bus[5]**
D[4]	V8		**Data Bus[4]**
D[3]	V9		**Data Bus[3]**
D[2]	U8		**Data Bus[2]**
D[1]	U9		**Data Bus[1]**
D[0]/SDO	R7		**Data Bus[0]** if SER_$\overline{\text{PAR}}$ = 0 **or Serial Data Input** if SER_$\overline{\text{PAR}}$ = 1
			Loop-back Control Pins, Bits [1:0] Channel_[7:4] - Hardware Mode
LOOP1_4	T7		Pins 67-74 and 173-180 control which Loop-Back mode is selected per channel. **SEE"LOOP-BACK CONTROL PINS, BITS [1:0] CHANNEL_[7:0]" ON PAGE 17.**
LOOP0_4	U7		
LOOP1_5	V7		
LOOP0_5	V8		***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
LOOP1_6	V9		
LOOP0_6	U8		
LOOP1_7	U9		
LOOP0_7	R7		

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
			Microprocessor Interface Address Bus Pins - Host mode:
A[7]	A12	**I**	**Microprocessor Interface Address Bus[7]**
A[6]	B11		**Microprocessor Interface Address Bus[6]**
A[5]	C11		**Microprocessor Interface Address Bus[5]**
A[4]	D11		**Microprocessor Interface Address Bus[4]**
A[3]	A11		**Microprocessor Interface Address Bus[3]**
A[2]	B10		**Microprocessor Interface Address Bus[2]**
A[1]	A10		**Microprocessor Interface Address Bus[1]**
A[0]/SDI	C10		**Microprocessor Interface Address Bus[0]** if SER_$\overline{\text{PAR}}$ = 0 **or Serial Data Input** if SER_$\overline{\text{PAR}}$ = 1
			Loop-back Control Pins, Bits [1:0] Channel_[3:0]
LOOP1_3	A12		In **Hardware mode**, pins 67-74 and 173-180 control which Loop-Back mode is selected per channel. **SEE"LOOP-BACK CONTROL PINS, BITS [1:0] CHANNEL_[7:0]" ON PAGE 17.**
LOOP0_3	B11		
LOOP1_2	C11		
LOOP0_2	D11		***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
LOOP1_1	A11		
LOOP0_1	B10		
LOOP1_0	A10		
LOOP0_0	C10		
µPCLK/SCLK	T13	**I**	**Microprocessor Clock Input - Host Mode:** **µPCLK -** Input clock for synchronous parrallel microprocessor operation. Maximum clock rate is 54 MHz, SER_$\overline{\text{PAR}}$ = 0 **SCLK** - Input serial clock for SPI interface, SER_$\overline{\text{PAR}}$ = 1 ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor for asynchronous microprocessor interface when no clock is present.*
ATAOS	T13		**Automatic Transmit "All Ones" - Hardware mode** This pin functions as an Automatic Transmit "All Ones". **SEE"AUTOMATIC TRANSMIT "ALL ONES" PATTERN - HARDWARE MODE" ON PAGE 16.**
$\overline{\text{INT}}$	L16	**O**	**Interrupt Output - Host mode** This pin goes "Low" to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to a "0" in the command control register.
TRATIO	L16	**I**	**Transmitter Transformer Ratio Select - Hardware mode** TRATIO is Not Supported in the 83VL38. This pin is for $\overline{\text{INT}}$ only. ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*

JITTER ATTENUATOR

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
JASEL0 JASEL1	A14 B13	I	**Jitter Attenuator Select Pins Hardware Mode** **Jitter Attenuator select Bit 0** **Jitter Attenuator select Bit 1** JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it. **NOTE:** *These pins are internally pulled "Low" with 50kΩ resistors.*

JASEL1	JASEL0	JA PATH
0	0	Disabled
0	1	Transmit Path
1	0	Receive Path
1	1	Rx & Tx Paths

CLOCK SYNTHESIZER

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
MCLKOUT	H1	O	**Synthesized Master Clock Output** This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.
MCLKT1	K1	I	**T1 Master Clock Input** This signal is an independent 1.544MHz clock for T1 systems with accuracy better than ±50ppm and duty cycle within 40% to 60%. MCLKT1 is used in the T1 mode. **NOTES:** 1. *All channels of the XRT83VL38 must be operated at the same clock rate, either T1, E1 or J1.* 2. *See pin 26 description for further explanation for the usage of this pin.* 3. *Internally pulled "Low" with a 50kΩ resistor.*
MCLKE1	J1	I	**E1 Master Clock Input** A 2.048MHz clock for with an accuracy of better than ±50ppm and a duty cycle of 40% to 60% can be provided at this pin. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. **NOTES:** 1. *All channels of the XRT83VL38 must be operated at the same clock rate, either T1, E1 or J1.* 2. *Internally pulled "Low" with a 50kΩ resistor.*

<table>
<tr><th>SIGNAL NAME</th><th>LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>CLKSEL0
CLKSEL1
CLKSEL2</td><td>A8
B8
C8</td><td>I</td><td>Clock Select inputs for Master Clock Synthesizer - Hardware mode
CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the table below.
In Hardware mode, the MCLKRATE control signal is generated from the state of EQC[4:0] inputs.
In Host mode, the state of these pins are ignored and the master frequency PLL is controlled by the corresponding interface bits. See Table 40 register address 10000001
<table>
<tr><th>MCLKE1 kHz</th><th>MCLKT1 kHz</th><th>CLKSEL 2</th><th>CLKSEL1</th><th>CLKSEL0</th><th>MCLKRATE</th><th>CLKOUT kHz</th></tr>
<tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1544</td></tr>
<tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr>
<tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2048</td></tr>
<tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr>
</table>
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
</table>

ALARM FUNCTIONS/REDUNDANCY SUPPORT

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
GAUGE	J18	**I**	**Twisted Pair Cable Wire Gauge Select - Hardware Mode** Connect this pin "High" to select 26 Gauge wire. Connect this pin "Low" to select 22 and 24 gauge wire for all channels. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
DMO_0	D5	**O**	**Driver Failure Monitor Channel _0:** This pin transitions "High" if a short circuit condition is detected in the transmit driver of Channel _0, or no transmit output pulse is detected for more than 128 TCLK_0 cycles.
DMO_1	D4		**Driver Failure Monitor Channel _1**
DMO_2	C15		**Driver Failure Monitor Channel _2**
DMO_3	C13		**Driver Failure Monitor Channel _3**
DMO_4	R5		**Driver Failure Monitor Channel _4**
DMO_5	P4		**Driver Failure Monitor Channel _5**
DMO_6	U17		**Driver Failure Monitor Channel _6**
DMO_7	V14		**Driver Failure Monitor Channel _7**
ATAOS	T13	**I**	**Automatic Transmit "All Ones" Pattern - Hardware Mode** A "High" level on this pin enables the automatic transmission of an "All Ones" AMI pattern from the transmitter of any channel that the receiver of that channel has detected an LOS condition. A "Low" level on this pin disables this function. *Note: All channels share the same ATAOS control function.*
µPCLK/SCLK	T13		**Microprocessor Clock Input - Host mode** **SEE"MICROPROCESSOR CLOCK INPUT - HOST MODE:" ON PAGE 13.** ***NOTE:*** *This pin is internally pulled "Low" for asynchronous microprocessor interface when no clock is present.*
TRATIO	L16	**I**	**Transmitter Transformer Ratio Select - Hardware mode** TRATIO is Not Supported in the 83VL38. This pin is for $\overline{INT}$ only..
$\overline{INT}$	L16	**O**	**Interrupt Output - Host mode** This pin is asserted "Low" to indicate an alarm condition. **SEE"INTERRUPT OUTPUT - HOST MODE" ON PAGE 13.** ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*
$\overline{RESET}$	T8	**I**	**Hardware Reset (Active "Low"):** When this pin is tied "Low" for more than 10µs, the device is put in the reset state. **Exar recommends initiating a Harware reset upon power up.** ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor.*
SR/$\overline{DR}$	K4	**I**	**Single-Rail/Dual-Rail Data Format:** Connect this pin "Low" to select transmit and receive data format in **Dual-Rail mode**. In this mode, HDB3 or B8ZS encoder and decoder are not available. Connect this pin "High" to select **single-rail data format**. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

<table>
<tr><th>SIGNAL NAME</th><th>LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td></td><td></td><td></td><td>Loop-back Control Pins, Bits [1:0] Channel_[7:0]</td></tr>
<tr><td>LOOP1_0</td><td>A10</td><td>I</td><td>Loop-back Control bit 1, Channel _0</td></tr>
<tr><td>LOOP0_0</td><td>C10</td><td></td><td>Loop-back Control bit 0, Channel _0</td></tr>
<tr><td>LOOP1_1</td><td>A11</td><td></td><td>Loop-back Control bit 1, Channel _1</td></tr>
<tr><td>LOOP0_1</td><td>B10</td><td></td><td>Loop-back Control bit 0, Channel _1</td></tr>
<tr><td>LOOP1_2</td><td>C11</td><td></td><td>Loop-back Control bit 1, Channel _2</td></tr>
<tr><td>LOOP0_2</td><td>D11</td><td></td><td>Loop-back Control bit 0, Channel _2</td></tr>
<tr><td>LOOP1_3</td><td>A12</td><td></td><td>Loop-back Control bit 1, Channel _3</td></tr>
<tr><td>LOOP0_3</td><td>B11</td><td></td><td>Loop-back Control bit 0, Channel _3</td></tr>
<tr><td>LOOP1_4</td><td>T7</td><td></td><td>Loop-back Control bit 1, Channel _4</td></tr>
<tr><td>LOOP0_4</td><td>U7</td><td></td><td>Loop-back Control bit 0, Channel _4</td></tr>
<tr><td>LOOP1_5</td><td>V7</td><td></td><td>Loop-back Control bit 1, Channel _5</td></tr>
<tr><td>LOOP0_5</td><td>V8</td><td></td><td>Loop-back Control bit 0, Channel _5</td></tr>
<tr><td>LOOP1_6</td><td>V9</td><td></td><td>Loop-back Control bit 1, Channel _6</td></tr>
<tr><td>LOOP0_6</td><td>U8</td><td></td><td>Loop-back Control bit 0, Channel _6</td></tr>
<tr><td>LOOP1_7</td><td>U9</td><td></td><td>Loop-back Control bit 1, Channel _7</td></tr>
<tr><td>LOOP0_7</td><td>R7</td><td></td><td>Loop-back Control bit 0, Channel _7
In Hardware mode, these pins control the Loop-Back mode for each channel_n per the following table.
<table>
<tr><th>LOOP1_n</th><th>LOOP0_n</th><th>MODE</th></tr>
<tr><td>0</td><td>0</td><td>Normal Mode No Loop-Back Channel_n</td></tr>
<tr><td>0</td><td>1</td><td>Local Loop-Back Channel_n</td></tr>
<tr><td>1</td><td>0</td><td>Remote Loop-Back Channel_n</td></tr>
<tr><td>1</td><td>1</td><td>Digital Loop-Back Channel_n</td></tr>
</table></td></tr>
<tr><td>A[1]</td><td>A10</td><td></td><td rowspan="17">Microprocessor Address A[7:0] and Data Bus Pins D[7:0] - Host mode
These pins are microprocessor address and data bus pins. SEE”MICROPROCESSOR INTERFACE ADDRESS BUS PINS - HOST MODE:” ON PAGE 13. and see “Microprocessor Read/Write Data Bus Pins - Host mode” on page 12.
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>A[0]/SDI</td><td>C10</td><td></td></tr>
<tr><td>A[3]</td><td>A11</td><td></td></tr>
<tr><td>A[2]</td><td>B10</td><td></td></tr>
<tr><td>A[5]</td><td>C11</td><td></td></tr>
<tr><td>A[4]</td><td>D11</td><td></td></tr>
<tr><td>A[7]</td><td>A12</td><td></td></tr>
<tr><td>A[6]</td><td>B11</td><td></td></tr>
<tr><td>D[7]</td><td>T7</td><td></td></tr>
<tr><td>D[6]</td><td>U7</td><td></td></tr>
<tr><td>D[5]</td><td>V7</td><td></td></tr>
<tr><td>D[4]</td><td>V8</td><td></td></tr>
<tr><td>D[3]</td><td>V9</td><td></td></tr>
<tr><td>D[2]</td><td>U8</td><td></td></tr>
<tr><td>D[1]</td><td>U9</td><td></td></tr>
<tr><td>D[0]/SDO</td><td>R7</td><td></td></tr>
</table>

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
EQC4	A6	**I**	**Equalizer Control Input 4 - Hardware mode** This pin together with pins EQC[3:0] is used to control the transmit pulse shaping, transmit line build-out (LBO) and receive monitoring while operating at one of either the T1, E1 or J1 clock rates/modes. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31.** for description of Transmit Equalizer Control bits. **Equalizer Control Input 3** **Equalizer Control Input 2** **Equalizer Control Input 1** **Equalizer Control Input 0** ***NOTES:*** 1. *In **Hardware mode** all transmit channels share the same pulse setting controls function.* 2. *All channels of an XRT83VL38 must operate at the same clock rate, either the T1, E1 or J1 modes.*
EQC3	B7	**I**	
EQC2	A7	**I**	
EQC1	C7	**I**	
EQC0	D7	**I**	
$\overline{RDY}$_$\overline{DTACK}$	A6	**O**	In **Host mode**, these pins perform various microprocessor functions. **SEE"MICRO-PROCESSOR INTERFACE" ON PAGE 11.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{CS}$	B7	**I**	
ALE_$\overline{AS}$	A7	**I**	
$\overline{RD}$_$\overline{DS}$	C7	**I**	
$\overline{WR}$_R/$\overline{W}$	D7	**I**	
RXTSEL	U11	**I**	**Receiver Termination Select** In **Hardware mode**, when this pin is "Low" the receive line termination is determined only by an external resistor. When "High", the receive termination is realized by the internal resistor or the combination of internal and external resistors. These conditions are described in the table below. ***NOTE:*** *In **Hardware mode** all channels share the same RXTSEL control function.* **RXTSEL / RX Termination** **0 / External** **1 / Internal** In **Host mode**, the RXTSEL_n bits in the channel control registers determine if the receiver termination is external or internal. However, the function of RXTSEL can be transferred to the **Hardware** pin by setting the TERCNTL bit (bit 6) to "1" in the register address hex 0x82. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TXTSEL	V11	**I**	**Transmit Termination Select - Hardware Mode** When this pin is "Low" the transmit line termination is determined only by an external resistor. When "High", the transmit termination is realized only by the internal resistor. **TXTSEL / TX Termination** **0 / External** **1 / Internal** ***NOTES:*** 1. *This part does not support external termination in E1 operation.* 2. *This pin is internally pulled "Low" with a 50kΩ resistor.* 3. *In **Hardware mode** all channels share the same **TXTSEL** control function.*

<table>
<tr><th>SIGNAL NAME</th><th>LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>TERSEL1
TERSEL0</td><td>T11
R11</td><td>I</td><td>Termination Impedance Select bit 1:
Termination Impedance Select bit 0:
In the Hardware mode and in the internal termination mode (TXTSEL="1" and RXTSEL="1") TERSEL[1:0] control the transmit and receive termination impedance according to the following table.
<table><tr><th>TERSEL1</th><th>TERSEL0</th><th>Termination</th></tr><tr><td>0</td><td>0</td><td>100Ω</td></tr><tr><td>0</td><td>1</td><td>110Ω</td></tr><tr><td>1</td><td>0</td><td>75Ω</td></tr><tr><td>1</td><td>1</td><td>120Ω</td></tr></table>
In the internal termination mode the receiver termination of each receiver is realized completely by internal resistors or by the combination of internal and one fixed external resistor (see description of RXRES[1:0] pins).
In the internal termination mode the transformer ratio of 1:2 and 1:1 is required for transmitter and receiver respectively with the transmitter output AC coupled to the transformer.
NOTES:
1. This pin is internally pulled "Low" with a 50kΩ resistor.
2. In Hardware mode, all channels share the same TERSEL control function.
3. In the external termination mode a 1:2 transformer ratio must be used for the transmitter.</td></tr>
<tr><td>TEST</td><td>U12</td><td>I</td><td>Manufacturing Test:
NOTE: For normal operation this pin must be tied to ground.</td></tr>
<tr><td>$\overline{\text{ICT}}$</td><td>V12</td><td>I</td><td>In-Circuit Testing (Active "Low"):
When this pin is tied "Low", all output pins are forced to a high impedance state for in-circuit testing.
Pulling $\overline{\text{RESET}}$ and $\overline{\text{ICT}}$ pins "Low" simultaneously will put the chip in factory test mode. This condition should not be permitted during normal operation.
NOTE: This pin is internally pulled "High" with a 50kΩ resistor.</td></tr>
</table>

SERIAL MICROPROCESSOR INTERFACE

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
SER_$\overline{PAR}$	P18	I	**Serial/Parallel Select Input (Host Mode Only)** This pin is used in the Host mode to select between the parallel microprocessor or serial interface. By default, the Host mode operates in the parallel microprocessor mode. To configure the device for a serial interface, this pin must be pulled "HIgh". ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
SCLK	T13	I	**Serial Clock Input (Host Mode Only)** If Pin SER_$\overline{PAR}$ is pulled "High", this input pin is used the timing reference for the serial microprocessor interface. See the Microprocessor Section of this datasheet for details.
SDI	C10	I	**Serial Data Input (Host Mode Only)** If Pin SER_$\overline{PAR}$ is pulled "High", this input pin from the serial interface is used to input the serial data for Read and Write operations. See the Microprocessor Section of this datasheet for details.
SDO	R7	O	**Serial Data Output (Host Mode Only)** If Pin SER_$\overline{PAR}$ is pulled "High", this output pin from the serial interface is used to read back the regsiter contents. See the Microprocessor Section of this datasheet for details.
TDO	B1		**Test Data Out** This pin is used as the output data pin for the boundary scan chain.
TDI	R1		**Test Data In** This pin is used as the input data pin for the boundary scan chain. For normal operation, this pin should be pulled "High". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
TCK	N1		**Test Clock Input** This pin is used as the input clock source for the boundary scan chain. For normal operation, this pin should be pulled "High". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
TMS	E1		**Test Mode Select** This pin is used as the input mode select for the boundary scan chain. For normal operation, this pin should be pulled "High". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
SENSE	N18	O	**Factory Test Pin** This pin shpould be left floating.

POWER AND GROUND

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TGND_0 **TGND_1** **TGND_2** **TGND_3** **TGND_4** **TGND_5** **TGND_6** **TGND_7**	D3 F2 E15 C17 R3 P3 T16 R16	****	**Transmitter Analog Ground for Channel _0** It is recomended that all ground pins form this device be tied together.
TVDD_0 **TVDD_1** **TVDD_2** **TVDD_3** **TVDD_4** **TVDD_5** **TVDD_6** **TVDD_7**	E4 F4 F16 E17 R4 P1 N15 P15	****	**Transmitter Analog Power Supply (3.3V ± 5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog supply RVDD. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Each power supply pin should be bypassed to ground with an external 0.1uf capcitor.
RVDD_0 **RVDD_1** **RVDD_2** **RVDD_3** **RVDD_4** **RVDD_5** **RVDD_6** **RVDD_7**	C2 E5 G16 D16 V2 N3 N17 U18	****	**Receiver Analog Positive Supply (3.3V± 5%)** RVDD should not be shared with any other supply. It is recommended that RVDD be isolated from the digital supply DVDD and the analog power supply TVDD. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Each power supply pin should be bypassed to ground with an external 0.1uf capcitor.
RGND_0 **RGND_1** **RGND_2** **RGND_3** **RGND_4** **RGND_5** **RGND_6** **RGND_7**	D2 G3 G17 D17 T2 M2 M17 R17	****	**Receiver Analog Ground for Channel_0** It is recomended that all ground pins form this device be tied together.
AVDD	K17 J3 J2	****	**Analog Positive Supply (1.8V± 5%)** AVDD should be isolated from other supplies. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Each power supply pin should be bypassed to ground with at least one 0.1uf capcitor
AGND	J17 K3 L4	****	**Analog Ground** It is recomended that all ground pins form this device be tied together.
DVDD1v8	U10 K18 D10 A9 V1		**Digital Positive Supply (1.8V± 5%)** DVDD1v8 should be isolated from other analog supplies. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Every two DVDD1v8 power supply pins should be bypassed to ground with at least one 0.1uf capcitor