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GENERAL DESCRIPTION

The XRT83VSH314 is a fully integrated 14-channel short-haul line interface unit (LIU) that operates from a 1.8V Inner Core and 3.3V I/O power supplies. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode independently on a per channel basis with minimum external components. The LIU features are programmed through a standard microprocessor interface. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

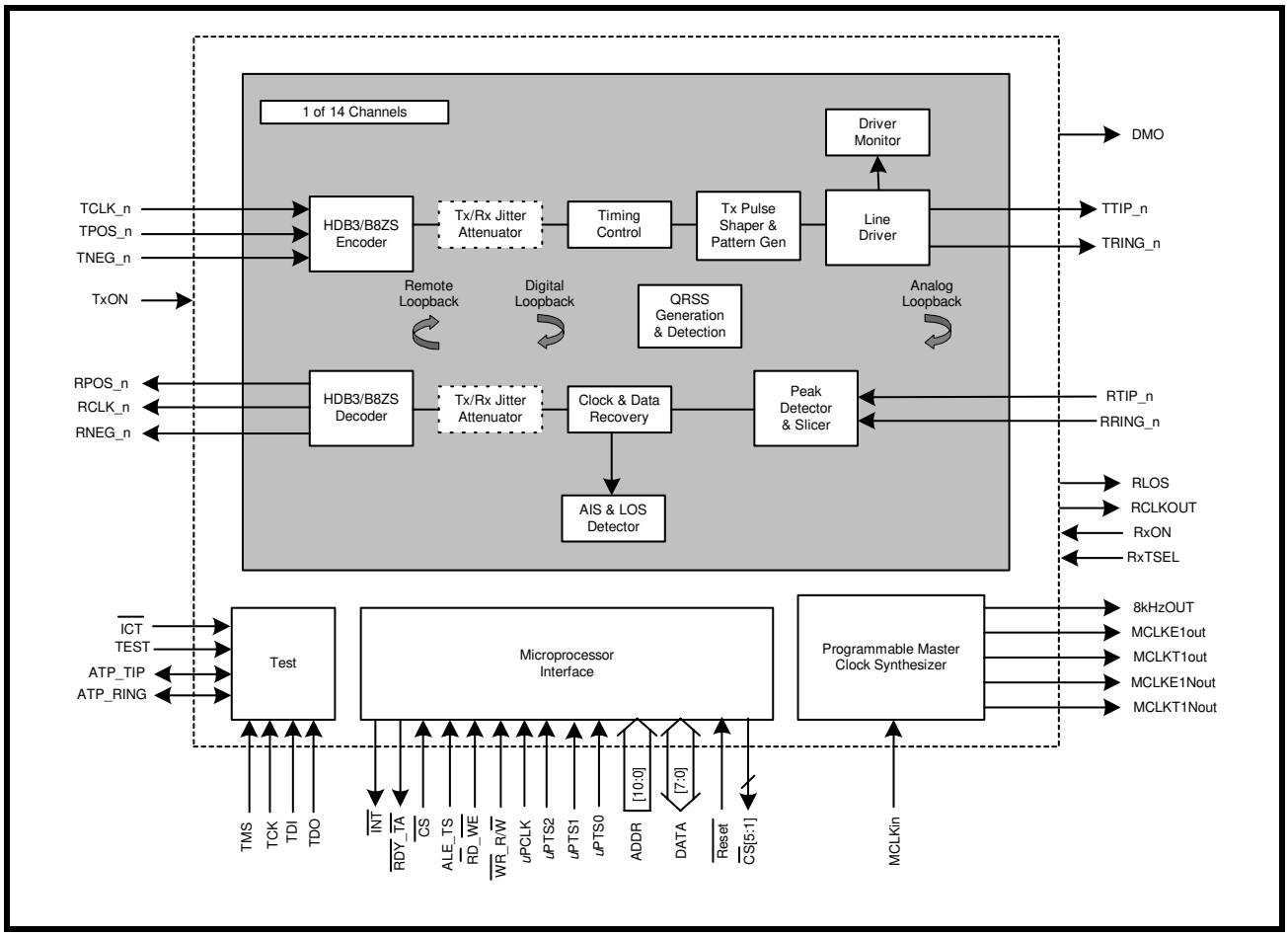
The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and has five output clock references that can be used for external timing (8kHz, 1.544Mhz, 2.048Mhz, nxT1/J1, nxE1).

Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS/PRBS generation/detection, TAOS, DMO, and diagnostic loopback modes.

APPLICATIONS

- T1 Digital Cross Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA)
- Wireless Base Stations

FIGURE 1. BLOCK DIAGRAM OF THE XRT83VSH314



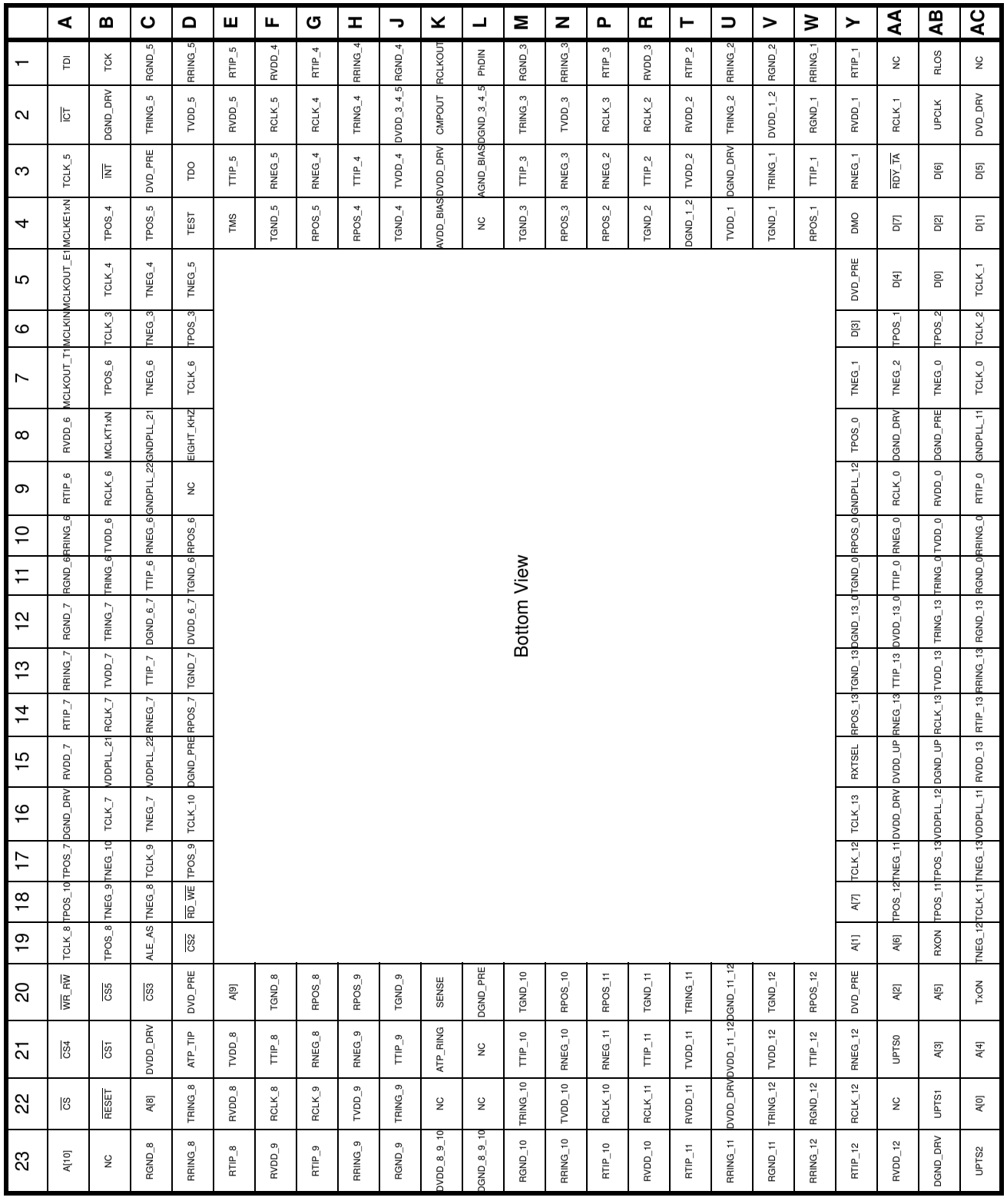
FEATURES

- Fully integrated 14-Channel short haul transceivers for T1/J1 (1.544MHz) and E1 (2.048MHz) applications
- T1/E1/J1 short haul and clock rate are per port selectable through software without changing components
- Internal Impedance matching on both receive and transmit for 75Ω (E1), 100Ω (T1), 110Ω (J1), and 120Ω (E1) applications are per port selectable through software without changing components
- Power down on a per channel basis with independent receive and transmit selection
- Five pre-programmed transmit pulse settings for T1 short haul applications per channel
- User programable Arbitrary Pulse mode
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis
- Selectable Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit path
- Driver failure monitor output (DMO) alerts of possible system or external component problems
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis
- Support for automatic protection switching
- 1:1 and 1+1 protection without relays
- Receive monitor mode handles 0 to 6dB resistive attenuation (flat loss) along with 0 to 6dB cable loss for both T1 and E1
- Loss of signal (RLOS) according to ITU-T G.775/ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Programmable data stream muting upon RLOS detection
- On-Chip HDB3/B8ZS encoder/decoder with an internal 16-bit LCV counter for each channel
- On-Chip digital clock recovery circuit for high input jitter tolerance
- QRSS/PRBS pattern generator and detection for testing and monitoring
- Error and bipolar violation insertion and detection
- Transmit all ones (TAOS) Generators and Detectors
- Supports local analog, remote, digital, and dual loopback modes
- 1.8V Digital Core
- 3.3V I/O and Analog Core
- 304-Pin BGA package
- -40°C to +85°C Temperature Range
- Supports gapped clocks for mapper/multiplexer applications

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83VSH314IB	304 Lead PBGA	-40°C to +85°C

PIN OUT OF THE XRT83VSH314



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1.0 PIN DESCRIPTIONS

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
$\overline{CS}$	A22	I	**Chip Select Input** Active low signal. This signal enables the microprocessor interface by pulling chip select "Low". The microprocessor interface is disabled when the chip select signal returns "High". ***NOTE:*** *Internally pulled "High" with a 50k Ω resistor.*
ALE_TS	C19	I	**Address Latch Enable Input (Transfer Start)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{WR}$_R/$\overline{W}$	A20	I	**Write Strobe Input (Read/Write)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{RD}$_$\overline{WE}$	D18	I	**Read Strobe Input (Write Enable)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{RDY}$_$\overline{TA}$	AA3	O	**Ready Output (Transfer Acknowledge)** See the Microprocessor section of this datasheet for a description.
$\overline{INT}$	B3	O	**Interrupt Output** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTE:*** *This pin is an open-drain output that requires an external 10KΩ pull-up resistor.*
µPCLK	AB2	I	**Micro Processor Clock Input** In a synchronous microprocessor interface, µPCLK is used as the internal timing reference for programming the LIU. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
ADDR10 ADDR9 ADDR8 ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0	A23 E20 C22 Y18 AA19 AB20 AC21 AB21 AA20 Y19 AC22	I	**Address Bus Input** ADDR[10:8] is used as a chip select decoder. The LIU has 5 chip select output pins for enabling up to 5 additional devices for accessing internal registers. The LIU has the option to select itself (master device), up to 5 additional devices, or all 6 devices simultaneously by setting the ADDR[10:8] pins specified below. ADDR[7:0] is a direct address bus for permitting access to the internal registers. **ADDR[10:8]** 000 = Master Device 001 = Chip Select Output 1 (Pin B21) 010 = Chip Select Output 2 (Pin D19) 011 = Chip Select Output 3 (Pin C20) 100 = Chip Select Output 4 (Pin A21) 101 = Chip Select Output 5 (Pin B20) 110 = Reserved 111 = All Chip Selects Active Including the Master Device ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0	AA4 AB3 AC3 AA5 Y6 AB4 AC4 AB5	I/O	**Bi-directional Data Bus** DATA[7:0] is a bi-directional data bus used for read and write operations. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
µPTS2 µPTS1 µPTS0	AC23 AB22 AA21	I	**Microprocessor Type Select Input** µPTS[2:0] are used to select the microprocessor type interface. 000 = Intel 68HC11, 8051, 80C188 (Asynchronous) 001 = Motorola 68K (Asynchronous) 111 = Motorola MPC8260, MPC860 Power PC (Synchronous) ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{\text{Reset}}$	B22	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
$\overline{\text{CS5}}$ $\overline{\text{CS4}}$ $\overline{\text{CS3}}$ $\overline{\text{CS2}}$ $\overline{\text{CS1}}$	B20 A21 C20 D19 B21	O	**Chip Select Output** The XRT83VSH314 can be used to provide the necessary chip selects for up to 5 additional devices by using the 3 MSBs ADDR[10:8] from the 11-Bit address bus. The LIU allows up to 84-channel applications with only using one chip select. See the ADDR[10:0] definition in the pin description.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RxON	AB19	I	**Receive On/Off Input** Upon power up, the receivers are powered off. Turning the receivers On or Off can be selected through the microprocessor interface by programming the appropriate channel register if the hardware pin is pulled "High". If the hardware pin is pulled "Low", all channels are automatically turned off. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
RxTSEL	Y15	I	**Receive Termination Control** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register. Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.* **RxTSEL (pin)** / **Rx Termination** 0 / External 1 / Internal *Note: RxTCNTL (bit) must be set to "1"*
RLOS	AB1	O	**Receive Loss of Signal (Global Pin for All 14-Channels)** When a receive loss of signal occurs for any one of the 14-channels according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel RLOS, see the register map.*
RCLK13 RCLK12 RCLK11 RCLK10 RCLK9 RCLK8 RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	AB14 Y22 R22 P22 G22 F22 B14 B9 F2 G2 P2 R2 AA2 AA9	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RxON is pulled "Low", RCLK maintains its timing by using an internal master clock as its reference. Software control (RCLKE) allows RPOS/RNEG data to be updated on either edge of RCLK. ***NOTE:*** *RCLKE is a global setting that applies to all 14 channels.*

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RCLKOUT	K1	O	**Recovered Clock Output:** One of the 14 RCLKS is selected with the Recoved Clock Select [3:0] (register 0xEEh) bits and output through this pin. See table below.
RPOS13 RPOS12 RPOS11 RPOS10 RPOS9 RPOS8 RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	Y14 W20 P20 N20 H20 G20 D14 D10 G4 H4 N4 P4 W4 Y10	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.

Recovered Clock Select[3:0]	Selected RCLK[13:0]
0000, 1111	No RCLK Selected
0001	RCLK 0
0010	RCLK 1
0011	RCLK 2
0100	RCLK 3
0101	RCLK 4
0110	RCLK 5
0111	RCLK 6
1000	RCLK 7
1001	RCLK 8
1010	RCLK 9
1011	RCLK 10
1100	RCLK 11
1101	RCLK 12
1110	RCLK 13

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RNEG13 RNEG12 RNEG11 RNEG10 RNEG9 RNEG8 RNEG7 RNEG6 RNEG5 RNEG4 RNEG3 RNEG2 RNEG1 RNEG0	AA14 Y21 P21 N21 H21 G21 C14 C10 F3 G3 N3 P3 Y3 AA10	O	**RNEG/LCV_OF Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin can either be a Line Code Violation or Overflow indicator. If LCV is selected by software and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. However, if OF is selected the LCV pin will pull "High" if the internal LCV counter is saturated. The LCV pin will remain "High" until the LCV counter is reset.
RTIP13 RTIP12 RTIP11 RTIP10 RTIP9 RTIP8 RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	AC14 Y23 T23 P23 G23 E23 A14 A9 E1 G1 P1 T1 Y1 AC9	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING13 RRING12 RRING11 RRING10 RRING9 RRING8 RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	AC13 W23 U23 N23 H23 D23 A13 A10 D1 H1 N1 U1 W1 AC10	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TxON	AC20	I	**Transmit On/Off Input** Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 14 transmitters are powered off. ***NOTES:*** *1. TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details.* *2. Internally pulled "Low" with a 50KΩ resistor.*
DMO	Y4	O	**Digital Monitor Output (Global Pin for All 14-Channels)** When no transmit output pulse is detected for more than 128 TCLK cycles on one of the 14-channels, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel DMO, see the register map.*
TCLK13 TCLK12 TCLK11 TCLK10 TCLK9 TCLK8 TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	Y16 Y17 AC18 D16 C17 A19 B16 D7 A3 B5 B6 AC6 AC5 AC7	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING can be selected to send an all ones or an all zero signal by programming TCLKCNL. In addition, software control (TCLKE) allows TPOS/TNEG data to be sampled on either edge of TCLK. ***NOTES:*** *1. TCLKE is a global setting that applies to all 14 channels.* *2. Internally pulled "Low" with a 50k Ω resistor.*
TPOS13 TPOS12 TPOS11 TPOS10 TPOS9 TPOS8 TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	AB17 AA18 AB18 A18 D17 B19 A17 B7 C4 B4 D6 AB6 AA6 Y8	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TNEG13 TNEG12 TNEG11 TNEG10 TNEG9 TNEG8 TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	AC17 AC19 AA17 B17 B18 C18 C16 C7 D5 C5 C6 AA7 Y7 AB7	I	**Transmit Negative Data Input** In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
TTIP13 TTIP12 TTIP11 TTIP10 TTIP9 TTIP8 TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	AA13 W21 R21 M21 J21 F21 C13 C11 E3 H3 M3 R3 W3 AA11	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING13 TRING12 TRING11 TRING10 TRING9 TRING8 TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	AB12 V22 T20 M22 J22 D22 B12 B11 C2 H2 M2 U2 V3 AB11	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.

CONTROL FUNCTION

NAME	PIN	TYPE	DESCRIPTION
TEST	D4	I	**Factory Test Mode** For normal operation, the TEST pin should be tied to ground. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{ICT}$	A2	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
PhDIN	L1	I	**Test Pin** For testing purposes only. For normal operation leave this pin unconnected. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
CMPOUT	K2	O	**Test Pin** For testing purposes only. For normal operation leave this pin unconnected.

CLOCK SECTION

NAME	PIN	TYPE	DESCRIPTION
MCLKin	A6	I	**Master Clock Input** The master clock input can accept a wide range of inputs that can be used to generate T1 or E1 clock rates on a per channel basis. See the register map for details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
8kHzOUT	D8	O	**8kHz Output Clock**
MCLKE1out	A5	O	**2.048MHz Output Clock**
MCLKE1Nout	A4	O	**2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz Output Clock** See the register map for programming details.
MCLKT1out	A7	O	**1.544MHz Output Clock**
MCLKT1Nout	B8	O	**1.544MHz, 3.088MHz, 6.176MHz, or 12.352MHz Output Clock** See the register map for programming details.

JTAG SECTION

NAME	PIN	TYPE	DESCRIPTION
ATP_TIP ATP_RING	D21 K21	I/O	**Analog Test Pin_TIP** **Analog Test Pin_RING** These pins are used to check continuity of the Transmit and Receive TIP and RING connections on the assembled board. ***NOTE:*** *See* "Section 5.7, Analog Board Continuity Check" on page 39 *for more detailed description.*
TMS	E4	I	**Test Mode Select** This pin is used as the input mode select for the boundary scan chain. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
TCK	B1	I	**Test Clock Input** This pin is used as the input clock source for the boundary scan chain. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
TDI	A1	I	**Test Data In** This pin is used as the input data pin for the boundary scan chain. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
TDO	D3	O	**Test Data Out** This pin is used as the output data pin for the boundary scan chain.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
TVDD13 TVDD12 TVDD11 TVDD10 TVDD9 TVDD8 TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0	AB13 V21 T21 N22 H22 E21 B13 B10 D2 J3 N2 T3 U4 AB10	PWR	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.
RVDD13 RVDD12 RVDD11 RVDD10 RVDD9 RVDD8 RVDD7 RVDD6 RVDD5 RVDD4 RVDD3 RVDD2 RVDD1 RVDD0	AC15 AA23 T22 R23 F23 E22 A15 A8 E2 F1 R1 T2 Y2 AB9	PWR	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.
DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV	AC2 K3 U22 C21 AA16	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1µF capacitor.
DVDD_PRE DVDD_PRE DVDD_PRE DVDD_PRE DVDD DVDD DVDD DVDD DVDD DVDD DVDD_µP	Y5 C3 D20 Y20 J2 V2 D12 AA12 U21 K23 AA15	PWR	**Digital Power Supply (1.8V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1µF capacitor.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
AVDD_BIAS AVDD_PLL22 AVDD_PLL21 AVDD_PLL12 AVDD_PLL11	K4 C15 B15 AB16 AC16	PWR	**Analog Power Supply (1.8V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
TGND13 TGND12 TGND11 TGND10 TGND9 TGND8 TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	Y13 V20 R20 M20 J20 F20 D13 D11 F4 J4 M4 R4 V4 Y11	GND	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
RGND13 RGND12 RGND11 RGND10 RGND9 RGND8 RGND7 RGND6 RGND5 RGND4 RGND3 RGND2 RGND1 RGND0	AC12 W22 V23 M23 J23 C23 A12 A11 C1 J1 M1 V1 W2 AC11	GND	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND DGND DGND DGND DGND DGND	L2 T4 C12 Y12 U20 L23	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
DGND_DRV DGND_DRV DGND_DRV DGND_DRV DGND_DRV DGND_PRE DGND_PRE DGND_PRE DGND_UP	B2 U3 A16 AA8 AB23 D15 AB8 L20 AB15	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.
AGND_BIAS AGND_PLL22 AGND_PLL21 AGND_PLL12 AGND_PLL11	L3 C9 C8 Y9 AC8	GND	**Analog Ground** It's recommended that all ground pins of this device be tied together.

NO CONNECTS

NAME	PIN	TYPE	DESCRIPTION
NC NC NC NC NC NC NC NC NC NC	AA1 AC1 K20 K22 L22 AA22 B23 L4 L21 D9	NC	**No Connect** These pins can be left floating or tied to ground.

2.0 CLOCK SYNTHESIZER

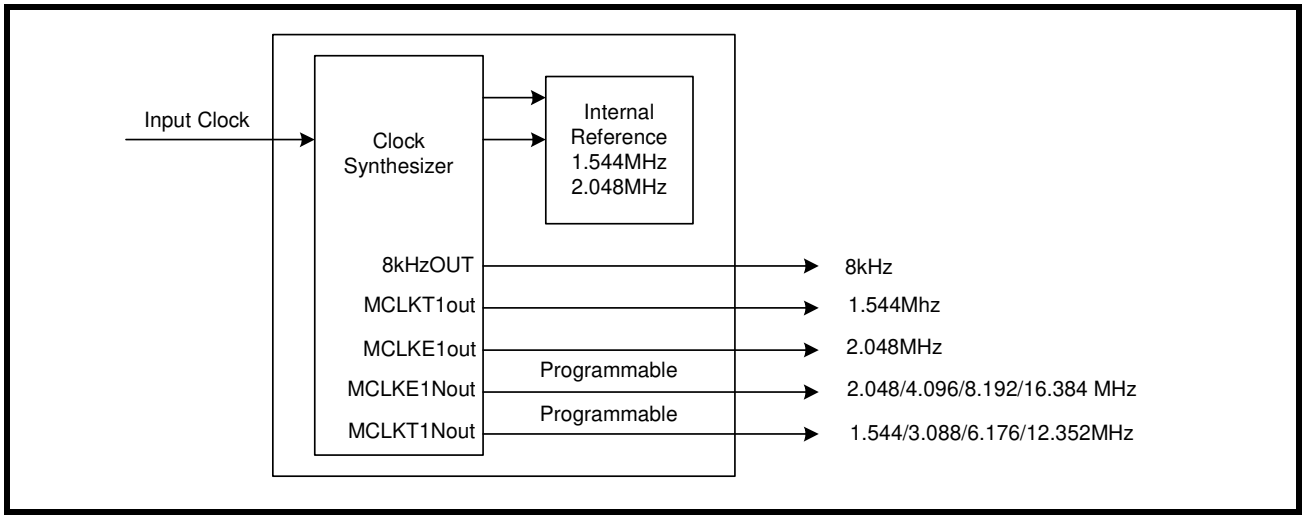
In system design, fewer clocks on the network card could reduce noise and interference. Network cards that support both T1 and E1 modes must be able to produce 1.544MHz and 2.048MHz transmission data. The XRT83VSH314 has a built in clock synthesizer that requires only one input clock reference by programming CLKSEL[3:0] in the appropriate global register. A list of the input clock options is shown in Table 1.

TABLE 1: INPUT CLOCK SOURCE SELECT

CLKSEL[3:0]	INPUT CLOCK REFERENCE
0h (0000)	2.048 MHz
1h (0001)	1.544MHz
8h (1000)	4.096 MHz
9h (1001)	3.088 MHz
Ah (1010)	8.192 MHz
Bh (1011)	6.176 MHz
Ch (1100)	16.384 MHz
Dh (1101)	12.352 MHz
Eh (1110)	2.048 MHz
Fh (1111)	1.544 MHz

The single input clock reference is used to generate multiple timing references. The first objective of the clock synthesizer is to generate 1.544MHz and 2.048MHz for each of the 14 channels. This allows each channel to operate in either T1 or E1 mode independent from the other channels. The state of the equalizer control bits in the appropriate channel registers determine whether the LIU operates in T1 or E1 mode. The second objective is to generate additional output clock references for system use. The available output clock references are shown in Figure 2.

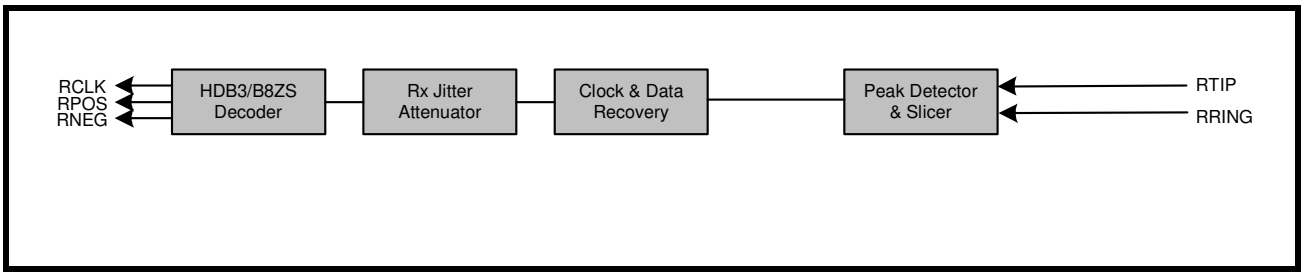
FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE CLOCK SYNTHESIZER



3.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83VSH314 LIU consists of 14 independent T1/E1/J1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in Figure 3.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



3.1 Line Termination (RTIP/RRING)

3.1.1 Internal Termination

The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance (along with the transmit impedance) is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 2.

TABLE 2: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT83VSH314 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See Figure 4 for a typical connection diagram using the internal termination.

FIGURE 4. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION

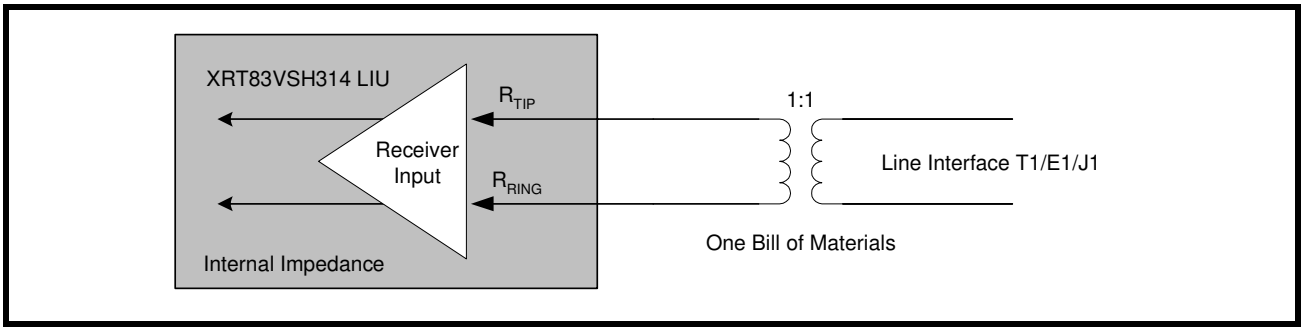


TABLE 3: RECEIVE TERMINATIONS

RXTSEL	TERSEL1	TERSEL0	RXRES1	RXRES0	R_{ext}	R_{int}	MODE
0	x	x	x	x	R_{ext}	∞	T1/E1/J1
1	0	0	0	0	∞	100Ω	T1
1	0	1	0	0	∞	110Ω	J1
1	1	0	0	0	∞	75Ω	E1
1	1	1	0	0	∞	120Ω	E1
1	0	0	0	1	240Ω	172Ω	T1
1	0	1	0	1	240Ω	204Ω	J1
1	1	0	0	1	240Ω	108Ω	E1
1	1	1	0	1	240Ω	240Ω	E1
1	0	0	1	0	210Ω	192Ω	T1
1	0	1	1	0	210Ω	232Ω	J1
1	1	0	1	0	210Ω	116Ω	E1
1	1	1	1	0	210Ω	280Ω	E1
1	0	0	1	1	150Ω	300Ω	T1
1	0	1	1	1	150Ω	412Ω	J1
1	1	0	1	1	150Ω	150Ω	E1
1	1	1	1	1	150Ω	600Ω	E1

3.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1/J1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. Figure 5 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 6 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 4.

FIGURE 5. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

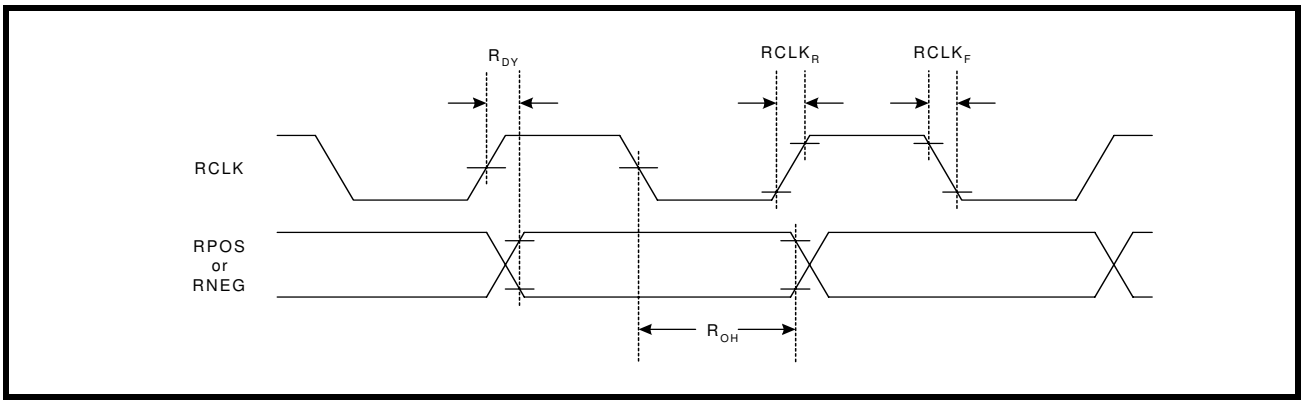


FIGURE 6. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

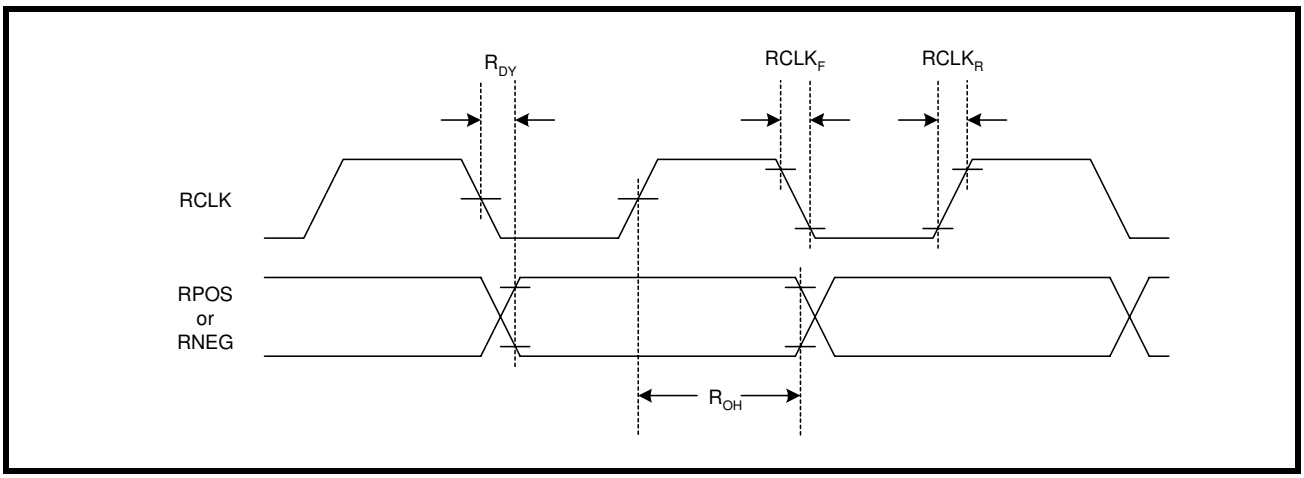


TABLE 4: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

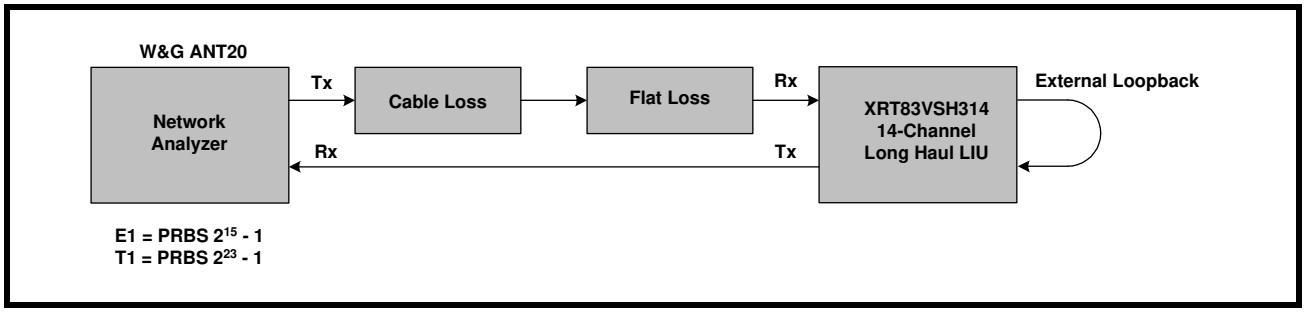
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-	-	ns
Receive Data Hold Time	R_{HO}	150	-	-	ns
RCLK to Data Delay	R_{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, VDDc=1.8V ±5%, T_A=25°C, Unless Otherwise Specified*

3.2.1 Receive Sensitivity

To meet short haul requirements, the XRT83VSH314 can accept T1/E1/J1 signals that have been attenuated by 6dB of cable loss plus 6db of flat loss . Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in Figure 7.

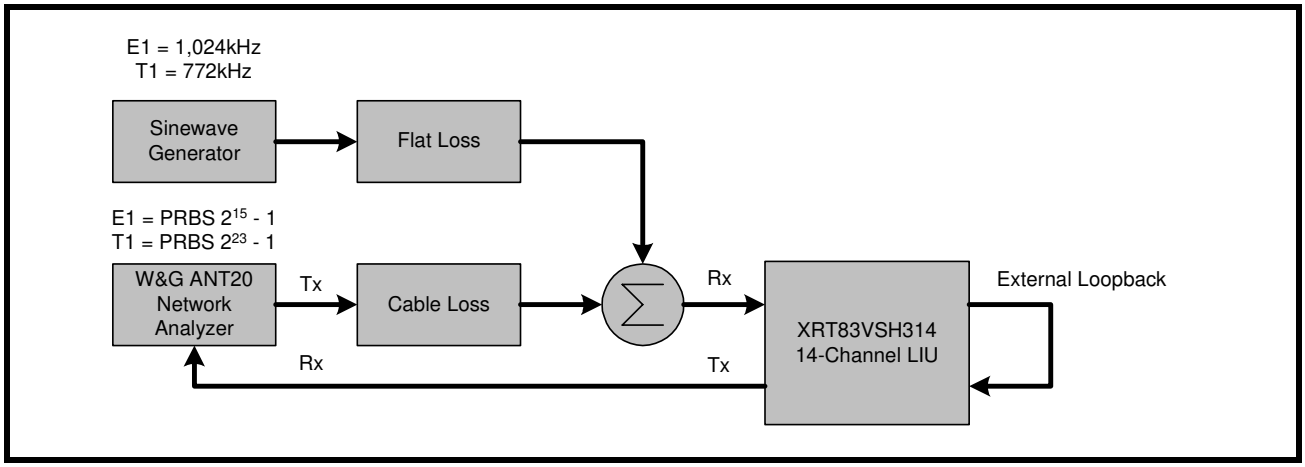
FIGURE 7. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



3.2.2 Interference Margin

The test configuration for measuring the interference margin is shown in Figure 8.

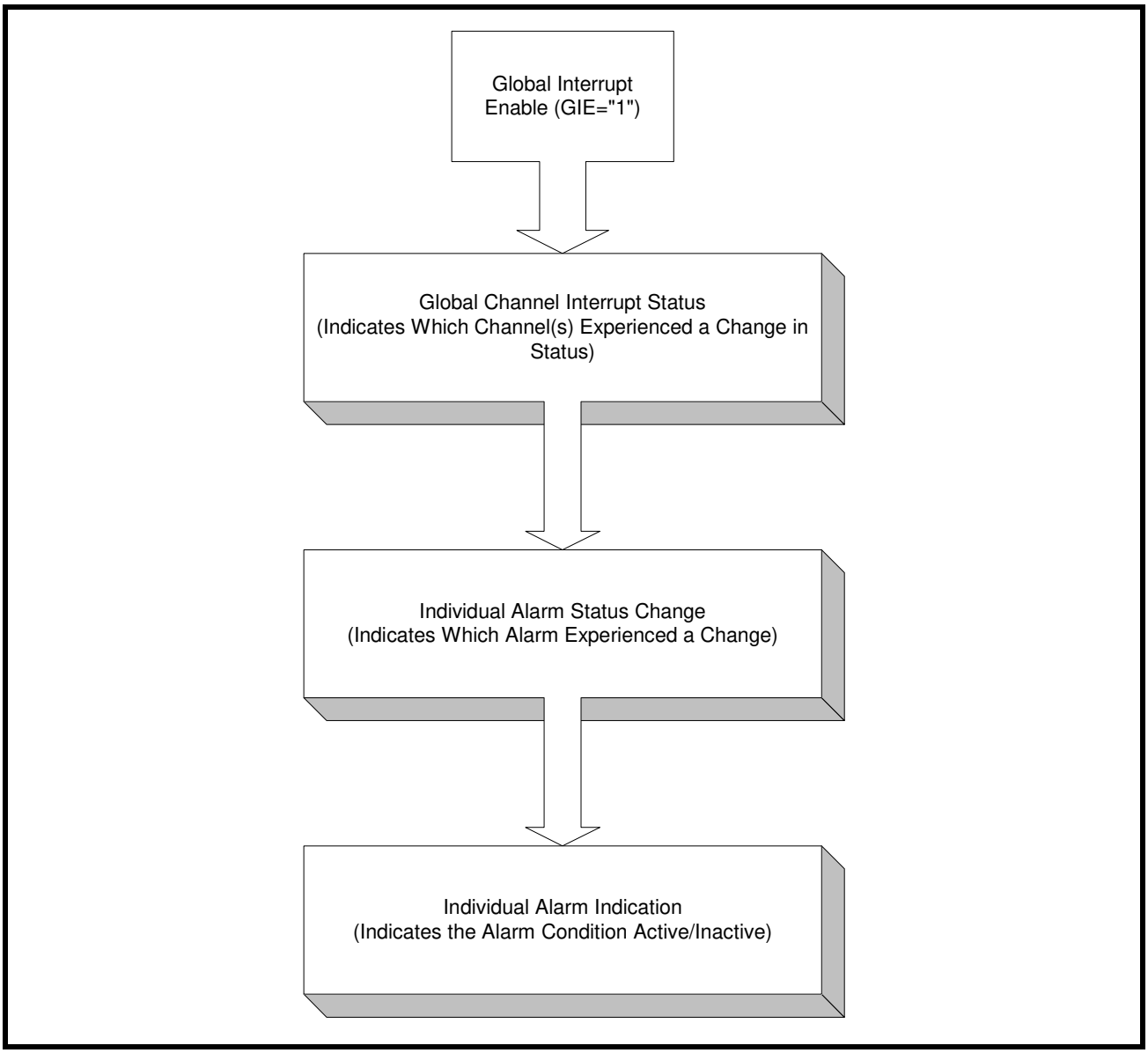
FIGURE 8. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN



3.2.3 General Alarm Detection and Interrupt Generation

The receive path detects RLOS, AIS, QRPD and FLS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (it the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the INT pin will return "High". The status registers are Reset Upon Read (RUR). The interrupts are categorized in a hierarchical process block. Figure 9 is a simplified block diagram of the interrupt generation process.

FIGURE 9. INTERRUPT GENERATION PROCESS BLOCK



NOTE: *The interrupt pin is an open-drain output that requires a 10kΩ external pull-up resistor.*

3.2.3.1 RLOS (Receiver Loss of Signal)

The XRT83VSH314supports both G.775 or ETSI-300-233 RLOS detection scheme.

In G.775 mode, RLOS is declared when the received signal is less than 375mV for 32 consecutive pulse periods (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 425mV (typical).

In ETSI-300-233 mode the device declares RLOS when the input level drops below 375mV (typical) for more than 2048 pulse periods (1msec).

The device exits RLOS when the input signal exceeds 425mV (typical) and has transitions for more than 32 pulse periods with 12.5% ones density with no more than 15 consecutive zero's in a 32 bit sliding window. ETSI-300-233 RLOS detection method is only available in Host mode.

In T1 mode RLOS is declared when the received signal is less than 320mV for 175 consecutive pulse period (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 100 consecutive zeros in a 128 bit sliding window and the signal level exceeds 425mV (typical).

3.2.3.2 EXLOS (Extended Loss of Signal)

By enabling the extended loss of signal by programming the appropriate channel register, the digital RLOS is extended to count 4,096 consecutive zeros before declaring RLOS in T1 and E1 mode. By default, EXLOS is disabled and RLOS operates in normal mode.

3.2.3.3 AIS (Alarm Indication Signal)

The XRT83VSH314 adheres to the ITU-T G.775 specification for an all ones pattern. The alarm indication signal is set to "1" if an all ones pattern (at least 99.9% ones density) is present for T, where T is 3ms to 75ms in T1 mode. AIS will clear when the ones density is not met within the same time period T. In E1 mode, the AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

3.2.4 FLSD (FIFO Limit Status Detection)

The purpose of the FIFO limit status is to indicate when the Read and Write FIFO pointers are within a pre-determined range (over-flow or under-flow indication). The FLSD is set to "1" if the FIFO Read and Write Pointers are within ±3-Bits.

3.2.4.1 LCVD (Line Code Violation Detection)

The LIU contains 14 independent, 16-bit LCV counters. When the counters reach full-scale, they remain saturated at FFFFh until they are reset globally or on a per channel basis. For performance monitoring, the counters can be updated globally or on a per channel basis to place the contents of the counters into holding registers. The LIU uses an indirect address bus to access a counter for a given channel. Once the contents of the counters have been placed in holding registers, they can be individually read out from register 0xE8h 8-bits at a time according to the BYTEsel bit in the appropriate global register. By default, the LSB byte is in register 0xE8h until the BYTEsel is pulled "High" where upon the MSB byte will be placed in the register for read back. Once both bytes have been read, the next channel may be selected for read back.

By default, the LCV_OFD will be set to a "1" if the receiver is currently detecting line code violations or excessive zeros for HDB3 (E1 mode) or B8ZS (T1 mode). In AMI mode, the LCVD will be set to a "1" if the receiver is currently detecting bipolar violations or excessive zeros. However, if the LIU is configured to monitor the 16-bit LCV counter by programming the appropriate global register, the LCV_OFD will be set to a "1" if the counter saturates.