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GENERAL DESCRIPTION

The XRT83VSH316 is a fully integrated 16-channel short-haul line interface unit (LIU) that operates from a 1.8V Inner Core and 3.3V I/O power supplies. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode independently on a per channel basis with minimum external components. The LIU features are programmed through a standard parallel microprocessor interface or SPI (Serial Mode). EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

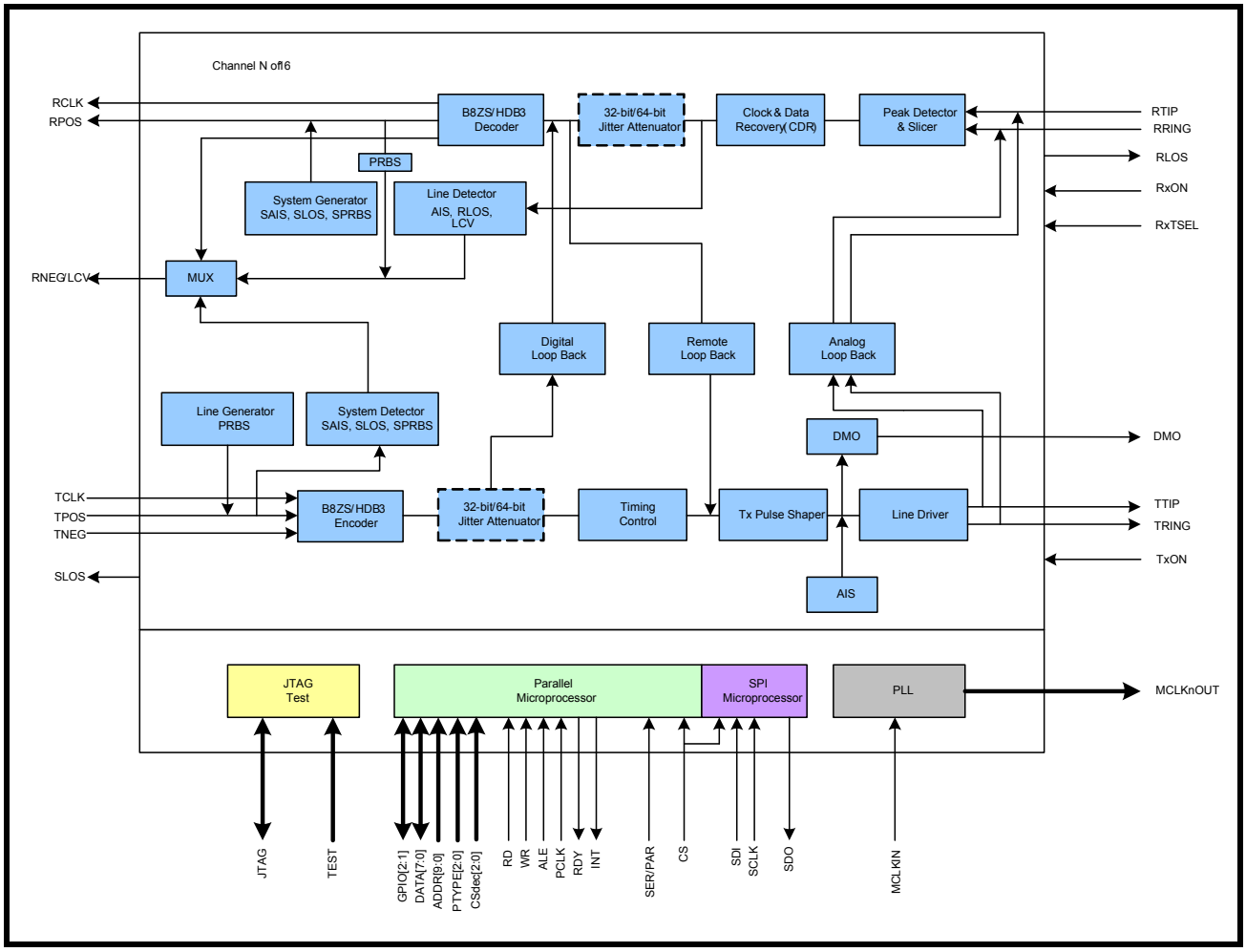
The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and has five output clock references that can be used for external timing (8kHz, 1.544Mhz, 2.048Mhz, nxT1/J1, nxE1).

Additional features include System Side LOS, AIS, QRSS/PRBS and Line Side RLOS, AIS, QRSS/PRBS, DMO with 16-bit LCV counters and diagnostic loopback modes for each channel.

APPLICATIONS

- T1 Digital Cross Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA)
- Wireless Base Stations

FIGURE 1. BLOCK DIAGRAM OF THE XRT83VSH316



FEATURES

- Fully integrated 16-Channel short haul transceivers for T1/J1 (1.544MHz) and E1 (2.048MHz) applications
- Parallel or SPI Microprocessor Interface
- T1/E1/J1 short haul and clock rate are per port selectable through software without changing components
- Internal Impedance matching on both receive and transmit for 75Ω (E1), 100Ω (T1), 110Ω (J1), and 120Ω (E1) applications are per port selectable through software without changing components
- Power down on a per channel basis with independent receive and transmit selection
- Five pre-programmed transmit pulse settings for T1 short haul applications per channel
- User programable Arbitrary Pulse mode for T1 and E1
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis
- Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit path per channel
- Driver failure monitor output (DMO) alerts of possible system or external component problems
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis
- Support for automatic protection switching
- 1:1 and 1+1 protection without relays
- Receive monitor mode handles 0 to 6dB resistive attenuation (flat loss) along with 0 to 6dB cable loss for both T1 and E1
- Loss of signal (LOS) according to ITU-T G.775/ETS300233 (E1) and ANSI T1.403 (T1/J1) for system (SLOS) and line (RLOS) side diagnostics
- Programmable data stream muting upon RLOS detection
- On-Chip HDB3/B8ZS encoder/decoder with an internal 16-bit LCV counter for each channel
- On-Chip digital clock recovery circuit for high input jitter tolerance
- QRSS/PRBS pattern generator and detection for testing and monitoring for system (SPRBS) and line (PRBS) side diagnostics
- Error and bipolar violation insertion and detection
- Transmit all ones (TAOS) Generators and Detectors for system (SAIS) and line (AIS) side diagnostics
- Supports local analog, remote, digital, and dual loopback modes
- Supports gapped clocks for mapper/multiplexer applications
- 1.8V Digital Core
- 3.3V I/O and Analog Core
- 316-Pin STBGA package
- -40°C to +85°C Temperature Range

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83VSH316IB-F	316 Shrink Thin Ball Grid Array (21.0 mm x 21.0 mm, STBGA)	-40^{O}C to +85^{O}C

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1.0 PIN DESCRIPTIONS

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
$\overline{CS}$	A19	I	**Chip Select Input** Active low signal. This signal enables the microprocessor interface by pulling chip select "Low". The microprocessor interface is disabled when the chip select signal returns "High". This pin is used for both the Parallel or the Serial Interface modes. ***NOTE:*** *Internally pulled "High" with a 50k Ω resistor.*
ALE_TS	D15	I	**Address Latch Enable Input (Transfer Start)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{WR}$_R/$\overline{W}$	E15	I	**Write Strobe Input (Read/Write)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{RD}$_$\overline{WE}$	C18	I	**Read Strobe Input (Write Enable)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{RDY}$_$\overline{TA}$	R5	O	**Ready Output (Transfer Acknowledge)** See the Microprocessor section of this datasheet for a description.
$\overline{INT}$	B19	O	**Interrupt Output** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTE:*** *This pin is an open-drain output that requires an external 10KΩ pull-up resistor.*
PCLK	U6	I	**Micro Processor Clock Input** In a synchronous microprocessor interface, PCLK is used as the internal timing reference for programming the LIU. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
ADDR9 ADDR8 ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0	E17 D17 Y18 W18 W17 V17 V16 U16 U15 T15	I	**Address Bus Input** ADDR[9:0] are a direct address bus for permitting access to the internal registers. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
CSdec2 CSdec1 CSdec0	U17 F16 E16	I	**Chip Select Decoder Input Pins [2:0]** CSdec[2:0] are used as a chip select decoder. The LIU has 5 chip select output pins for enabling up to 5 additional devices for accessing internal registers. The LIU has the option to select itself (master device), up to 5 additional devices, or all 6 devices simultaneously by setting the CSdec[2:0] pins specified below. 000 = Master Device 001 = Chip Select Output 1 010 = Chip Select Output 2 011 = Chip Select Output 3 100 = Chip Select Output 4 101 = Chip Select Output 5 110 = Reserved 111 = All Chip Selects Active Including the Master Device *Internally pulled "Low" with a 50k Ω resistor.*
DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0	U5 V5 V4 W4 W3 Y3 Y2 Y5	I/O	**Bi-directional Data Bus** DATA[7:0] is a bi-directional data bus used for read and write operations. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
PTYPE2 PTYPE1 PTYPE0	W19 W2 U4	I	**Microprocessor Type Select Input** PTYPE[2:0] are used to select the microprocessor type interface. 000 = Intel 8051 Asynchronous 001 = Motorola Asynchronous 101 = Power PC Synchronous 111 = MPC8xx Motorola Synchronous ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{\text{Reset}}$	D16	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
$\overline{\text{CS5}}$ $\overline{\text{CS4}}$ $\overline{\text{CS3}}$ $\overline{\text{CS2}}$ $\overline{\text{CS1}}$	C16 C17 B17 B18 A18	O	**Chip Select Output** The XRT83VSH316 can be used to provide the necessary chip selects for up to 5 additional devices by using the CSdec[2:0] input pins. The LIU allows up to 84-channel applications with only using one chip select. See the CSdec[2:0] definition in the pin description.
GPIO1 GPIO0	T16 R16	I/O	**General Purpose Input/Output** These two GPIO pins are controlled through the internal registers in the microprocessor block. One register controls the direction, while the other register is used to store or retrieve the status of these pins.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RxON	Y16	I	**Receive On/Off Input** Upon power up, the receivers are powered off. Turning the receivers On or Off can be selected through the microprocessor interface by programming the appropriate channel register if the hardware pin is pulled "High". If the hardware pin is pulled "Low", all channels are automatically turned off. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
RxTSEL	A16	I	**Receive Termination Control** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register. Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.* **RxTSEL (pin)** / **Rx Termination** 0 / External 1 / Internal *Note: RxTCNTL (bit) must be set to "1"*
RLOS	T4	O	**Receive Loss of Signal (Global Pin for All 16-Channels)** When a line side receive loss of signal occurs for any one of the 16-channels according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel RLOS, see the register map.*
SRLOS	T5	O	**System Receive Loss of Signal (Global Pin for All 16-Channels)** When a system side receive loss of signal occurs for any one of the 16-channels according to ITU-T G.775, the SRLOS pin will go "High" for a minimum of one TCLK cycle. SRLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RCLK15 RCLK14 RCLK13 RCLK12 RCLK11 RCLK10 RCLK9 RCLK8 RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	V12 R17 N18 V15 C15 H18 F17 C12 C9 F4 H3 C6 V6 N3 R4 V9	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RxON is pulled "Low", RCLK maintains its timing by using an internal master clock as its reference. Software control (RCLKE) allows RPOS/RNEG data to be updated on either edge of RCLK. ***NOTE:*** *RCLKE is a global setting that applies to all 16 channels.*

RECEIVER SECTION

<table>
<tr><th>NAME</th><th>PIN</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RCLK_IO</td><td>C5</td><td>I/O</td><td>Recovered Clock Input/Output:
This bi-directional clock can be used in two different modes:
1. As an input, the LIU will use this clock as its internal clock timing synchronization of the 19.44Mhz clock reference.
2. As an output, it is one of 16 recoverd line clocks selected by the Recovered Clock Select [4:0] bits and output through this pin.
See table below.

<table>
<tr><th>Recovered Clock Select [4:0]</th><th>Selected RCLK</th></tr>
<tr><td>0XXXX</td><td>Input</td></tr>
<tr><td>10000</td><td>RCLK0</td></tr>
<tr><td>10001</td><td>RCLK1</td></tr>
<tr><td>10010</td><td>RCLK2</td></tr>
<tr><td>10011</td><td>RCLK3</td></tr>
<tr><td>10100</td><td>RCLK4</td></tr>
<tr><td>10101</td><td>RCLK5</td></tr>
<tr><td>10110</td><td>RCLK6</td></tr>
<tr><td>10111</td><td>RCLK7</td></tr>
<tr><td>11000</td><td>RCLK8</td></tr>
<tr><td>11001</td><td>RCLK9</td></tr>
<tr><td>11010</td><td>RCLK10</td></tr>
<tr><td>11011</td><td>RCLK11</td></tr>
<tr><td>11100</td><td>RCLK12</td></tr>
<tr><td>11101</td><td>RCLK13</td></tr>
<tr><td>11110</td><td>RCLK14</td></tr>
<tr><td>11111</td><td>RCLK15</td></tr>
</table>
</td></tr>
<tr><td>RCLK_T1_E1B</td><td>V18</td><td>I/O</td><td>Recovered Clock Frequency Select
This bi-directional clock can be used in two different modes along with the RCLK_IO pin.
1. As an input (RCLK_IO must be an input), it selects the frequency of the RCLK_IO input. "Low" = E1, "High" = T1.
2. As an output (RCLK_IO must be an output), it indicates the frequency of RCLK_IO, "Low" = E1, "High" = T1.
NOTE: The RCLKSEL[4:0] bits determine whether this pin is an input or output.</td></tr>
</table>

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RPOS15 RPOS14 RPOS13 RPOS12 RPOS11 RPOS10 RPOS9 RPOS8 RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	U12 U19 P19 W15 B15 G19 D19 D12 D9 D2 G2 B6 W6 P2 U2 U9	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.
RNEG15 RNEG14 RNEG13 RNEG12 RNEG11 RNEG10 RNEG9 RNEG8 RNEG7 RNEG6 RNEG5 RNEG4 RNEG3 RNEG2 RNEG1 RNEG0	W11 T18 P18 N19 H19 G18 E18 B11 B10 E3 G3 H2 N2 P3 T3 W10	O	**RNEG/LCV_OF Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin can either be a Line Code Violation or Overflow indicator. If LCV is selected by software and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. However, if OF is selected the LCV pin will pull "High" if the internal LCV counter is saturated. The LCV pin will remain "High" until the LCV counter is reset.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RTIP15 RTIP14 RTIP13 RTIP12 RTIP11 RTIP10 RTIP9 RTIP8 RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	Y12 V20 T20 P20 G20 E20 C20 A12 A9 C1 E1 G1 P1 T1 V1 Y9	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING15 RRING14 RRING13 RRING12 RRING11 RRING10 RRING9 RRING8 RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	Y11 U20 R20 N20 H20 F20 D20 A11 A10 D1 F1 H1 N1 R1 U1 Y10	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TxON	Y19	I	**Transmit On/Off Input** Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 16 transmitters are powered off. ***NOTES:*** *1. TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details.* *2. Internally pulled "Low" with a 50KΩ resistor.*
DMO	T6	O	**Digital Monitor Output (Global Pin for All 16-Channels)** When no transmit output pulse is detected for more than 128 TCLK cycles on one of the 16-channels, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel DMO, see the register map.*
TCLK15 TCLK14 TCLK13 TCLK12 TCLK11 TCLK10 TCLK9 TCLK8 TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	W13 Y15 U13 U14 D14 D13 A15 B13 B8 A6 D8 D7 U7 U8 Y6 W8	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING can be selected to send an all ones or an all zero signal by programming TCLKCNL. In addition, software control (TCLKE) allows TPOS/TNEG data to be sampled on either edge of TCLK. ***NOTES:*** *1. TCLKE is a global setting that applies to all 16 channels.* *2. Internally pulled "Low" with a 50k Ω resistor.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TPOS15 TPOS14 TPOS13 TPOS12 TPOS11 TPOS10 TPOS9 TPOS8 TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	W12 Y14 V13 T14 E14 C13 A14 B12 B9 A7 C8 E7 T7 V8 Y7 W9	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
TNEG15 TNEG14 TNEG13 TNEG12 TNEG11 TNEG10 TNEG9 TNEG8 TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	Y13 W14 T13 V14 C14 E13 B14 A13 A8 B7 E8 C7 V7 T8 W7 Y8	I	**Transmit Negative Data Input** In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TTIP15 TTIP14 TTIP13 TTIP12 TTIP11 TTIP10 TTIP9 TTIP8 TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	T11 P16 L16 L17 K17 K16 G16 E11 E10 G5 K5 K4 L4 L5 P5 T10	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING15 TRING14 TRING13 TRING12 TRING11 TRING10 TRING9 TRING8 TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	V11 N16 M16 M19 J19 J16 H16 C11 C10 H5 J5 J2 M2 M5 N5 V10	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.

CONTROL FUNCTION

NAME	PIN	TYPE	DESCRIPTION
TEST	V3	I	**Factory Test Mode** For normal operation, the TEST pin should be tied to ground. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{ICT}}$	C3	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*

CLOCK SECTION

NAME	PIN	TYPE	DESCRIPTION
MCLKin	A5	I	**Master Clock Input** The master clock input can accept a wide range of inputs that can be used to generate T1 or E1 clock rates on a per channel basis. See the register map for details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
8kHzOUT	B3	O	**8kHz Output Clock**
MCLKE1out	A2	O	**2.048MHz Output Clock**
MCLKE1Nout	A3	O	**2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz Output Clock** See the register map for programming details.
MCLKT1out	B4	O	**1.544MHz Output Clock**
MCLKT1Nout	C4	O	**1.544MHz, 3.088MHz, 6.176MHz, or 12.352MHz Output Clock** See the register map for programming details.
CLK19MHz	M1	O	**19.44MHz Output Clock Reference for Recovered Clock Synchronization** The purpose of this clock is to provide a 19.44MHz clock that is synchronous to either an externally provided clock or to one of the 16 selectable recovered line clocks from the LIU. See Figure 3 for details.
XTAL1	J1	I	**Crystal Input Pin** This pin should be tied to the input pin of a 19.44MHz crystal with an accuracy of +/-20ppm.
XTAL2	K1	O	**Crystal Output Pin** This pin should be tied to the output pin of a 19.44MHz crystal with an accuracy of +/-20ppm.
CMPOUT	L1	O	**Charge Pump Filter Output** See Figure 3 for filtering component selection.

SPI (SERIAL PERIPHERAL INTERFACE)

NOTE: These pins are only used if the SPI interface is used in place of the parallel microprocessor interface. The SPI Microprocessor interface uses shared pins except for SER/PAR.

NAME	PIN	TYPE	DESCRIPTION
SER/PAR	T17	I	**Serial/Parallel Select Input** This pin is used to select between the parallel microprocessor or serial interface. By default, the parallel microprocessor mode is selected. To configure the device for a serial interface, this pin must be pulled "HIgh". *NOTE: Internally pulled "Low" with a 50kΩ resistor.*
SCLK/PCLK	U6	I	**Serial Clock Input** If Pin SER_PAR is pulled "High", this input pin is used as the timing reference for the serial microprocessor interface. See the Microprocessor Section of this datasheet for details.
SDI/ADDR0	T15	I	**Serial Data Input** If Pin SER_PAR is pulled "High", this input pin from the serial interface is used to input the serial data for Read and Write operations. See the Microprocessor Section of this datasheet for details.
SDO/D0	Y5	O	**Serial Data Output** If Pin SER_PAR is pulled "High", this output pin from the serial interface is used to read back the regsiter contents. See the Microprocessor Section of this datasheet for details.

JTAG SECTION

NAME	PIN	TYPE	DESCRIPTION
ATP_TIP ATP_RING	M20 L20	I/O	**Analog Test Pin_TIP** **Analog Test Pin_RING** These pins are used to check continuity of the Transmit and Receive TIP and RING connections on the assembled board. *NOTE: See "Section 5.7, Analog Board Continuity Check" on page 48 for more detailed description.*
TMS	E6	I	**Test Mode Select** This pin is used as the input mode select for the boundary scan chain. *NOTE: Internally pulled "High" with a 50KΩ resistor.*
TCK	D5	I	**Test Clock Input** This pin is used as the input clock source for the boundary scan chain. *NOTE: Internally pulled "High" with a 50KΩ resistor.*
TDI	D6	I	**Test Data In** This pin is used as the input data pin for the boundary scan chain. *NOTE: Internally pulled "High" with a 50KΩ resistor.*
TDO	D4	O	**Test Data Out** This pin is used as the output data pin for the boundary scan chain.

JTAG SECTION

NAME	PIN	TYPE	DESCRIPTION
Analog	C2	O	**Factory Test Mode Pin** ***NOTE:*** *For Internal Use Only*
Sense	B2	O	**Factory Test Mode Pin** ***NOTE:*** *For Internal Use Only*

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
TVDD15 TVDD14 TVDD13 TVDD12 TVDD11 TVDD10 TVDD9 TVDD8 TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0	U11 P17 M17 M18 J18 J17 G17 D11 D10 G4 J4 J3 M3 M4 P4 U10	PWR	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RVDD1 RVDD0	F19 F2	PWR	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV	Y1 Y20 A20 A1	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.
DVDD_PRE DVDD_PRE DVDD_PRE DVDD_PRE DVDD DVDD DVDD DVDD DVDD_μP	V2 V19 C19 D3 E2 T2 T19 E19 Y17	PWR	**Digital Power Supply (1.8V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
AVDD_BIAS AVDD_PLL22 AVDD_PLL21 AVDD_PLL1	J20 A4 A17 Y4	PWR	**Analog Power Supply (1.8V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
TGND15 TGND14 TGND13 TGND12 TGND11 TGND10 TGND9 TGND8 TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	T12 R18 N17 L18 K18 H17 F18 E12 E9 F3 H4 K3 L3 N4 R3 T9	GND	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
RGND1 RGND0	R19 R2	GND	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND DGND DGND DGND	K2 L2 L19 K19	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.
DGND_DRV DGND_DRV DGND_DRV DGND_DRV DGND_PRE DGND_PRE DGND_PRE DGND_PRE DGND_μP	B1 W1 W20 B20 U3 U18 D18 E4 W16	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.
AGND_BIAS AGND_PLL22 AGND_PLL21 AGND_PLL1	K20 B5 B16 W5	GND	**Analog Ground** It's recommended that all ground pins of this device be tied together.

THERMAL GROUND

NAME	PIN	TYPE	DESCRIPTION
THGND15 THGND14 THGND13 THGND12 THGND11 THGND10 THGND9 THGND8 THGND7 THGND6 THGND5 THGND4 THGND3 THGND2 THGND1 THGND0	J9 J10 J11 J12 K9 K10 K11 K12 L9 L10 L11 L12 M9 M10 M11 M12	GND	**Thermal Ground** It's recommended that all ground pins of this device be tied together.

NO CONNECTS

NAME	PIN	TYPE	DESCRIPTION
NC	E5 F5	NC	**No Connect** These pins can be left floating or tied to ground.

2.0 CLOCK SYNTHESIZER

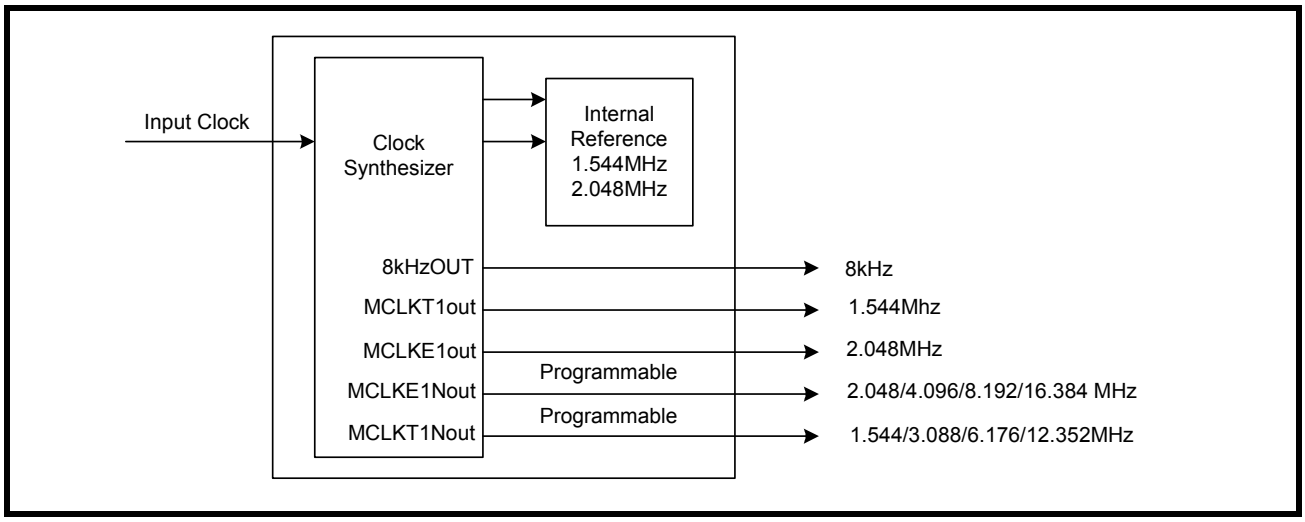
In system design, fewer clocks on the network card could reduce noise and interference. Network cards that support both T1 and E1 modes must be able to produce 1.544MHz and 2.048MHz transmission data. The XRT83VSH316 has a built in clock synthesizer that requires only one input clock reference by programming CLKSEL[3:0] in the appropriate global register. A list of the input clock options is shown in Table 1.

TABLE 1: INPUT CLOCK SOURCE SELECT

CLKSEL[3:0]	INPUT CLOCK REFERENCE
0h (0000)	2.048 MHz
1h (0001)	1.544MHz
8h (1000)	4.096 MHz
9h (1001)	3.088 MHz
Ah (1010)	8.192 MHz
Bh (1011)	6.176 MHz
Ch (1100)	16.384 MHz
Dh (1101)	12.352 MHz
Eh (1110)	2.048 MHz
Fh (1111)	1.544 MHz

The single input clock reference is used to generate multiple timing references. The first objective of the clock synthesizer is to generate 1.544MHz and 2.048MHz for each of the 16 channels. This allows each channel to operate in either T1 or E1 mode independent from the other channels. The state of the equalizer control bits in the appropriate channel registers determine whether the LIU operates in T1 or E1 mode. The second objective is to generate additional output clock references for system use. The available output clock references are shown in Figure 2.

FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE CLOCK SYNTHESIZER

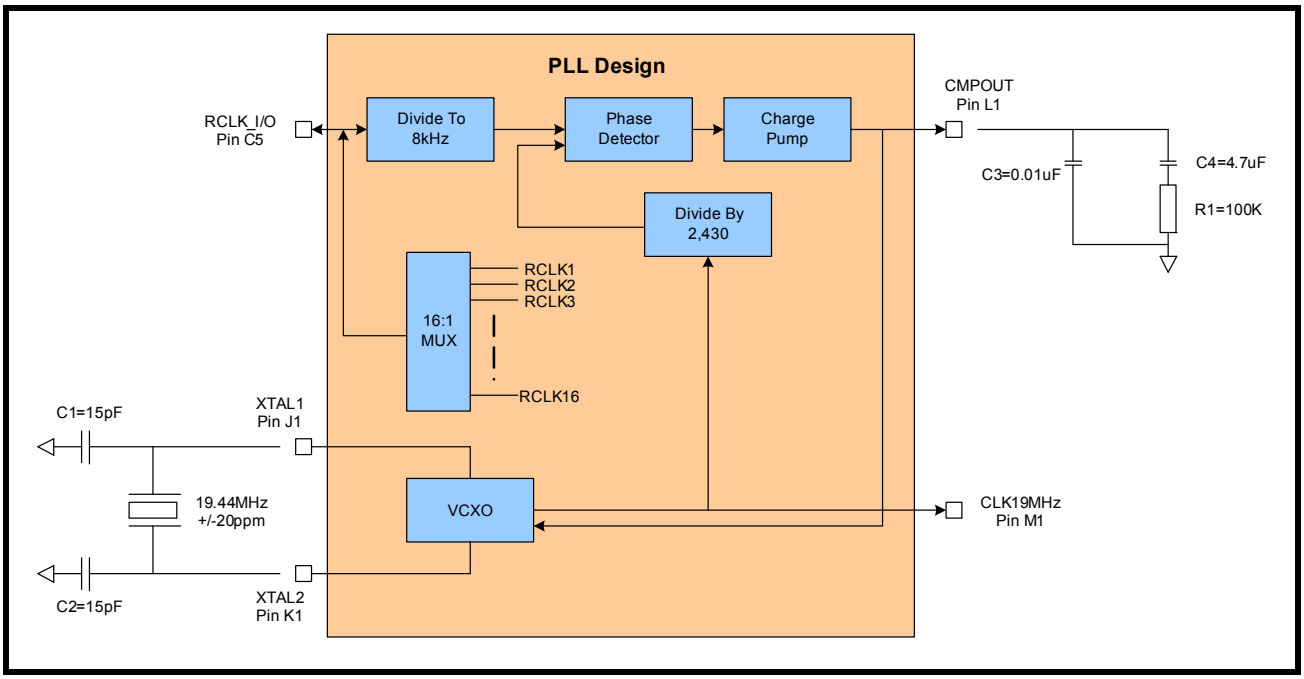


2.1 19.44MHz Output Clock Reference for Recovered Clock Synchronization

For Loop Timing Applications, the EXAR 16-channel LIIU can provide a SONET 19.44MHz clock reference that is synchronized to one of the recovered line clocks from the T1 or E1 line interface or to an externally supplied reference clock. Figure 3 below shows a simplified block diagram with recommend components for this feature. The external crystall connected to XTAL1 and XTAL2 should have a minimum accuracy of +/-20ppm if it is to be used as a SONET/SDH clock reference. The two filtering caps, C1 and C2 are recommendations only. The value of these caps will depend on the system characteristics of the PCB, but should range from 10pf to 20pf.

If RCLK_I/O is configured as an output, it will be connected to one of the 16 channel recovered line clocks. In addition, the recovered line clock that is selected will be used as the reference for the 19.44MHz SONET/SDH output clock. If RCLK_I/O is configured as an input, an external reference clock will be used to derive the 19.44MHz output clock.

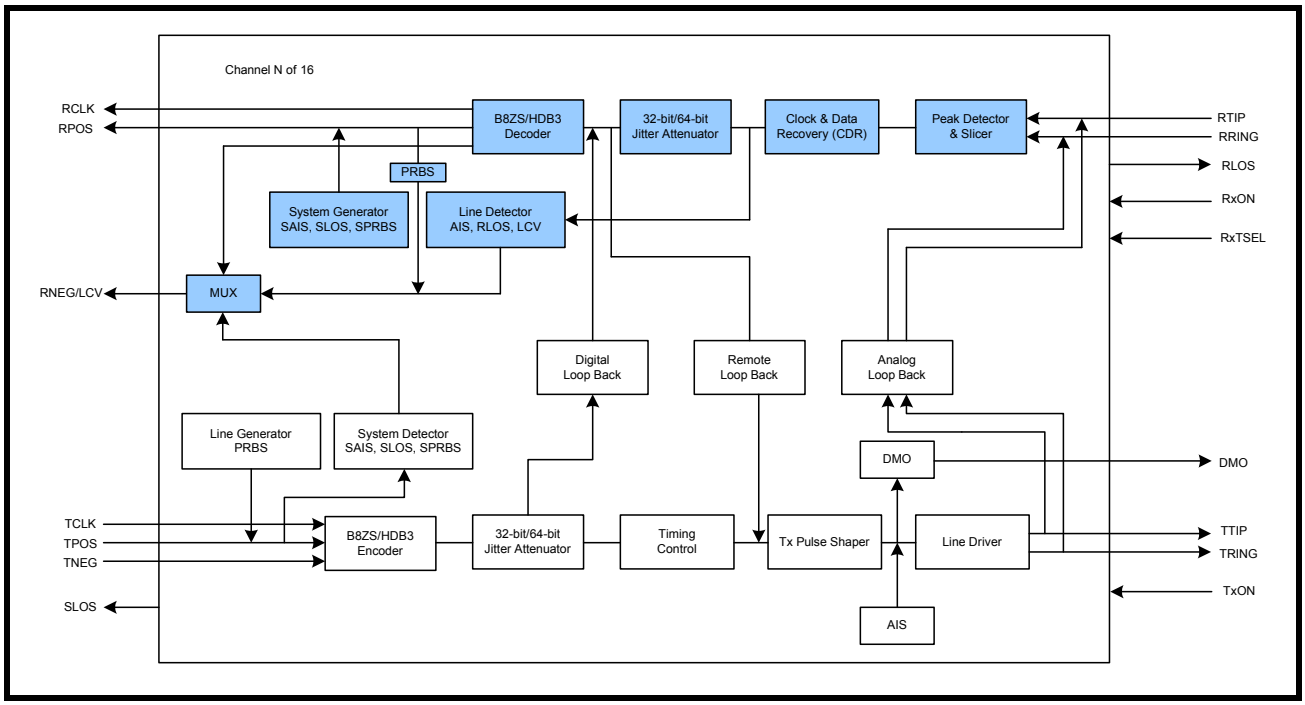
FIGURE 3. 19.44MHZ OUTPUT CLOCK REFERENCE



3.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83VSH316 LIU consists of 16 independent T1/E1/J1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. If any of the diagnostic detection features are used, the LIU must be set in Single Rail mode. Since, the receive path has system diagnostic generators, the part will automatically be placed in Singe Rail Mode whenever one of the diagnostic patterns is used. A simplified block diagram of the receive and transmit path is shown in Figure 4.

FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



3.1 Line Termination (RTIP/RRING)

3.1.1 Internal Termination

The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance (along with the transmit impedance) is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 2.

TABLE 2: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	TRANSMISSION TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT83VSH316 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See Figure 5 for a typical connection diagram using the internal termination.

FIGURE 5. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION

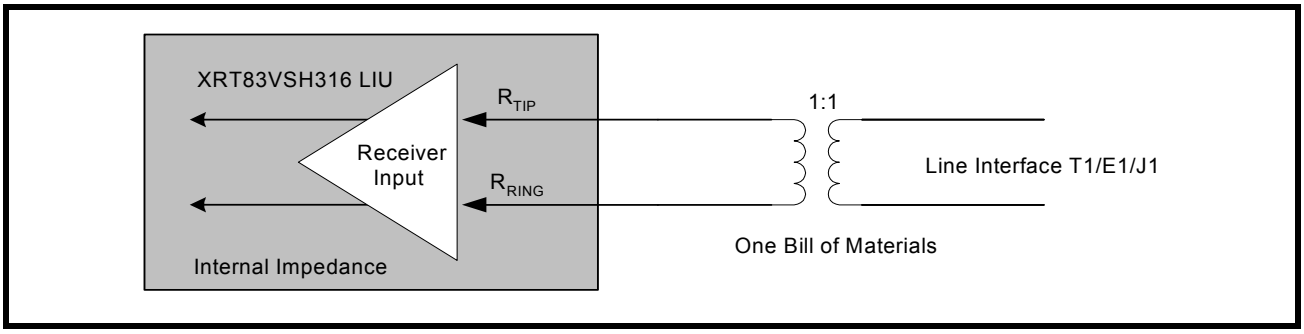


TABLE 3: RECEIVE TERMINATIONS

RXTSEL	TERSEL1	TERSEL0	RXRES1	RXRES0	R_{ext}	R_{int}	MODE
0	x	x	x	x	R_{ext}	∞	T1/E1/J1
1	0	0	0	0	∞	100Ω	T1
1	0	1	0	0	∞	110Ω	J1
1	1	0	0	0	∞	75Ω	E1
1	1	1	0	0	∞	120Ω	E1
1	0	0	0	1	240Ω	172Ω	T1
1	0	1	0	1	240Ω	204Ω	J1
1	1	0	0	1	240Ω	108Ω	E1
1	1	1	0	1	240Ω	240Ω	E1
1	0	0	1	0	210Ω	192Ω	T1
1	0	1	1	0	210Ω	232Ω	J1
1	1	0	1	0	210Ω	116Ω	E1
1	1	1	1	0	210Ω	280Ω	E1
1	0	0	1	1	150Ω	300Ω	T1
1	0	1	1	1	150Ω	412Ω	J1
1	1	0	1	1	150Ω	150Ω	E1
1	1	1	1	1	150Ω	600Ω	E1

3.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1/J1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. Figure 6 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 7 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 4.

FIGURE 6. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

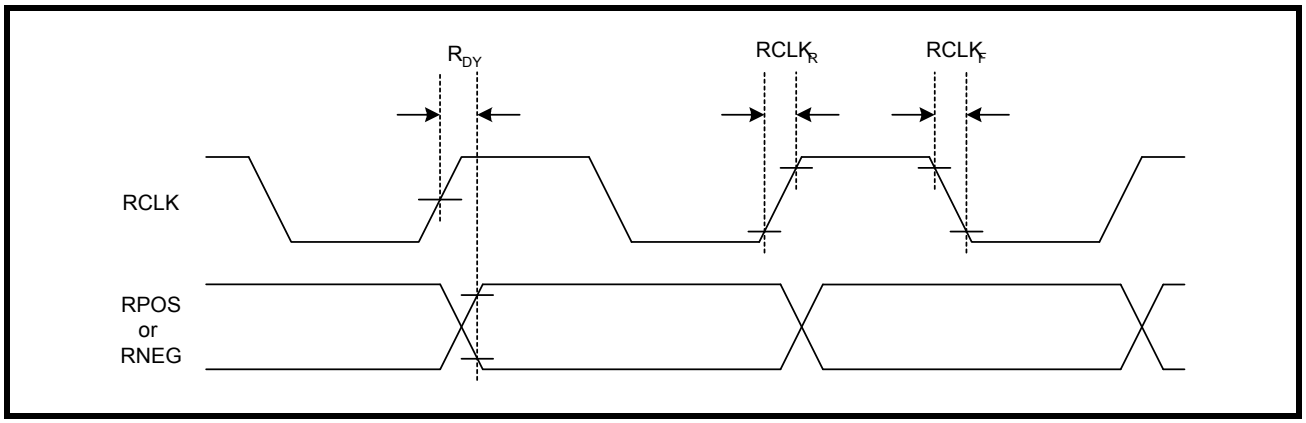


FIGURE 7. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

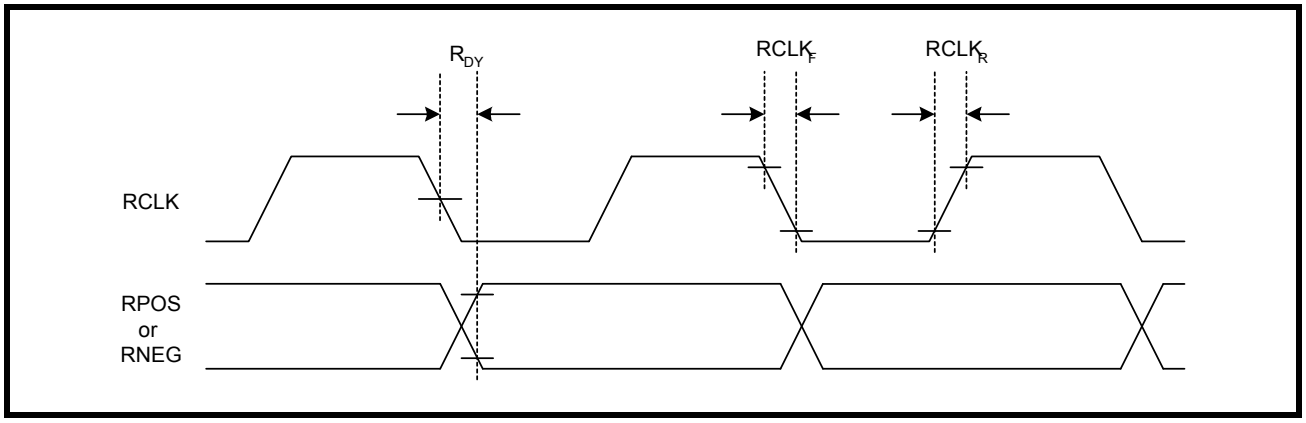


TABLE 4: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
RCLK to Data Delay	R_{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, VDDc=1.8V ±5%, T_A=25°C, Unless Otherwise Specified*