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GENERAL DESCRIPTION

The XRT83VSH38 is a fully integrated 8-channel short-haul line interface unit (LIU) that operates from a 1.8V and a 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode with minimum external components. The LIU features are programmed through a standard parallel or serial microprocessor interface. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and outputs a clock reference of the line rate chosen.

Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/ detection, TAOS, DMO, and diagnostic loopback modes.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

FIGURE 1. BLOCK DIAGRAM OF THE XRT83VSH38 T1/E1/J1 LIU (HOST MODE)

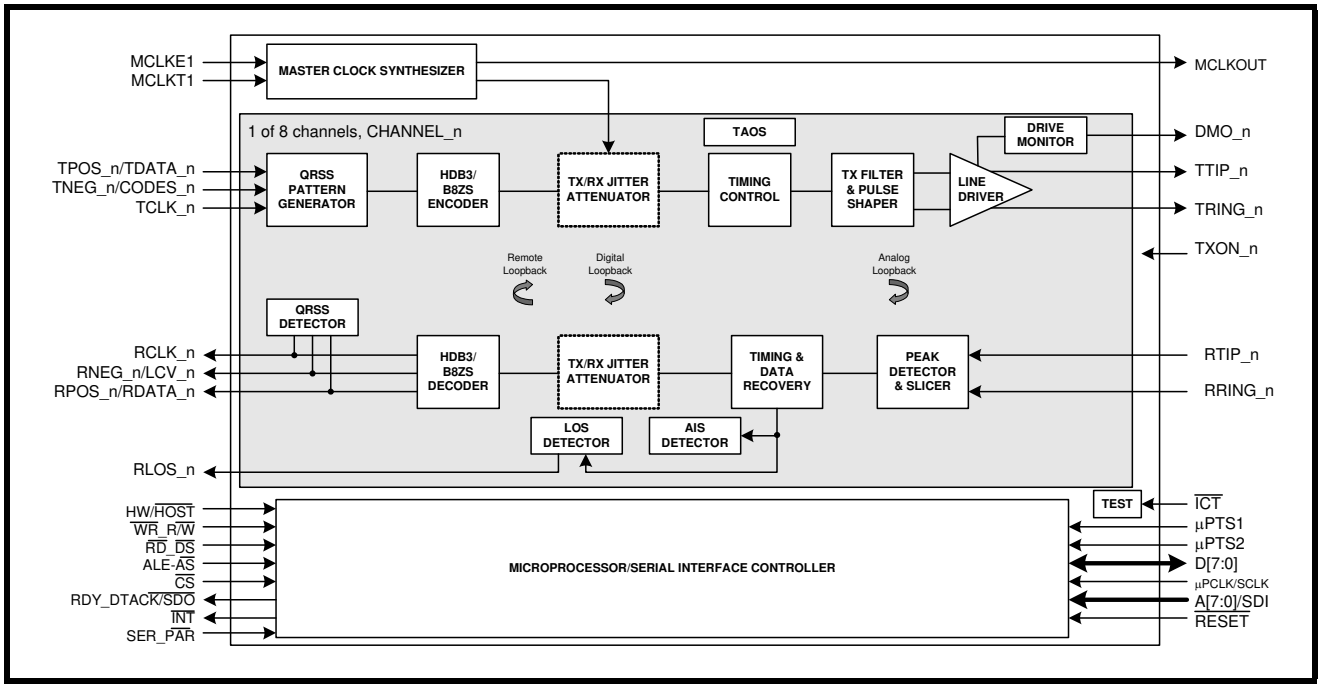
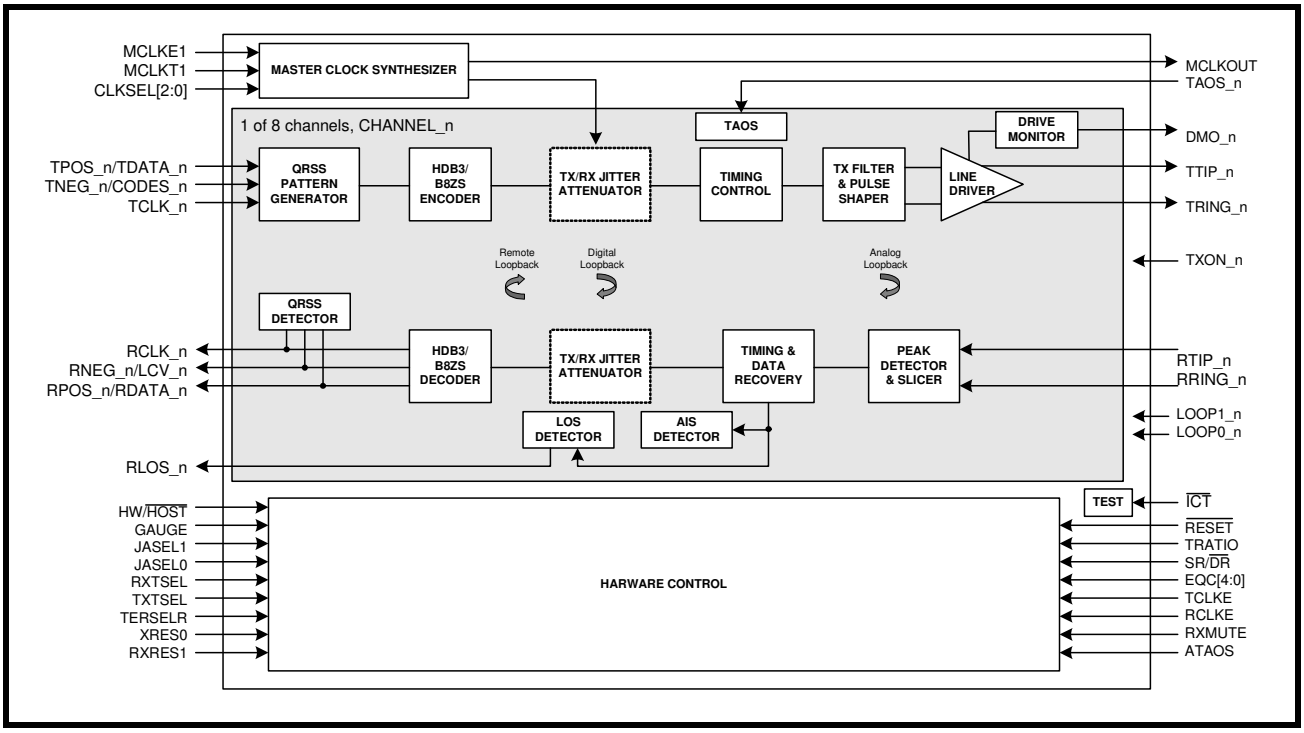


FIGURE 2. BLOCK DIAGRAM OF THE XRT83VSH38 T1/E1/J1 LIU (HARDWARE MODE)

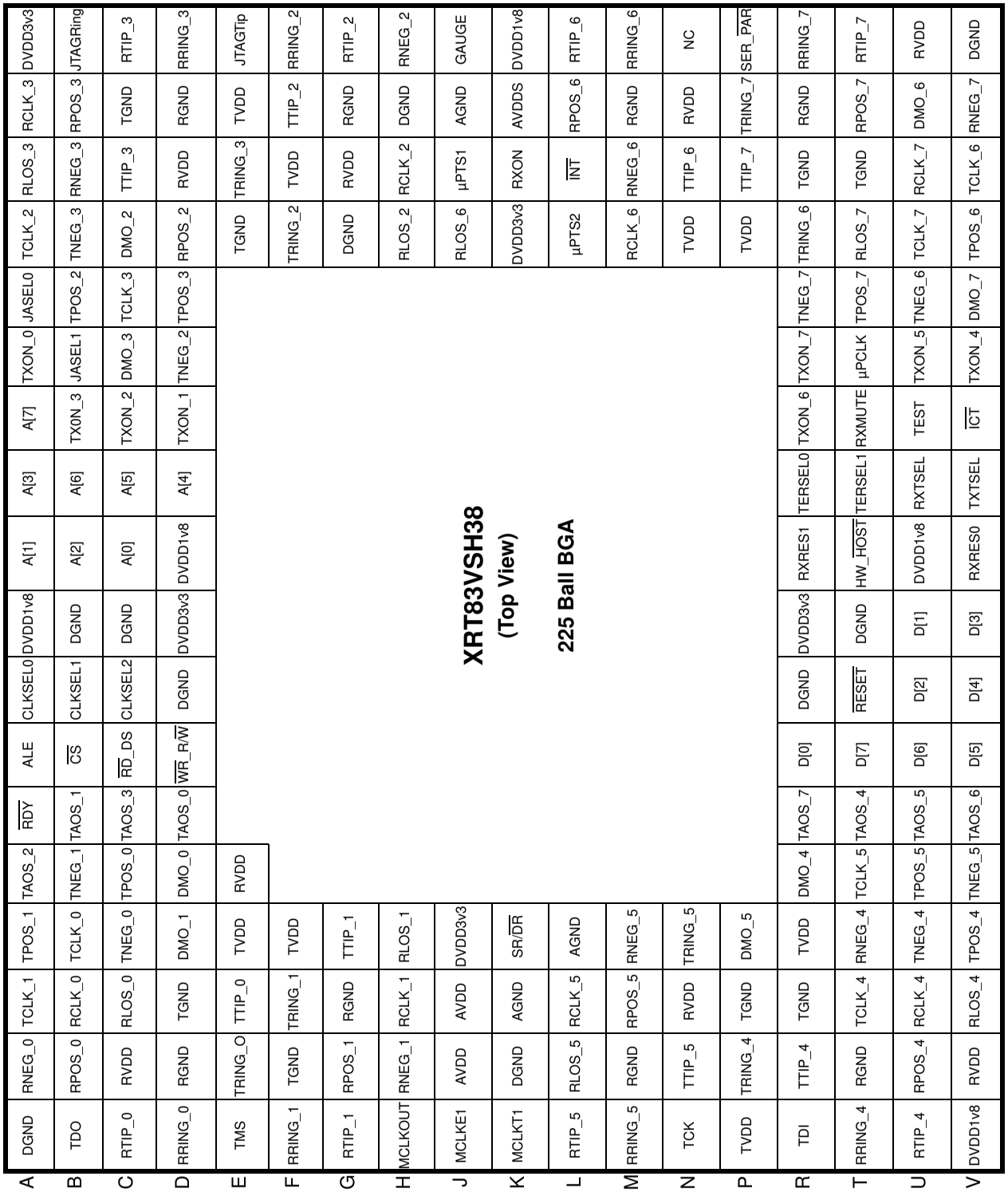


FEATURES

- Fully integrated eight channel short-haul transceivers for T1/J1 (1.544MHz) and E1 (2.048MHz) applications
- T1/E1/J1 short haul and clock rate are per port selectable through software without changing components
- Internal Impedance matching on both receive and transmit for 75Ω (E1), 100Ω (T1), 110Ω (J1), and 120Ω (E1) applications are per port selectable through software without changing components
- Power down on a per channel basis with independent receive and transmit selection
- Five pre-programmed transmit pulse settings for T1 short haul applications per channel
- User programable Arbitrary Pulse mode
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis
- Selectable Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit path
- Driver failure monitor output (DMO) alerts of possible system or external component problems
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis
- Support for automatic protection switching
- 1:1 and 1+1 protection without relays
- Receive monitor mode handles 0 to 6dB resistive attenuation (flat loss) along with 0 to 6dB cable loss for both T1 and E1
- Loss of signal (RLOS) according to ITU-T G.775/ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Programmable data stream muting upon RLOS detection
- On-Chip HDB3/B8ZS encoder/decoder with an internal 16-bit LCV counter for each channel
- On-Chip digital clock recovery circuit for high input jitter tolerance
- QRSS/PRBS pattern generator and detection for testing and monitoring
- Error and bipolar violation insertion and detection
- Transmit all ones (TAOS) Generators and Detectors
- Supports local analog, remote, digital, and dual loopback modes
- Supports gapped clocks for mapper/multiplexer applications
- 1.8V Digital Inner Core
- 3.3V I/O Supply and Analog Inner Core
- 225 ball BGA package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83VSH38IB	225 Ball BGA	-40°C to +85°C



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DGND	RNEG_0	TCLK_1	TPOS_1	TAOS_2	RDY	ALE	CLKSEL0	DVDD1v8	A[1]	A[3]	A[7]	TXON_0	JASEL0	TCLK_2	RLOS_3	RCLK_3	DVDD3v3
B	TDO	RPOS_0	RCLK_0	TCLK_0	TNEG_1	TAOS_1	CS	CLKSEL1	DGND	A[2]	A[6]	TXON_3	JASEL1	TPOS_2	TNEG_3	RNEG_3	RPOS_3	JTAGRing
C	RTIP_0	RVDD	RLOS_0	TNEG_0	TPOS_0	TAOS_3	RD_DS	CLKSEL2	DGND	A[0]	A[5]	TXON_2	DMO_3	TCLK_3	DMO_2	TTIP_3	TGND	RTIP_3
D	RRING_0	RGND	TGND	DMO_1	DMO_0	TAOS_0	WR_R/W	DGND	DVDD3v3	DVDD1v8	A[4]	TXON_1	TNEG_2	TPOS_3	RPOS_2	RVDD	RGND	RRING_3
E	TMS	TRING_O	TTIP_0	TVDD	RVDD										TGND	TRING_3	TVDD	JTAGTip
F	RRING_1	TGND	TRING_1	TVDD											TRING_2	TVDD	TTIP_2	RRING_2
G	RTIP_1	RPOS_1	RGND	TTIP_1											DGND	RVDD	RGND	RTIP_2
H	MCLKOUT	RNEG_1	RCLK_1	RLOS_1											RLOS_2	RCLK_2	DGND	RNEG_2
J	MCLKE1	AVDD	AVDD	DVDD3v3											RLOS_6	µPTS1	AGND	GAUGE
K	MCLKT1	DGND	AGND	SR/DR											DVDD3v3	RXON	AVDDS	DVDD1v8
L	RTIP_5	RLOS_5	RCLK_5	AGND											µPTS2	INT	RPOS_6	RTIP_6
M	RRING_5	RGND	RPOS_5	RNEG_5											RCLK_6	RNEG_6	RGND	RRING_6
N	TCK	TTIP_5	RVDD	TRING_5											TVDD	TTIP_6	RVDD	NC
P	TVDD	TRING_4	TGND	DMO_5											TVDD	TTIP_7	TRING_7	SER_PAR
R	TDI	TTIP_4	TGND	TVDD	DMO_4	TAOS_7	D[0]	DGND	DVDD3v3	RXRES1	TERSEL0	TXON_6	TXON_7	TNEG_7	TRING_6	TGND	RGND	RRING_7
T	RRING_4	RGND	TCLK_4	RNEG_4	TCLK_5	TAOS_4	D[7]	RESET	DGND	HW_HOST	TERSEL1	RXMUTE	µPCLK	TPOS_7	RLOS_7	TGND	RPOS_7	RTIP_7
U	RTIP_4	RPOS_4	RCLK_4	TNEG_4	TPOS_5	TAOS_5	D[6]	D[2]	D[1]	DVDD1v8	RXTSEL	TEST	TXON_5	TNEG_6	TCLK_7	RCLK_7	DMO_6	RVDD
V	DVDD1v8	RVDD	RLOS_4	TPOS_4	TNEG_5	TAOS_6	D[5]	D[4]	D[3]	RXRES0	TXTSEL	ICT	TXON_4	DMO_7	TPOS_6	TCLK_6	RNEG_7	DGND

TABLE OF CONTENTS

PIN DESCRIPTION BY FUNCTION

RECEIVE SECTION

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
RXON	K16	I	**Receiver On** Hardware Mode Only This pin is used to enable the receivers for all channels. By default, the receivers are turned ON in hardware mode. To turn the receivers OFF, pull this pin "Low". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
RLOS0 RLOS1 RLOS2 RLOS3 RLOS4 RLOS5 RLOS6 RLOS7	C3 H4 H15 A16 V3 L2 J15 T15	O	**Receive Loss of Signal** When a receive loss of signal occurs according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. ***NOTE:*** *This pin can be used for redundancy applications to initiate an automatic switch to a backup card.*
RCLK0 RCLK1 RCLK2 RCLK3 RCLK4 RCLK5 RCLK6 RCLK7	B3 H3 H16 A17 U3 L3 M15 U16	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RTIP/RRING are in "High-Z", RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKE. ***NOTE:*** *RCLKE is a global setting that applies to all 8 channels.*
RNEG/LCV0 RNEG/LCV1 RNEG/LCV2 RNEG/LCV3 RNEG/LCV4 RNEG/LCV5 RNEG/LCV6 RNEG/LCV7	A2 H2 H18 B16 T4 M4 M16 V17	O	**RNEG/LCV_OF Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation / Overflow indicator Indicator. If LCV is selected by software and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV_OF pin will pull "High" for a minimum of one RCLK cycle. LCV_OF will remain "High" until there are no more violations. However, if OF (Overflow) is selected, then the LCV_OF pin will pull "High" if the internal LCV counter is saturated. The LCV_OF pin will remain "High" until the LCV counter is reset.
RPOS0 RPOS1 RPOS2 RPOS3 RPOS4 RPOS5 RPOS6 RPOS7	B2 G2 D15 B17 U2 M3 L17 T17	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
RTIP0 RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7	C1 G1 G18 C18 U1 L1 L18 T18	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING0 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7	D1 F1 F18 D18 T1 M1 M18 R18	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP- signal, these pins should be coupled to a 1:1 transformer for proper operation.
RXMUTE	T12	I	**Receive Data Muting** Hardware Mode Only This pin is AND-ed with each of the RLOS functions on a per channel basis. Therefore, if this pin is pulled "High" and a given channel experiences a loss of signal, then the RPOS/RNEG output pins are automatically pulled "Low" to prevent data chattering. To disable this feature, the RxMUTE pin must be pulled "Low". ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor*
RXRES1 RXRES0	R10 V10	I	**Receive External Resistor Control Pins** Hardware mode Only These pins are used in the Receive Internal Impedance mode for unique applications where an accurate resistor can be used to achieve optimal return loss. When RxRES[1:0] are used, the LIU automatically sets the internal impedance to match the line build out. For example: if 240Ω is selected, the LIU chooses an internal impedance such that the parallel combination equals the impedance chosen by TERSEL[1:0]. "00" = No External Fixed Resistor "01" = 240Ω "10" = 210Ω "11" = 150Ω ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor. This feature is available in Host mode by programming the appropriate channel register.*
RCLKE/ µPTS1	J16	I	**Receive Clock Edge** Hardware Mode This pin is used to select which edge of the recovered clock is used to update data to the receiver on the RPOS/RNEG outputs. By default, data is updated on the risinge edge. To udpdate data on the falling edge, this pin must be pulled "High". Host Mode µPTS[2:1] pins are used to select the type of microprocessor to be used for Host communication. "00" = 8051 Intel Asynchronous "01" = 68K Motorola Asynchronous ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*

TRANSMIT SECTION

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TCLKE/µPTS2	L15	I	**Transmit Clock Edge** Hardware Mode This pin is used to select which edge of the transmit clock is used to sample data on the transmitter on the TPOS/TNEG inputs. By default, data is sampled on the falling edge. To sample data on the rising edge, this pin must be pulled "High". Host Mode µPTS[2:1] pins are used to select the type of microprocessor to be used for Host communication. "00" = 8051 Intel Asynchronous "01" = 68K Motorola Asynchronous ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TTIP0 TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7	E3 G4 F17 C16 R2 N2 N16 P16	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING0 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7	E2 F3 F15 E16 P2 N4 R15 P17	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TPOS0 TPOS1 TPOS2 TPOS3 TPOS4 TPOS5 TPOS6 TPOS7	C5 A4 B14 D14 V4 U5 V15 T14	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
TNEG0 TNEG1 TNEG2 TNEG3 TNEG4 TNEG5 TNEG6 TNEG7	C4 B5 D13 B15 U4 V5 U14 R14	I	**Transmitter Negative NRZ Data Input** In dual rail mode, this signal is the negative-rail input data for the transmitter. In single rail mode, this pin can be left unconnected while in Host mode. However, in Hardware mode, this pin is used to select the type of encoding/decoding for the E1/T1 data format. Connecting this pin "Low" enables HDB3 in E1 or B8ZS in T1. Connecting this pin "High" selects AMI data format. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TCLK0 TCLK1 TCLK2 TCLK3 TCLK4 TCLK5 TCLK6 TCLK7	B4 A3 A15 C14 T3 T5 V16 U15	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING sends an all zero signal to the line. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLKE. ***NOTE:*** *1. TCLKE is a global setting that applies to all 8 channels.* ***NOTE:*** *2. Internally pulled "Low" with a 50kΩ resistor.*
TAOS0 TAOS1 TAOS2 TAOS3 TAOS4 TAOS5 TAOS6 TAOS7	D6 B6 A5 C6 T6 U6 V6 R6	I	**Transmit All Ones for Channel** Hardware Mode Only Setting this pin “High” enables the transmission of an all ones pattern to the line from TTIP/TRING. If this pin is pulled “Low”, the transmitters operate in normal throughput mode. ***NOTE:*** *Internally pulled “Low” with a 50kΩ resistor for all channels. This feature is available in Host mode by programming the appropriate channel register.*
TXON0 TXON1 TXON2 TXON3 TXON4 TXON5 TXON6 TXON7	A13 D12 C12 B12 V13 U13 R12 R13	I	**Transmit On/Off Input** Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by software control while in Host mode. However, if TxONCNTL is set "High" in software, or if in Hardware mode, the activity of the transmitter outputs is controlled by the TxON pins. ***NOTE:*** *TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.*

PARALLEL MICROPROCESSOR INTERFACE

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
HW/$\overline{\text{HOST}}$	T10	I	**Mode Control Input** This pin is used to select Host mode or Hardware mode. By default, the LIU is set in Hardware mode. To use Host mode, this pin must be pulled "Low". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
$\overline{\text{WR}}$_R/$\overline{\text{W}}$/EQC0	D7	I	**Write Input(R/$\overline{\text{W}}$)/Equalizer Control Signal 0** Host Mode This pin is used to communicate a Read or Write operation according to the which microprocessor is chosen. See the Microprocessor Section of this datasheet for details. Hardware Mode EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See **Table 22** for more details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{RD}}$_DS/EQC1	C7	I	**Read Input (Data Strobe)/Equalizer Control Signal 1** Host Mode This pin is used to communicate a Read or Write operation according to the which microprocessor is chosen. See the Microprocessor Section of this datasheet for details. Hardware Mode EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See **Table 22** for more details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
ALE/EQC2	A7	I	**Address Latch Input (Address Strobe)** Host Mode This pin is used to latch the address contents into the internal registers within the LIU device. See the Microprocessor Section of this datasheet for details. Hardware Mode EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See **Table 22** for more details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{CS}}$/EQC3	B7	I	**Chip Select Input - Host mode:** Host Mode This pin is used to initiate communication with the microprocessor interface. See the Microprocessor Section of this datasheet for details. Hardware Mode EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See **Table 22** for more details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
$\overline{\text{RDY}}$/EQC4	A6	I/O	**Ready Output (Data Transfer Acknowledge)** Host Mode (Parallel Microprocessor) If Pin SER_$\overline{\text{PAR}}$ is pulled "Low", this output pin from the microprocessor block is used to inform the local µP that the Read or Write operation has been completed and is waiting for the next command. See the Microprocessor Section of this datasheet for details. Hardware Mode EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See **Table 22** for more details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
D[7]/Loop14 D[6]/Loop04 D[5]/Loop15 D[4]/Loop05 D[3]/Loop16 D[2]/Loop06 D[1]/Loop17 D[0]/Loop07	T7 U7 V7 V8 V9 U8 U9 R7	I/O	**Bi-Directional Data Bust/Loopback Mode Select** Host Mode These pins are used for the 8-bit bi-directional data bus to allow data transfer to and from the microprocessor interface. Hardware Mode (Channels 4 through 7) These pins are used to select the loopback mode. Each channel has two loopback pins Loop[1:0]. "00" = No Loopback "01" = Analog Local Loopback "10" = Remote Loopback "11" = Digital Loopback ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
A[7]/Loop13 A[6]/Loop03 A[5]/Loop12 A[4]/Loop02 A[3]/Loop11 A[2]/Loop01 A[1]/Loop10 A[0]/Loop00	A12 B11 C11 D11 A11 B10 A10 C10	I	**Direct Address Bus/Loopback Mode Select** Host Mode These pins are used for the 8-bit direct address bus to allow access to the internal registers within the microprocessor interface. Hardware Mode (Channels 0 through 3) These pins are used to select the loopback mode. Each channel has two loopback pins Loop[1:0]. "00" = No Loopback "01" = Analog Local Loopback "10" = Remote Loopback "11" = Digital Loopback ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
ATAOS	T13	I	**Synchronous Microprocessor Clock/Automatic Transmit All Ones** Hardware Mode This pin is used select an all ones signal to the line interface through TTIP/TRING any time that a loss of signal occurs. This feature is avaiable in Host mode by programming the appropriate global register. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{INT}$	L16	O	**Interrupt Output** Host Mode This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTES:*** 1. *This pin is an open-drain output that requires an external 10KΩ pull-up resistor.* 2. *This pin has an internal PULL-DOWN 50kΩ resistor*

JITTER ATTENUATOR

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
JASEL0 JASEL1	A14 B13	I	**Jitter Attenuator Select Pins Hardware Mode** JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it. ***NOTE:*** *These pins are internally pulled "Low" with 50kΩ resistors.*

JASEL1	JASEL0	JA Path	JA BW Hz		FIFO Size
			T1	E1	
0	0	Disabled	-----	-----	--------
0	1	Transmit	3	10	32/32
1	0	Receive	3	10	32/32
1	1	Receive	3	1.5	64/64

CLOCK SYNTHESIZER

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
MCLKOUT	H1	O	**Synthesized Master Clock Output** This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.
MCLKT1	K1	I	**T1 Master Clock Input** This signal is an independent 1.544MHz clock for T1 systems with accuracy better than ±50ppm and duty cycle within 40% to 60%. MCLKT1 is used in the T1 mode. ***NOTE:*** *All channels must operate at the same clock rate, either T1, E1 or J1. This pin is internally pulled "Low" with a 50kΩ resistor.*

<table>
<tr><th>SIGNAL NAME</th><th>BGA LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>MCLKE1</td><td>J1</td><td>I</td><td>E1 Master Clock Input
A 2.048MHz clock for with an accuracy of better than ±50ppm and a duty cycle of 40% to 60% can be provided at this pin. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation.
NOTE: All channels of the XRT83VSH38 must be operated at the same clock rate, either T1, E1 or J1. This pin is internally pulled “Low” with a 50kΩ resistor.</td></tr>
<tr><td>CLKSEL0
CLKSEL1
CLKSEL2</td><td>A8
B8
C8</td><td>I</td><td>Clock Select inputs for Master Clock Synthesizer
Hardware Mode Only
CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the table below. MCLKRATE is automatically generated from the state of the EQC[4:0] pins.
<table>
<tr><th>MCLKE1 kHz</th><th>MCLKT1 kHz</th><th>CLKSEL2</th><th>CLKSEL1</th><th>CLKSEL0</th><th>MCLKRATE</th><th>CLKOUT/ kHz</th></tr>
<tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1544</td></tr>
<tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr>
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<tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr>
</table>
NOTE: These pins are internally pulled “Low” with a 50kΩ resistor.</td></tr>
</table>

ALARM FUNCTIONS/REDUNDANCY SUPPORT

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
GAUGE	J18	I	**Twisted Pair Cable Wire Gauge Select** Hardware Mode Only This pin is used to match the frequency characteristics according to the gauge of wire used in Telecom circuits. By default, the LIU is matched to 22 gauge or 24 gauge wire. To select 26 gauge, this pin must be pulled "High". ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
DMO0 DMO1 DMO2 DMO3 DMO4 DMO5 DMO6 DMO7	D5 D4 C15 C13 R5 P4 U17 V14	O	**Digital Monitor Output** When no transmit output pulse is detected for more than 128 TCLK cycles within the transmit output buffer, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. ***NOTE:*** *This pin can be used for redundancy applications to initiate an automatic switch to a backup card.*
$\overline{\text{RESET}}$	T8	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
SR/$\overline{\text{DR}}$	K4	I	**Single-Rail/Dual-Rail Data Format** Hardware Mode Only This pin is used to control the data format on the facility side of the LIU to interface to a Framer or Mapper/ASIC device. By default, dual rail mode is selected which relies upon the Framer to handle the encoding/decoding functions. To select single rail mode, this pin must be pulled "High". If single rail mode is selected, the LIU can encode/decode AMI or B8ZS/HDB3 data formats. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
RXTSEL	U11	I	**Receiver Termination Select** Hardware Mode This pin is used to select between the internal and external impedance modes for the receive path. By default, the receivers are configured for external impedance mode, which is ideal for redundancy applications without relays. To select internal impedance, this pin must be pulled "HIgh". Host Mode Internal/External impedance can be selected by programming the appropriate channel registers. However, to assist in redundancy applications, this pin can be used for a hard switch if the RxTCNTL bit is set "High" in the appropriate global register. If RxTCNTL is set "High", the individual RxTSEL register bits are ignored. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TXTSEL	V11	I	**Transmitter Termination Select** Hardware Mode This pin is used to select between the internal and external impedance modes for the transmit path. By default, the receivers are configured for external impedance mode, which is ideal for redundancy applications without relays. To select internal impedance, this pin must be pulled "HIgh". ***NOTE:*** *This pin is internally pulled "Low".*

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TERSEL1 TERSEL0	T11 R11	I	**Termination Impedance Select** Hardware Mode Only The TERSEL[1:0] pins are used to select the transmitter and receiver impedance. By default, the impedance is set to 100Ω. "00" = 100Ω "01" = 110Ω "10" = 75Ω "11" = 120Ω ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*
TEST	U12	I	**Factory Test Mode** For normal operation, the TEST pin should be tied to ground. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{ICT}$	V12	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*

SERIAL MICROPROCESSOR INTERFACE

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
SER_$\overline{PAR}$	P18	I	**Serial/Parallel Select Input (Host Mode Only)** This pin is used in the Host mode to select between the parallel microprocessor or serial interface. By default, the Host mode operates in the parallel microprocessor mode. To configure the device for a serial interface, this pin must be pulled "HIgh". ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
SCLK	T13	I	**Serial Clock Input (Host Mode Only)** If Pin SER_$\overline{PAR}$ is pulled "High", this input pin is used the timing reference for the serial microprocessor interface. See the Microprocessor Section of this datasheet for details.
SDI	C10	I	**Serial Data Input (Host Mode Only)** If Pin SER_$\overline{PAR}$ is pulled "High", this input pin from the serial interface is used to input the serial data for Read and Write operations. See the Microprocessor Section of this datasheet for details.
SDO	R7	O	**Serial Data Output (Host Mode Only)** If Pin SER_$\overline{PAR}$ is pulled "High", this output pin from the serial interface is used to read back the regsiter contents. See the Microprocessor Section of this datasheet for details.
ATP-Tip ATP-Ring	E18 B18		**Analog JTAG Positive Pin** **Analog JTAG Negative Pin**
TDO	B1		**Test Data Out** This pin is used as the output data pin for the boundary scan chain.
TDI	R1		**Test Data In** This pin is used as the input data pin for the boundary scan chain. ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
TCK	N1		**Test Clock Input** This pin is used as the input clock source for the boundary scan chain. ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
TMS	E1		**Test Mode Select** This pin is used as the input mode select for the boundary scan chain. ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*
SENSE	N18	****	**Factory Test Pin**

POWER AND GROUND

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TGND	D3 F2 E15 C17 R3 P3 T16 R16	****	**Transmitter Analog Ground** It's recommended that all ground pins of this device be tied together.
TVDD	E4 F4 F16 E17 R4 P1 N15 P15	****	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RVDD	C2 E5 G16 D16 V2 N3 N17 U18	****	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RGND	D2 G3 G17 D17 T2 M2 M17 R17	****	**Receiver Analog Ground** It's recommended that all ground pins of this device be tied together.
AVDD-Bias	K17 J3 J2	****	**Analog Power Supply (1.8V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
AGND	J17 K3 L4	****	**Analog Ground** It's recommended that all ground pins of this device be tied together.

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
DVDD3v3	A18 R9 D9 K15 J4	****	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.
DVDD1v8	V1 U10 K18 D10 A9	****	**Digital Power Supply (1.8V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor. ***NOTE:*** *For proper operation, the power-up sequence is: bring up 1.8V power befor the 3.3V.*
DGND	A1 R8 T9 H17 B9 D8 C9 G15 K2 V18	****	**Digital Ground** It's recommended that all ground pins of this device be tied together.

FUNCTIONAL DESCRIPTION

The XRT83VSH38 is a fully integrated 8-channel short-haul line interface unit (LIU) that operates from a 1.8V and a 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode with minimum external components. The LIU features are programmed through a standard microprocessor interface or controlled through Hardware mode. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays. The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and outputs a clock reference of the line rate chosen. Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/detection, Network Loop Code generation/detection, TAOS, DMO, and diagnostic loopback modes.

1.0 HARDWARE MODE VS HOST MODE

The LIU supports a parallel or serial microprocessor interface (Host mode) for programming the internal features, or a Hardware mode that can be used to configure the device.

1.1 Feature Differences in Hardware Mode

Some features within the Hardware mode are not supported on a per channel basis. The differences between Hardware mode and Host mode are descibed below in Table 1.

TABLE 1: DIFFERENCES BETWEEN HARDWARE MODE AND HOST MODE

FEATURE	HOST MODE	HARDWARE MODE
Tx Test Patterns	Fully Supported	QRSS diagnostic patterns are not available in Hardware mode. The TAOS feature is available.
RxRES[1:0]	Per Channel	In Hardware mode, RxRES[1:0] is a global setting that applies to all channels.
TERSEL[1:0]	Per Channel	In Hardware mode, TERSEL[1:0] is a global setting that applies to all channels.
EQC[4:0]	Per Channel	In Hardware mode, the EQC[4:0] is a global setting that applies to all channels. ***NOTE:*** *In Host mode, all channels have to operate at one line rate T1 or E1, however each channel can have an individual line build out.*
Dual Loopback	Fully Supported	In Hardware mode, dual loopback mode is not supported. Remote, Analog local, and digital loopback modes are available.
JASEL[1:0]	Per Channel	In Hardware mode, the jitter attenuator selection is a global setting that applies to all channels.
RxTSEL	Per Channel	In Hardware mode, the receive termination select is a global setting that applies to all channels.
TxTSEL	Per Channel	In Hardware mode, the transmit termination select is a global setting that applies to all channels.

2.0 MASTER CLOCK GENERATOR

Using external clock sources, the on-chip frequency synthesizer generates the T1 (1.544MHz) or E1 (2.048MHz) master clocks necessary for the transmit pulse shaping and receive clock recovery circuit. There are two master clock inputs MCLKE1 and MCLKT1. In systems where both T1 and E1 master clocks are available these clocks can be connected to the respective pins. All channels of a given XRT83VSH38 must be operated at the same clock rate, either T1, E1 or J1 modes. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation.

FIGURE 3. TWO INPUT CLOCK SOURCE

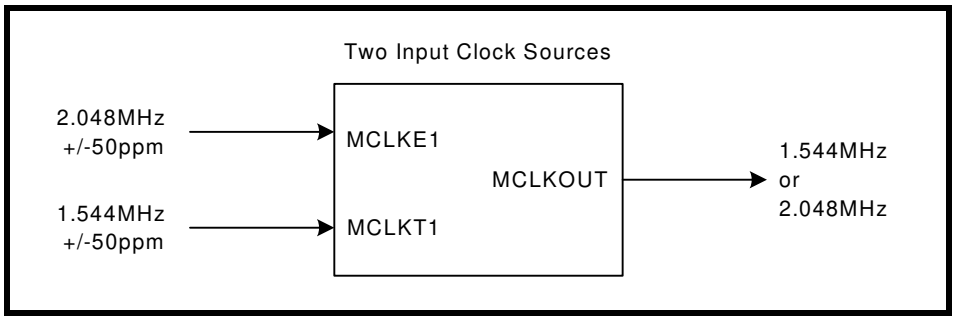


FIGURE 4. ONE INPUT CLOCK SOURCE

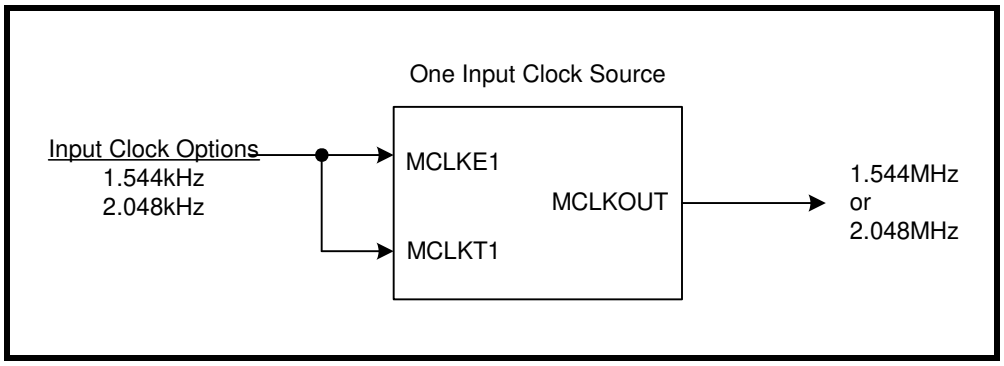


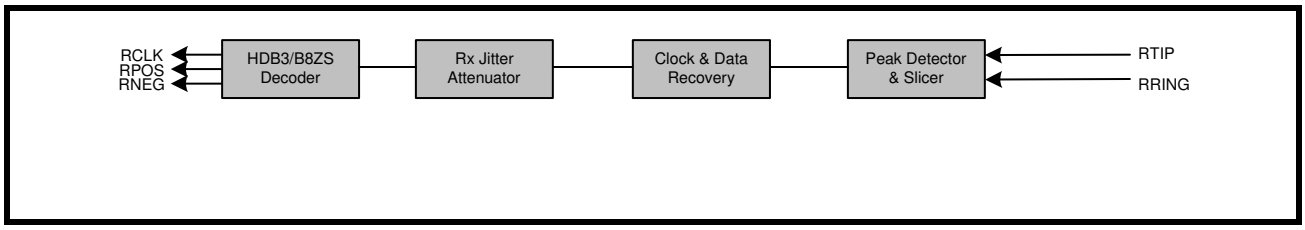
TABLE 2: MASTER CLOCK GENERATOR

MCLKE1 kHz	MCLKT1 kHz	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	MASTER CLOCK kHz
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544

3.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83VSH38 LIU consists of 8 independent T1/E1/J1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in Figure 5.

FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



3.1 Line Termination (RTIP/RRING)

3.1.1 CASE 1: Internal Termination

The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 3.

TABLE 3: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT83VSH38 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See Figure 6 for a typical connection diagram using the internal termination.

FIGURE 6. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION

3.1.2 CASE 2: Internal Termination With One External Fixed Resistor for All Modes

Along with the internal termination, a high precision external fixed resistor can be used to optimize the return loss. This external resistor can be used for all modes of operation ensuring one bill of materials. There are three resistor values that can be used by setting the RxRES[1:0] bits in the appropriate channel register. Selecting the value for the external fixed resistor is shown in Table 4.

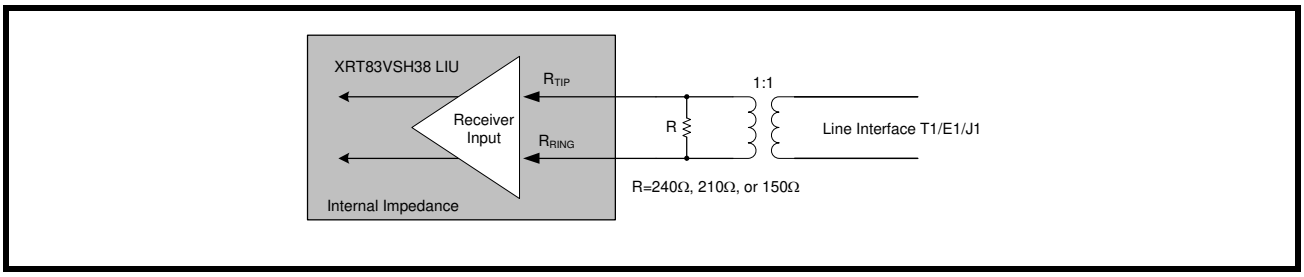
TABLE 4: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR

RxRES[1:0]	EXTERNAL FIXED RESISTOR
0h (00)	None
1h (01)	240Ω
2h (10)	210Ω
3h (11)	150Ω

By default, RxRES[1:0] is set to "None" for no external fixed resistor. If an external fixed resistor is used, the XRT83VSH38 uses the parallel combination of the external fixed resistor and the internal termination as the input impedance. See Figure 7 for a typical connection diagram using the external fixed resistor.

NOTE: *Without the external resistor, the XRT83VSH38 meets all return loss specifications. This mode was created to add flexibility for optimizing return loss by using a high precision external resistor.*

FIGURE 7. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR



3.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1/J1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. **Figure 8** is a timing diagram of the receive data updated on the rising edge of RCLK. **Figure 9** is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in **Table 5**.

FIGURE 8. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

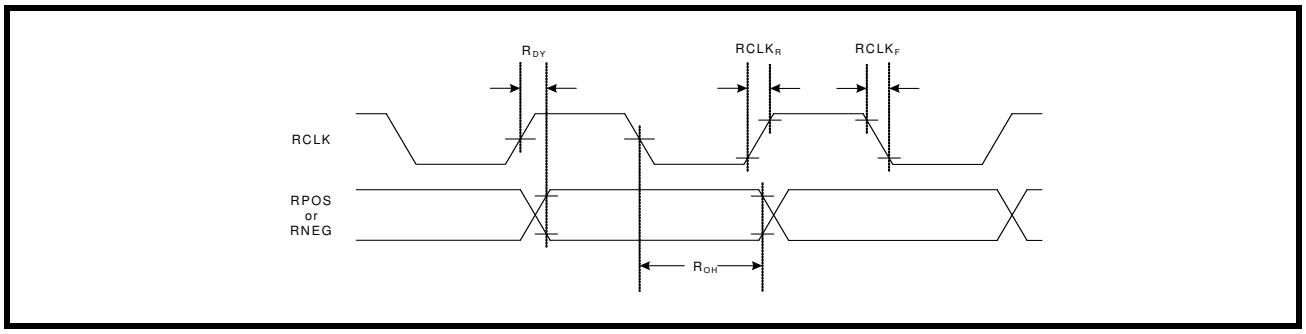


FIGURE 9. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

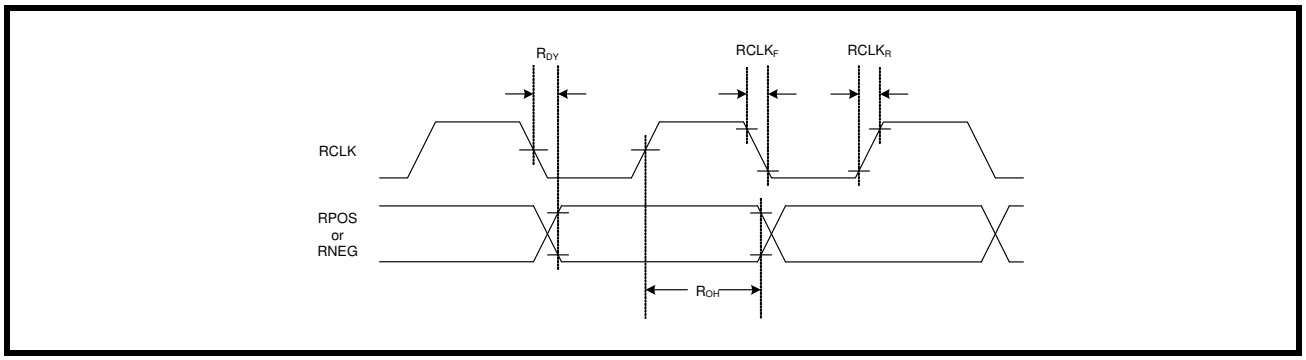


TABLE 5: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-	-	ns
Receive Data Hold Time	R_{HO}	150	-	-	ns
RCLK to Data Delay	R_{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

3.2.1 Receive Sensitivity