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GENERAL DESCRIPTION

The XRT86L30 is a single channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy). The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86L30 provides protection from power failures and hot swapping.

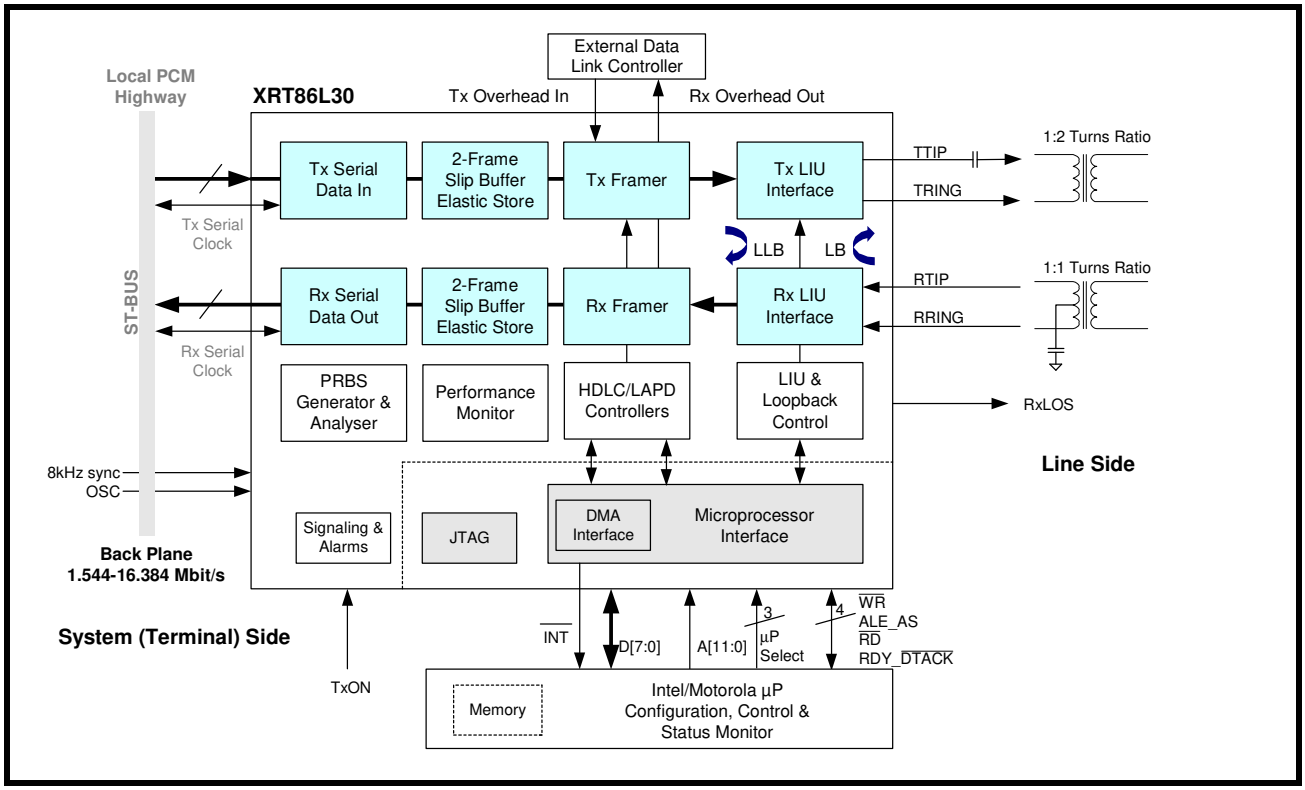
The XRT86L30 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. The framer has a framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

The Framer block contains a Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. The framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86L30 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1999, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86L30 1-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Full duplex DS1 Tx and Rx Framer/LIU
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus (with stuffed don't care bits for the other 3 channels)
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)

- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 3.3V CMOS operation with 5V tolerant inputs
- 128-pin LQFP package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86L30IV	128 LQFP	-40°C to +85°C

LIST OF PARAGRAPHS

LIST OF FIGURES

LIST OF TABLES

1.0 PIN LIST

TABLE 1: LIST BY PIN NUMBER

PIN	PIN NAME
1	LOP
2	NC
3	NC
4	DVDD
5	DGND
6	TRING
7	TVDD
8	TTIP
9	TGND
10	JTAG_RING
11	JTAG_TIP
12	RGND
13	RRING
14	RTIP
15	RVDD
16	AVDD
17	AGND
18	SENSE
19	ANALOG
20	VDDPLL
21	VDDPLL
22	PLLGND
23	PLLGND
24	MCLKIN
25	MCLKnOUT
26	RxOH
27	RxCHN_4
28	RxCHN_3
29	DGND
30	RxCASYNC
31	RxOHCLK
32	RxCHN_2

PIN	PIN NAME
33	RxSYNC
34	NC
35	NC
36	RxCHN_1
37	DVDD
38	RxCHCLK
39	RxCRCSYNC
40	RxCHN_0
41	DVDD
42	RxSERCLK
43	RxLOS
44	RxSER
45	TxCHN_4
46	TxCHN_3
47	TxCHN_2
48	DGND
49	TxCHCLK
50	TxCHN_1
51	TxOH
52	DVDD
53	TxCHN_0
54	TxSERCLK
55	TxSER
56	DVDD
57	TxOHCLK
58	TxMSYNC
59	TxSYNC
60	DGND
61	REQ1
62	ACK0
63	DVDD
64	REQ0
65	ACK1
66	NC

PIN	PIN NAME
67	NC
68	PCLK
69	DATA0
70	DATA1
71	RD
72	DGND
73	DBEN
74	RDY
75	ADDR0
76	ADDR1
77	ADDR2
78	DVDD
79	ADDR3
80	ADDR4
81	ADDR5
82	ADDR6
83	DGND
84	ADDR7
85	RESET
86	OSCCLK
87	DGND
88	8KSYNC
89	ADDR8
90	DATA2
91	DATA3
92	DVDD
93	ALE
94	ADDR9
95	ADDR10
96	INT
97	ADDR11
98	NC
99	NC
100	BLAST

PIN	PIN NAME
101	DATA4
102	DGND
103	DATA5
104	DATA6
105	DVDD
106	DATA7
107	WR
108	CS
109	DGND
110	DGND
111	TCK
112	TRST
113	TDI
114	TMS
115	TDO
116	GPIO1
117	GPIO0
118	GPIO2
119	GPIO3
120	aTEST
121	TEST
122	8KEXTOSC
123	fADDR
124	iADDR
125	PTYPE2
126	PTYPE1
127	PTYPE0
128	TxON

2.0 PIN DESCRIPTIONS

TRANSMIT SERIAL DATA INPUT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxSER	55	I	Transmit Serial Data Input This input pin along with TxSERCLK functions as the Transmit Serial input port to the framer block. DS1 Mode Any payload data applied to this pin will be inserted into a DS1 frame and output onto the T1 line. If the framer is configured accordingly, the framing alignment bits, facility data link bits, and the CRC-6 bits can be inserted to this input pin. The signal applied to this input pin can be latched to the Transmit Payload Data Input Interface on either the rising edge or the falling edge of TxSERCLK. E1 Mode Any payload data applied to this pin will be inserted into an E1 frame and output onto the E1 line. All data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31 must be applied to this input pin. If the framer is configured accordingly, data intended for Time Slots 0 and 16 can also be applied to this input pin. Framer Bypass Mode In framer bypass mode, TxSER is used for the positive digital input pin to the LIU.
TxSERCLK	54	I/O	Transmit Serial Clock Input/Output This clock signal is used by the Transmit payload data Input Interface to latch the contents of the TxSER signal into the framer. Data that is applied at the TxSER input can be latched on either the rising edge or the falling edge of TxSERCLK. DS1/E1 Standard Rate Mode (1.544Mhz/2.048MHz) If the Transmit Section of the framer has been configured to use TxSERCLK as the timing source, then this signal will be an input. If the recovered line clock or the MCLKIN input pin is used as the timing source for the transmitter, then TxSERCLK will be an output. DS1/E1 High-Speed Backplane Interface In High-Speed backplane applications, TxSERCLK is used as the timing source for the transmit line rate. Framer Bypass Mode In framer bypass mode, TxSERCLK is used for the transmit clock to the LIU.
TxSYNC	59	I/O	Transmit Single Frame Sync Pulse Input/Output This pin is configured to be an input if TxSERCLK is used as the timing reference for the transmitter. This pin is configured as an output if the recovered line clock or the MCLKIN input pin is used as the timing reference for the transmitter. DS1/E1 (TxSYNC as an Input) TxSYNC must pulse "High" for one period of TxSERCLK when the transmit payload data Input Interface is processing the first bit of an outbound DS1/E1 frame. ***NOTE:*** *It is imperative that the TxSYNC input signal be synchronized with the TxSERCLK input signal.* DS1/E1 (TxSYNC as an output) TxSYNC will pulse "High" for one period of TxSERCLK when the transmit payload data Input Interface is processing the first bit of an outbound DS1/E1 frame. Framer Bypass Mode In framer bypass mode, TxSYNC is used for the negative digital input pin to the LIU.

TRANSMIT SERIAL DATA INPUT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxMSYNC/ TxINCLK	58	I/O	Multiframe Sync Pulse/Transmit Input Clock This pin is a multiplexed I/O pin. When the device is configured to be in standard rate mode, this signal indicates the boundary of an outbound multi-frame. When the device is configured to be in High-Speed mode, this pin functions as an input clock signal for the high-speed Transmit back-plane interface. DS1/E1 Standard Rate Mode (TxMSYNC as an Input) This pin is configured to be an input if TxSERCLK is used as the timing reference for the transmitter. TxMSYNC must pulse "High" for one period of TxSERCLK when the transmit payload data Input Interface is processing the first bit of an outbound DS1/E1 multi frame. ***NOTE:*** *It is imperative that the TxMSYNC input signal be synchronized with the TxSERCLK input signal.* DS1/E1 Standard Rate Mode (TxMSYNC as an output) This pin is configured as an output if the recovered line clock or the MCLKIN input pin is used as the timing reference for the transmitter. TxMSYNC will pulse "High" for one period of TxSERCLK when the transmit payload data Input Interface is processing the first bit of an outbound DS1/E1 frame. DS1/E1 Non-Multiplexed High-Speed Backplane Interface In the non-multiplexed high-speed interface mode, this pin is used as the timing source for the high-speed data applied to TxSER. The non-multiplexed modes supported are MVIP 2.048MHz, 4.096MHz, and 8.192MHz. ***NOTE:*** *For DS1 mode, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* DS1/E1 Multiplexed High-Speed Backplane Interface In the multiplexed high-speed interface mode, this pin is used as the timing source for the high-speed data applied to TxSER. The multiplexed modes supported are 12.352MHz (DS1 only), 16.384MHz, 16.384MHz HMVIP, and 16.384MHz H.100. For DS1 mode in 16.384MHz rate, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).
TxCHCLK	49	O	Transmit Channel Clock Output Signal This pin indicates the boundary of each time slot of an outbound DS1/E1 frame. DS1/E1 Mode Each of these output pins is 192kHz/256kHz clock for DS1/E1 respectively which pulses "High" whenever the Transmit Payload Data Input Interface block accepts the LSB of each of the 24/32 time slots. The Terminal Equipment can use this clock signal to sample the TxCHN0 through TxCHN4 time slot identifier pins. DS1/E1 Fractional Interface Clock In the fractional interface mode, TxCHCLK can be configured to function as one of the following: The pin will output a gapped fractional clock that can be used by terminal equipment input fractional payload data using the falling edge of the clock. Otherwise the fractional payload data is clocked into the chip using the un-gapped TxSERCLK pin.

TRANSMIT SERIAL DATA INPUT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxCHN_0/ TxSig	53	O I	Transmit Time Slot Octet Identifier Output-Bit 0 These output signals (TxCHN4_n through TxCHN0_n) reflect the five-bit binary value of the number of the current time slot being accepted and processed by the transmit payload data input Interface block. Terminal Equipment can use TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. Transmit Serial Signaling Bus Input These pins can be used to input robbed-bit signaling data within an outbound DS1 frame or to input Channel Associated Signaling (CAS) bits within an outbound E1 frame.
TxCHN_1/ TxFrTD	50	I/O	Transmit Time Slot Octet Identifier Output-Bit 1 These output signals (TxCHN4_n through TxCHN0_n) reflect the five-bit binary value of the number of Time Slot being accepted and processed by the transmit payload data input Interface. Terminal Equipment can use TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. Transmit Serial Fractional DS1/E1 Input These pins can be used to input fractional DS1/E1 payload data within an outbound DS1/E1 frame. In this mode, terminal equipment will use either TxCHCLK or TxSERCLK to sample fractional DS1/E1 payload data.
TxCHN_2/ Tx12MHz	47	O	Transmit Time Slot Octet Identifier Output-Bit 2 These output signals (TxCHN4_n through TxCHN0_n) reflect the five-bit binary value of the number of Time Slot being accepted and processed by the transmit payload data input Interface block. Terminal Equipment can use TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. If TxCHN1_n is configured as TxFrTD_n to input fractional DS1/E1 payload data, the TxCHN2_n pin will serially output the five-bit binary value of the number of the Time Slot being accepted and processed. Transmit 12.352MHz Clock Output These pins can be used to output 12.352MHz/16.384MHz clock derived from the MCLKIN input pin.
TxCHN_3/ TxOHSync	46	O	Transmit Time Slot Octet Identifier Output-Bit 3: These output signals (TxCHN4_n through TxCHN0_n) reflect the five-bit binary value of the number of Time Slot being accepted and processed by the transmit payload data input Interface block. Terminal Equipment can use TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. Transmit Overhead Synchronization Pulse These pins can be used to output an Overhead Synchronization Pulse that indicates the first bit of each multi-frame.
TxCHN_4	45	O	Transmit Time Slot Octet Identifier Output-Bit 4: These output signals (TxCHN4_n through TxCHN0_n) reflect the five-bit binary value of the number of Time Slot being accepted and processed by the transmit payload data input Interface block. Terminal Equipment can use TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed.

OVERHEAD INTERFACE

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxOH	51	I	Transmit Overhead Input This input pin, along with TxOHCLK functions as the Transmit Overhead input port. DS1 Mode This input pin will become active if the Transmit Section has been configured to use this input as the source for the Facility Data Link bits in ESF framing mode, Fs bits in the SLC96 and N framing mode, and R bit in T1DM mode. The data that is input into this pin will be inserted into the Data Link Bits within the outbound DS1 frames at the falling edge of TxSERCLK. ***NOTE:*** *This input pin will be disabled if the framer is using the Transmit HDLC Controller, or the TxSER input as the source for the Data Link Bits.* E1 Mode This input pin will become active if the Transmit Section has been configured to use this input as the source for the Data Link bits. The data that is input into this pin will be inserted into the Sa4 through Sa8 bits (the National Bits) within the outbound non-FAS E1 frames. ***NOTE:*** *This input pin will be disabled if the framer is using the Transmit HDLC Controller, or the TxSER input as the source for the Data Link Bits.*
TxOHCLK	57	O	Transmit OH Serial Clock Output Signal This output clock signal functions as a demand clock signal for the transmit overhead data input interface block. DS1/E1 Mode If the TxOH pins have been configured to be the source for the Facility Data Link bits, then the framer will provide a clock edge for each Data Link Bit. The Data Link Equipment can provide data to TxOH on the rising edge of TxOHCLK. The framer will latch the data on the falling edge of this clock signal.
RxOH	26	O	Receive Overhead Output This pin, along with RxOHCLK functions as the Receive Overhead Output Interface. DS1 Mode This pin unconditionally outputs the contents of the Facility Data Link Bit in ESF framing mode, Fs bit in the SLC96 and N framing mode, and R bit in T1DM framing mode. ***NOTE:*** *This output pin is active even if the Receive HDLC Controller is active.* E1 mode This pin unconditionally outputs the contents of the National Bits (Sa4 through Sa8). If the framer has been configured to interpret the National bits of the incoming E1 frames as carrying Data Link information, then the Receive Overhead Output Interface will provide a clock pulse on RxOHCLK for each Sa bit carrying Data Link information. ***NOTE:*** *This output pin is active even if the Receive HDLC Controller is active.*
RxOHCLK	31	O	Receive OH Serial Clock Output Signal This pin, along with RxOH functions as the Receive Overhead Output Interface. DS1/E1 Mode This pin outputs a clock edge corresponding to each Facility Data Link Bit which carries Data Link information. The Data Link Equipment can sample data from RxOH on the rising edge of RxOHCLK. The framer will update the data on the falling edge of this clock signal.

RECEIVE SERIAL DATA OUTPUT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSYNC	33	I/O	Receive Single Frame Sync Pulse Input/Output This pin is configured to be an input if the slip buffer is enabled in the receive path. Otherwise, this pin is an output signal. DS1/E1 (RxSYNC as an Input) RxSYNC must pulse "High" for one period of RxSERCLK and repeat every 125µS. The framer will output the first bit of an inbound DS1/E1 frame during the provided RxSYNC pulse. ***NOTE:*** *It is imperative that the RxSYNC input signal be synchronized with RxSERCLK.* DS1/E1 (TxSYNC as an output) RxSYNC will pulse "High" for one period of RxSERCLK when the receive payload data Input Interface is processing the first bit of an inbound DS1/E1 frame. Framer Bypass Mode In framer bypass mode, RxSYNC is used for the negative digital output pin to the LIU.
RxCRCSYNC	39	O	**Multiframe Sync Pulse Output** This DS1 only signal will pulse "High" for one period of RxSERCLK the instant that the Receive payload data Interface is processing the first bit of a DS1 Multi-frame.
RxCASYNC	30	O	**Receive CAS Multiframe Sync Output Signal** This E1 only signal will pulse "High" for one period of RxSERCLK the instant that the Receive payload data Interface is processing the first bit of an E1 CAS Multi-frame.
RxSERCLK	42	I/O	Receive Serial Clock Signal This clock signal is used by the Receive payload data Output Interface to latch/update the contents of RxSER. The output data on RxSER can be updated on either the rising edge or the falling edge of RxSERCLK. This pin is configured to be an input if the slip buffer is enabled in the receive path. Otherwise, this pin is an output signal. DS1/E1 Non-Multiplexed High-Speed Backplane Interface (Input Only) In the non-multiplexed high-speed interface mode, this pin is used as the timing source for the high-speed output data to RxSER. The non-multiplexed modes supported are MVIP 2.048MHz, 4.096MHz, and 8.192MHz. ***NOTE:*** *For DS1 mode, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* DS1/E1 Multiplexed High-Speed Backplane Interface (Input Only) In the multiplexed high-speed interface mode, this pin is used as the timing source for the high-speed output data to RxSER. The multiplexed modes supported are 12.352MHz (DS1 only), 16.384MHz, 16.384MHz HMVIP, and 16.384MHz H.100. For DS1 mode in 16.384MHz rate, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care). Framer Bypass Mode: In framer bypass mode, RxSERCLK is used for the receive clock to the LIU.

RECEIVE SERIAL DATA OUTPUT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSER	44	O	Receive Serial Data Output This output pin along with RxSERCLK functions as the Receive Serial Output. DS1/E1 mode Any incoming T1/E1 line data that is received from the line will be decoded and output via this pin. The framer can use either the rising edge or the falling edge of RxSERCLK to update the received T1/E1 payload data. Framer Bypass Mode: In framer bypass mode, RxSER is used for the positive digital output pin to the LIU.
RxCHN_0/ RxSig	40	O	Receive Time Slot Octet Identifier Output-Bit 0 These output signals (RxCHN4_n through RxCHN0_n) reflect the five-bit binary value of the number of Time Slot being received and output to the Terminal Equipment via the Receive Payload Data Output Interface. The Terminal Equipment can use RxCHCLK to sample these five output pins in order to identify the time slot being processed. Receive Serial Signaling Output These pins can be used to output robbed-bit signaling (DS1) or CAS signaling (E1) extracted from an incoming DS1/E1 frame.
RxCHN_1/ RxFrTD	36	O	Receive Time Slot Octet Identifier Output-Bit 1 These output signals (RxCHN4_n through RxCHN0_n) reflect the five-bit binary value of the number of Time Slot being received and output to the Terminal Equipment via the Receive Payload Data Output Interface. The Terminal Equipment can use RxCHCLK to sample these five output pins in order to identify the time slot being processed. Receive Serial Fractional DS1/E1 Output These pins can be used to output fractional DS1/E1 payload data within an inbound DS1/E1 frame. In this mode, terminal equipment will use either RxCHCLK or RxSERCLK to clock out fractional DS1/E1 payload data.
RxCHN_2/ RxCHN	32	O	Receive Time Slot Octet Identifier Output-Bit 2 These output signals (RxCHN4_n through RxCHN0_n) reflect the five-bit binary value of the number of Time Slot being received and output to the Terminal Equipment via the Receive Payload Data Output Interface. The Terminal Equipment can use RxCHCLK to sample these five output pins in order to identify the time slot being processed. Receive Time Slot Identifier Serial Output If RxCHN1 is configured as RxFrTD to output fractional DS1/E1 payload data, then these pins serially output the five-bit binary value of the number of the Time Slot being accepted and processed by the Transmit Payload Data Input Interface.
RxCHN_3/ Rx8KHZ	28	O	Receive Time Slot Octet Identifier Output-Bit 3 These output signals (RxCHN4_n through RxCHN0_n) reflect the five-bit binary value of the number of Time Slot being received and output to the Terminal Equipment via the Receive Payload Data Output Interface. The Terminal Equipment can use RxCHCLK to sample these five output pins in order to identify the time slot being processed. Receive 8KHz Clock Output These pins can output a reference 8KHz clock signal if configured accordingly.

RECEIVE SERIAL DATA OUTPUT

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxCHN_4/ RxSCLK	27	O	Receive Time Slot Octet Identifier Output-Bit 4 These output signals (RxCHN4_n through RxCHN0_n) reflect the five-bit binary value of the number of Time Slot being received and output to the Terminal Equipment via the Receive Payload Data Output Interface. The Terminal Equipment can use RxCHCLK to sample these five output pins in order to identify the time slot being processed. Receive Recovered Line Clock Output These pins output the recovered T1/E1 line clock (1.544MHz and 2.048MHz) for each channel in the High-Speed modes of operation.
RxCHCLK	38	O	Receive Channel Clock Output This pin indicates the boundary of each time slot of an outbound DS1/E1 frame. DS1/E1 Mode Each of these output pins is 192kHz/256kHz clock for DS1/E1 respectively which pulses "High" whenever the Receive Payload Data Input Interface block outputs the LSB of each of the 24/32 time slots. The Terminal Equipment can use this clock signal to sample the RxCHN0 through RxCHN4 time slot identifier pins. DS1/E1 Fractional Interface Clock In the fractional interface mode, RxCHCLK can be configured to function as one of the following: The pin will output a gapped fractional clock that can be used by terminal equipment to output fractional payload data using the rising edge of the clock. Otherwise, the fractional payload data is clocked out of the chip using the un-gapped RxSERCLK pin.

RECEIVE LINE INTERFACE

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RTIP	14	I	Receive Positive Analog Input RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side).
RRING	13	I	Receive Negative Analog Input RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side).