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GENERAL DESCRIPTION

The XRT86VL34 is a four-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy). The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VL34 provides protection from power failures and hot swapping.

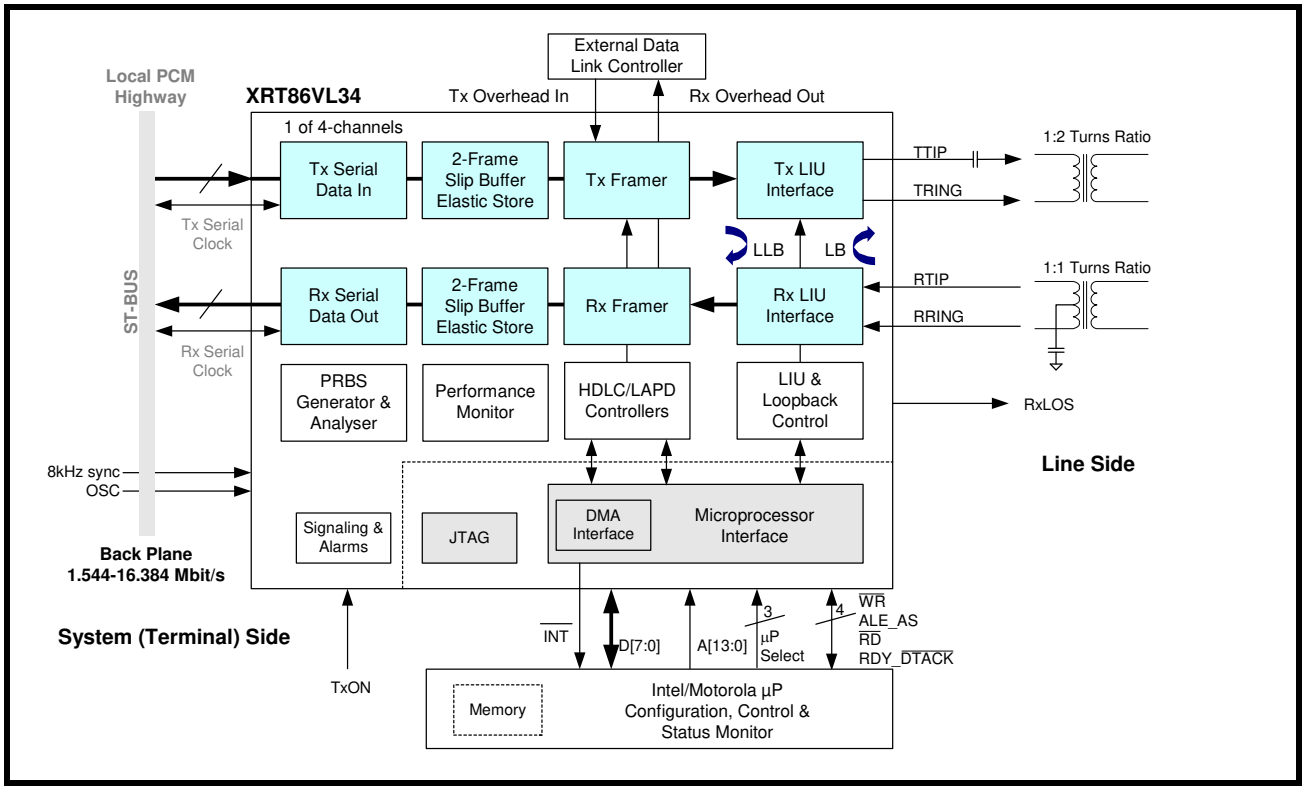
The XRT86VL34 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VL34 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VL34 4-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Four independent, full duplex DS1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers per channel for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.

- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core
- 3.3V CMOS operation with 5V tolerant inputs
- 225-pin PBGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL34IB	225 Plastic Ball Grid Array	-40°C to +85°C

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DESCRIPTION OF THE CONTROL REGISTERS - T1 MODE

All address on this register description is shown in HEX format, where n indicates channels 0-3 in the 4-channel device.

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Control Registers (0xn100 - 0xn1FF)		
Clock and Select Register	CSR	0xn100
Line Interface Control Register	LICR	0xn101
Reserved	-	0xn102 - 0xn106
Framing Select Register	FSR	0xn107
Alarm Generation Register	AGR	0xn108
Synchronization MUX Register	SMR	0xn109
Transmit Signaling and Data Link Select Register	TSDLSR	0xn10A
Framing Control Register	FCR	0xn10B
Receive Signaling & Data Link Select Register	RSDLSR	0xn10C
Receive Signaling Change Register 0	RSCR0	0xn10D
Receive Signaling Change Register 1	RSCR1	0xn10E
Receive Signaling Change Register 2	RSCR2	0xn10F
Reserved - E1 mode only	-	0xn110 - 0xn111
Receive In-Frame Register	RIFR	0xn112
Data Link Control Register 1	DLCR1	0xn113
Transmit Data Link Byte Count Register 1	TDLBCR1	0xn114
Receive Data Link Byte Count Register 1	RDLBCR1	0xn115
Slip Buffer Control Register	SBCR	0xn116
FIFO Latency Register	FIFOLR	0xn117
DMA 0 (Write) Configuration Register	D0WCR	0xn118
DMA 1 (Read) Configuration Register	D1RCR	0xn119
Interrupt Control Register	ICR	0xn11A
LAPD Select Register	LAPDSR	0xn11B
Customer Installation Alarm Generation Register	CIAGR	0xn11C
Performance Report Control Register	PRCR	0xn11D
Gapped Clock Control Register	GCCR	0xn11E
Transmit Interface Control Register	TICR	0xn120
PRBS Control & Status - Register 0	PRBSCSR0	0xn121

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Receive Interface Control Register	RICR	0xn122
PRBS Control & Status - Register 1	PRBSCSR1	0xn123
Loopback Code Control Register	LCCR	0xn124
Transmit Loopback Code Register	TLCR	0xn125
Receive Loopback Activation Code Register	RLACR	0xn126
Receive Loopback Deactivation Code Register	RLDCR	0xn127
Defect Detection Enable Register	DDER	0xn129
Reserved - E1 mode only	-	0xn130 - 0xn13F
Transmit SPRM Control Register	TSPRMCR	0xn142
Data Link Control Register 2	DLCR2	0xn143
Transmit Data Link Byte Count Register 2	TDLBCR2	0xn144
Receive Data Link Byte Count Register 2	RDLBCR2	0xn145
Data Link Control Register 3	DLCR3	0xn153
Transmit Data Link Byte Count Register 3	TDLBCR3	0xn154
Receive Data Link Byte Count Register 3	RDLBCR3	0xn155
Device ID Register	DEVID	0xn1FE
Revision Number Register	REVID	0xn1FF
Time Slot (payload) Control (0xn300 - 0xn3FF)		
Transmit Channel Control Register 0-23	TCCR 0-23	0xn300 - 0xn317
Transmit User Code Register 0-23	TUCR 0-23	0xn320 - 0xn337
Transmit Signaling Control Register 0-23	TSCR 0-23	0xn340 - 0xn357
Receive Channel Control Register 0-23	RCCR 0-23	0xn360 - 0xn377
Receive User Code Register 0-23	RUCR 0-23	0xn380 - 0xn397
Receive Signaling Control Register 0-23	RSCR 0-23	0xn3A0 - 0xn3B7
Receive Substitution Signaling Register 0-23	RSSR 0-23	0xn3C0 - 0xn3D7
Receive Signaling Array (0xn500 - 0xn51F)		
Receive Signaling Array Register 0	RSAR0-23	0xn500 - 0xn517
LAPDn Buffer 0		
LAPD Buffer 0 Control Register	LAPDBCR0	0xn600 - 0xn660
LAPDn Buffer 1		
LAPD Buffer 1 Control Register	LAPDBCR1	0xn700 - 0xn760

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Performance Monitor		
Receive Line Code Violation Counter: MSB	RLCVCU	0xn900
Receive Line Code Violation Counter: LSB	RLCVCL	0xn901
Receive Frame Alignment Error Counter: MSB	RFAECU	0xn902
Receive Frame Alignment Error Counter: LSB	RFAECL	0xn903
Receive Severely Errored Frame Counter	RSEFC	0xn904
Receive Synchronization Bit (CRC-6) Error Counter: MSB	RSBBECU	0xn905
Receive Synchronization Bit (CRC-6) Error Counter: LSB	RSBBECL	0xn906
Reserved - E1 Mode Only		0xn907 - 0xn908
Receive Slip Counter	RSC	0xn909
Receive Loss of Frame Counter	RLFC	0xn90A
Receive Change of Frame Alignment Counter	RCOAC	0xn90B
LAPD Frame Check Sequence Error counter 1	LFCSEC1	0xn90C
PRBS bit Error Counter: MSB	PBECU	0xn90D
PRBS bit Error Counter: LSB	PBECL	0xn90E
Transmit Slip Counter	TSC	0xn90F
Excessive Zero Violation Counter: MSB	EZVCU	0xn910
Excessive Zero Violation Counter: LSB	EZVCL	0xn911
LAPD Frame Check Sequence Error counter 2	LFCSEC2	0xn91C
LAPD Frame Check Sequence Error counter 3	LFCSEC3	0xn92C
Interrupt Generation/Enable Register Address Map (0xnB00 - 0xnB41)		
Block Interrupt Status Register	BISR	0xnB00
Block Interrupt Enable Register	BIER	0xnB01
Alarm & Error Interrupt Status Register	AEISR	0xnB02
Alarm & Error Interrupt Enable Register	AEIER	0xnB03
Framer Interrupt Status Register	FISR	0xnB04
Framer Interrupt Enable Register	FIER	0xnB05
Data Link Status Register 1	DLSR1	0xnB06
Data Link Interrupt Enable Register 1	DLIER1	0xnB07
Slip Buffer Interrupt Status Register	SBISR	0xnB08
Slip Buffer Interrupt Enable Register	SBIER	0xnB09
Receive Loopback code Interrupt and Status Register	RLCISR	0xnB0A
Receive Loopback code Interrupt Enable Register	RLCIER	0xnB0B

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Reserved - E1 Mode Only	-	0xnB0C - 0xnB0D
Excessive Zero Status Register	EXZSR	0xnB0E
Excessive Zero Enable Register	EXZER	0xnB0F
SS7 Status Register for LAPD 1	SS7SR1	0xnB10
SS7 Enable Register for LAPD 1	SS7ER1	0xnB11
RxLOS/CRC Interrupt Status Register	RLCISR	0xnB12
RxLOS/CRC Interrupt Enable Register	RLCIER	0xnB13
Data Link Status Register 2	DLSR2	0xnB16
Data Link Interrupt Enable Register 2	DLIER2	0xnB17
SS7 Status Register for LAPD 2	SS7SR2	0xnB18
SS7 Enable Register for LAPD 2	SS7ER2	0xnB19
Data Link Status Register 3	DLSR3	0xnB26
Data Link Interrupt Enable Register 3	DLIER3	0xnB27
SS7 Status Register for LAPD 3	SS7SR3	0xnB28
SS7 Enable Register for LAPD 3	SS7ER3	0xnB29
Customer Installation Alarm Status Register	CIASR	0xnB40
Customer Installation Alarm Interrupt Enable Register	CIAIER	0xnB41
LIU Register Summary - Channel Control Registers		
LIU Channel Control Register 0	LIUCCR0	0x0Fn0
LIU Channel Control Register 1	LIUCCR1	0x0Fn1
LIU Channel Control Register 2	LIUCCR2	0x0Fn2
LIU Channel Control Register 3	LIUCCR3	0x0Fn3
LIU Channel Control Interrupt Enable Register	LIUCCIER	0x0Fn4
LIU Channel Control Status Register	LIUCCSR	0x0Fn5
LIU Channel Control Interrupt Status Register	LIUCCISR	0x0Fn6
LIU Channel Control Cable Loss Register	LIUCCCR	0x0Fn7
LIU Channel Control Arbitrary Register 1	LIUCCAR1	0x0Fn8
LIU Channel Control Arbitrary Register 2	LIUCCAR2	0x0Fn9
LIU Channel Control Arbitrary Register 3	LIUCCAR3	0x0FnA
LIU Channel Control Arbitrary Register 4	LIUCCAR4	0x0FnB
LIU Channel Control Arbitrary Register 5	LIUCCAR5	0x0FnC
LIU Channel Control Arbitrary Register 6	LIUCCAR6	0x0FnD
LIU Channel Control Arbitrary Register 7	LIUCCAR7	0x0FnE

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
LIU Channel Control Arbitrary Register 8	LIUCCAR8	0x0FnF
Reserved	-	0x0F80 - 0x0FDF
LIU Register Summary - Global Control Registers		
LIU Global Control Register 0	LIUGCR0	0x0FE0
LIU Global Control Register 1	LIUGCR1	0x0FE1
LIU Global Control Register 2	LIUGCR2	0x0FE2
LIU Global Control Register 3	LIUGCR3	0x0FE4
LIU Global Control Register 4	LIUGCR4	0x0FE9
LIU Global Control Register 5	LIUGCR5	0x0FEA
Reserved	-	0x0FEB - 0x0FFF

1.0 REGISTER DESCRIPTIONS - T1 MODE

All addresses in this register description are shown in HEX format, where n indicates channels 0-3 in the 4-channel device.

TABLE 2: CLOCK SELECT REGISTER(CSR) **HEX ADDRESS: 0xn100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LCV Insert	R/W	0	**Line Code Violation Insertion** This bit is used to force a Line Code Violation (LCV) on the transmit output of TTIP/TRING. A “0” to “1” transition on this bit will cause a single LCV to be inserted on the transmit output of TTIP/TRING.
6	Set T1 Mode	R/W	0	**T1 Mode select** This bit is used to program the individual channel to operate in either T1 or E1 mode. 0 = Configures the selected channel to operate in E1 mode. 1 = Configures the selected channel to operate in T1 mode.
5	Sync All Transmit-ters to 8kHz	R/W	0	**Sync All Transmit Framers to 8kHz** This bit permits the user to configure each of the four (4) Transmit T1 Framer blocks to synchronize their “transmit output” frame alignment with the 8kHz signal that is derived from the MCLK PLL, as described below. 0 - Disables the “Sync all Transmit Framers to 8kHz” feature for all 4 channels. 1 - Enables the “Sync all Transmit Framers to 8kHz” feature for all 4 channels. ***NOTE:*** *Writing to this bit in register 0x0100 will enable this feature for all 4 channels.* ***NOTE:*** *This bit is only active if the MCLK PLL is used as the “Timing Source” for the Transmit T1 Framer” blocks. CSS[1:0] of this register allows users to select the transmit source of the framer.*
4	Clock Loss Detect	R/W	1	**Clock Loss Detect Enable/Disable Select** This bit enables a clock loss protection feature for the Framer whenever the recovered line clock is used as the timing source for the transmit section. If the LIU loses clock recovery, the Clock Distribution Block will detect this occurrence and automatically begin to use the internal clock derived from MCLK PLL as the Transmit source, until the LIU is able to regain clock recovery. 0 = Disables the clock loss protection feature. 1 = Enables the clock loss protection feature. ***NOTE:*** *This bit needs to be enabled in order to detect the clock closs detection interrupt status (address: 0xnB00, bit 5)*
3:2	Reserved	R/W	00	**Reserved**

TABLE 2: CLOCK SELECT REGISTER(CSR) **HEX ADDRESS: 0XN100**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1:0</td><td>CSS[1:0]</td><td>R/W</td><td>01</td><td>Clock Source Select
These bits select the timing source for the Transmit T1 Framer block. These bits can also determine the direction of TxSERCLK, TxSYNC, and TxMSYNC in base rate operation mode (1.544MHz Clock mode).
In Base Rate (1.544MHz Clock Mode):

<table>
<tr><th>CSS[1:0]</th><th>TRANSMIT SOURCE FOR THE TRANSMIT T1 FRAMER BLOCK</th><th>DIRECTION OF TXSERCLK</th></tr>
<tr><td>00/11</td><td>Loop Timing Mode
The recovered line clock is chosen as the timing source.</td><td>Output</td></tr>
<tr><td>01</td><td>External Timing Mode
The Transmit Serial Input Clock from the TxSERCLK_n input pin is chosen as the timing source.</td><td>Input</td></tr>
<tr><td>10</td><td>Internal Timing Mode
The MCLK PLL is chosen as the timing source.</td><td>Output</td></tr>
</table>
NOTE: TxSYNC/TxMSYNC can be programmed as input or output depending on the setting of SYNC INV bit in Register Address 0xn109, bit 4. Please see Register Description for the Synchronization Mux Register (SMR - 0xn109) Table 8.
NOTES: In High-Speed or multiplexed modes, TxSERCLK, TxSYNC, and TxMSYNC are all configured as INPUTS only.</td></tr>
</table>

TABLE 3: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FORCE_LOS	R/W	0	**Force Transmit LOS (To the Line Side)** This bit permits the user to configure the transmit direction circuitry (within the channel) to transmit the LOS pattern to the remote terminal equipment, as described below. 0 - Configures the transmit direction circuitry to transmit “normal” traffic. 1 - Configures the transmit direction circuitry to transmit the LOS Pattern.
6	SR	R/W	0	**Single Rail Mode** This bit can only be set if the LIU Block is also set to single rail mode. See Register 0x0FE0, bit 7. 0 - Dual Rail 1 - Single Rail
5:4	LB[1:0]	R/W	00	**Framer Loopback Selection** These bits are used to select any of the following loop-back modes for the framer section. For LIU loopback modes, see the LIU configuration registers.
3:2	Reserved	R/W	0	**Reserved**

LB[1:0]	TYPES OF LOOPBACK SELECTED
00	Normal Mode (No LoopBack)
01	**Framer Local LoopBack:** When framer local loopback is enabled, the transmit PCM input data is looped back to the receive PCM output data. The receive input data at RTIP/RRING is ignored while an All Ones Signal is transmitted out to the line interface.
10	**Framer Far-End (Remote) Line LoopBack:** When framer remote loopback is enabled, the digital data enters the framer interface, however does not enter the framing blocks. The receive digital data from the LIU is allowed to pass through the LIU Decoder/ Encoder circuitry before returning to the line interface.
11	**Framer Payload LoopBack:** When framer payload loopback is enabled, the raw data within the receive time slots are looped back to the transmit framer block where the data is re-framed according to the transmit timing.

TABLE 3: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Encode B8ZS	R/W	0	**Encode AMI or B8ZS/HDB3 Line Code Select** This bit enables or disables the B8ZS/HDB3 encoder on the transmit path. 0 = Enables the B8ZS encoder. 1 = Disables the B8ZS encoder. ***NOTE:*** *When B8ZS encoder is disabled, AMI line code is used.*
0	Decode AMI/B8ZS	R/W	0	**Decode AMI or B8ZS/HDB3 Line Code Select** This bit enables or disables the B8ZS/HDB3 decoder on the receive path. 0 = Enables the B8ZS decoder. 1 = Disables the B8ZS decoder. ***NOTE:*** *When B8ZS decoder is disabled, AMI line code is received.*

TABLE 4: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Signaling update on Superframe Boundaries	R/W	0	**Enable Robbed-Bit Signaling Update on Superframe Boundary on Both Transmit and Receive Direction** This bit enables or disables robbed-bit signaling update on the superframe boundary for both the transmit and receive side of the framer. **On the Receive Side:** If signaling update is enabled, signaling data on the receive side (RxSIG pin and Signaling Array Register - RSAR) will be updated on the superframe boundary, otherwise, signaling data will be updated as soon as it is received. **On the Transmit Side:** If signaling update is enabled, any signaling data changes on the transmit side will be transmitted on the superframe boundary, otherwise, signaling data will be transmitted as soon as it is changed. 0 - Disables the signaling update feature for both transmit and receive. 1 - Enables the signaling update feature for both transmit and receive.
6	Force CRC Errors	R/W	0	**Force CRC Errors (To the Line Side)** This bit permits the user to force the Transmit T1 Framer block to transmit CRC errors within the outbound T1 data-stream, as depicted below. 0 - Disables CRC error transmission on the outbound T1 stream. 1 **-** Enables CRC error transmission on the outbound T1 stream.
5	J1_MODE	R/W	0	**J1 Mode** This bit is used to configure the device in J1 mode. Once the device is configured in J1 mode, the following two changes will happen: **1.** CRC calculation is done in J1 format. The J1 CRC6 calculation is based on the actual values of all 4632 bits in a T1 multiframe including Fe bits instead of assuming all Fe bits to be a one in T1 format. **2.** Receive and Transmit Yellow Alarm signal format is interpreted per the J1 standard. (J1-SF or J1-ESF) 0 - Configures the device in T1 mode. (Default) 1 - Configures the device in J1 mode. ***NOTE:*** *Users can select between J1-SF or J1-ESF by setting this bit and the T1 Framing Mode Select Bits[2:0] (Bits 2-0 within this register).*
4	ONEONLY	R/W	0	**Allow Only One Sync Candidate** This bit is used to specify one of the synchronization criteria that the Receive T1 Framer block employs. 0 - Allows the Receive T1 Framer to select any one of the winners in the matching process when there are two or more valid synchronization patterns appear in the required time frame. 1 - Allows the Receive T1 Framer to declare success of match when there is only one candidate left in the required time frame.

TABLE 4: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	FASTSYNC	R/W	0	**Faster Sync Algorithm** This bit is used to specify one of the synchronization criteria that the Receive T1 Framer block employs. If this "Faster Sync Algorithm" is enabled, the Receive T1 Framer Block will declare synchronization earlier. The table below specifies the number of consecutive frames with correct F-bits that the T1 Receive framer must receive in order to declare "SYNC" when FASTSYNC is enabled or disabled. Framing / FastSync = 0 / FastSync = 1 ESF / 96 / 48 SF / 48 / 24 N / 48 / 24 SLC ® 96 / 48 / 24 0 - Disables FASTSYNC feature. 1 - Enables FASTSYNC feature.
2-0	FSI[2:0]	R/W	000	**T1 Framing Mode Select [2:0]** These three bits permit the user to select the exact T1 framing format that the channel is to operate in. Bit 2 is MSB and Bit 0 is LSB. The following table shows the five different framing formats that can be selected by configuring these three bits accordingly. ***NOTE:*** *Changing Framing formats 'on the fly' will cause the Receive T1 Framer block to undergo a "Reframe" event.* **Framing / FS[2] / FS[1] / FS[0]** **ESF** / 0 / X / X **SF** / 1 / 0 / 1 **N** / 1 / 1 / 0 **T1DM** / 1 / 1 / 1 **SLC®96** / 1 / 0 / 0

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Yellow Alarm - One Second Rule	R/W	0	**One-Second Yellow Alarm Rule Enforcement** This bit is used to enforce the one-second yellow alarm rule according to the yellow alarm (RAI) transmission duration per the ANSI standards. **If the one second alarm rule is enforced, the following will happen:** **1.** RAI will be transmitted for at least one second for both ESF and SF. **2.** There must be a minimum of one second delay between termination of the first RAI and the initiation of a subsequent RAI. **3.** ALARM_ENB bit (see description of bit 6 of this register) controls the duration of RAI. **4.** YEL[0] & YEL[1] (see description of bits 5-4 of this register) controls the format of RAI. **If the one second alarm rule is NOT enforced, the following will happen:** **1.** RAI will be transmitted for at least one second for ESF and SF. **2.** Minimum one second delay between termination of the first RAI and the initiation of the subsequent RAI is NOT enforced. **3.** YEL[0] and YEL[1] bits (see description of bits 5-4 of this register) are used to control the duration AND the format of RAI transmission. 0 - The one-second yellow alarm rule is NOT enforced. 1 - The one-second yellow alarm rule is enforced. ***NOTE:*** *When setting this bit to '0', yellow alarm transmission will be backward compatible with the XRT86L38 device. XRT86L38 does not support the one-second yellow alarm rule.*
6	ALARM_ENB	R/W	0	**Yellow Alarm Transmission Enable** This bit is used to control the duration of yellow alarm (RAI) when the one-second yellow alarm rule is enforced (bit 7 of this register set to'1'). When the one-second yellow alarm rule is not enforced (bit 7 of this register set to'0'), the duration of the RAI is controlled by the YEL[0] and YEL[1] bits (bits 5-4 of this register). **If the one-second alarm rule is enforced:** 0 - Stop the transmission of yellow alarm (see description of bits 5-4). 1 - Start the transmission of yellow alarm (see description of bits 5-4). ***NOTE:*** *This bit has no function if the one second alarm rule is not enforced.*

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>5-4</td><td>YEL[1:0]</td><td>R/W</td><td>00</td><td>
Yellow Alarm (RAI) Duration and Format
The exact function of these bits depends on whether or not the one-second yellow alarm rule is enforced. (Bit 7 of this register). The decoding of these bits are explained in Table 6 and Table 7 below.

TABLE 6: YELLOW ALARM DURATION AND FORMAT WHEN ONE SECOND RULE IS NOT ENFORCED
<table>
<tr><th>YEL[1:0]</th><th>YELLOW ALARM DURATION AND FORMAT</th></tr>
<tr><td>00</td><td>Disable the transmission of yellow alarm</td></tr>
<tr><td>01</td><td>SF or N mode:
RAI is transmitted as bit 2 = 0 (second MSB) in all DS0 data channel.
T1DM mode:
RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte).
ESF mode:
1. If YEL[0] bit is set ’high’ for a duration shorter or equal to the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link bits (M1-M12), RAI is transmitted for 255 patterns.of 1111_1111_0000_0000 (approximately 1 second)
2. If YEL[0] bit is set ’high’ for a duration longer than the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link bits (M1-M12), RAI transmission continues until YEL[0] bit is set ’low’.
3. If YEL[0] bit forms another pulse during the RAI transmission, it resets the pattern counter and extends the RAI duration for another 255 patterns of 1111_1111_0000_0000. (approximately 1 second)</td></tr>
<tr><td>10</td><td>SF mode:
RAI is transmitted as a “1” in the Fs bit of frame 12 (This is RAI for J1 SF standard).
T1DM mode:
RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte).
ESF mode:
RAI is controlled by the duration of YEL[1] bit. This allows continuous RAI of any length.</td></tr>
<tr><td>11</td><td>SF, N, and T1DM mode:
RAI format is the same as described above when YEL[1:0] is set to’01’.
ESF mode:
RAI duration is the same as described above when YEL[1:0] is set to’01’, except that format of RAI is transmitted as 255 patterns of 1111_1111_1111_1111 (sixteen ones) on the 4kbits/s data link bits instead of 255 patterns of 1111_1111_0000_0000.
NOTE: 255 patterns of 1111_1111_1111_111 is the J1 ESF RAI standard)</td></tr>
</table>
</td></tr>
</table>

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0Xn108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5-4	YEL[1:0]	R/W	00	(**Continued**)

TABLE 7: YELLOW ALARM FORMAT WHEN ONE SECOND RULE IS ENFORCED

YEL[1:0]	YELLOW ALARM FORMAT
00	Disable the transmission of yellow alarm
01	**SF or N mode**: RAI is transmitted as bit 2 = 0 (second MSB) in all DS0 data channel. **T1DM mode:** RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte). **ESF mode:** YEL[1:0] controls the format of RAI. When YEL[1:0] is set to'01', RAI is transmitted as 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12) (approximately 1 second). ALARM_ENB (Bit 6 of this register) controls the duration of RAI as described below: **1.** If ALARM_ENB bit is set 'high' for a duration shorter or equal to the time required to transmit 255 pattern of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12), RAI is transmitted for 255 patterns. (approximately 1 second) **2.** If ALARM_ENB bit is set 'high' for a duration longer than the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12), RAI continues until ALARM_ENB bit is set 'low'. **3.** If ALARM_ENB forms another pulse during an alarm transmission, it resets the pattern counter and extends the RAI duration for another 255 patterns.(approximately 1 second) ***NOTE:*** *A minimum of one second delay between termination of the first RAI and the initiation of a subsequent RAI is enforced.*
10	**SF mode:** RAI is transmitted as a "1" in the Fs bit of frame 12 (This is RAI for J1 SF standard). **T1DM mode**: RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte). **ESF mode**: RAI is controlled by the duration of ALARM_ENB bit. This allows continuous RAI of any length.
11	**SF, N, and T1DM mode:** RAI format is the same as described above when YEL[1:0] is set to'01'. **ESF mode:** RAI duration is the same as described above when YEL[1:0] is set to'01', except that format of RAI is transmitted as 255 patterns of 1111_1111_1111_1111 on the 4kbits/s data link bits (J1 ESF standard) instead of 255 patterns of 1111_1111_0000_0000.

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>Transmit AIS Pattern Select[1:0]</td><td>R/W</td><td>00</td><td>Transmit AIS Pattern Select[1:0]:
These two bits permit the user to do the following.
1. To select the appropriate AIS Pattern that the Transmit T1 Framer block will transmit to the remote terminal equipment, and
2. To command (via Software Control) the Transmit T1 Framer block to transmit that particular AIS Pattern to the remote terminal equipment, as depicted below.

<table>
<tr><th>AISG[1:0]</th><th>TYPES OF AIS PATTERNS TRANSMITTED</th></tr>
<tr><td>00/10</td><td>Disable AIS Alarm Generation
The Transmit T1 Framer block will transmit “normal” T1 traffic to the remote terminal equipment.</td></tr>
<tr><td>01</td><td>Enable Unframed AIS Alarm Generation
Transmit T1 Framer block will transmit an Unframed All Ones Pattern, as an AIS Pattern.</td></tr>
<tr><td>11</td><td>Enable Framed AIS Alarm Generation
Transmit T1 Framer block will transmit a Framed, All Ones Pattern, as the AIS Pattern.</td></tr>
</table>

NOTE: For normal operation (e.g., to configure the Transmit T1 Framer block to transmit normal T1 traffic) the user should set this bit to “[X, 0]”</td></tr>
<tr><td>1-0</td><td>AIS Defect Declaration Criteria [1:0]</td><td>R/W</td><td>00</td><td>AIS Defect Declaration Criteria[1:0]:
These bits permit the user to specify the types of AIS Patterns that the Receive T1 Framer block must detect before it will declare the AIS defect condition.

<table>
<tr><th>AISD[1:0]</th><th>AIS Defect Declaration Criteria</th></tr>
<tr><td>00/10</td><td>AIS Detection Disabled
AIS Defect Condition will NOT be declared.</td></tr>
<tr><td>01</td><td>Enable Unframed and Framed AIS Alarm Detection
ReceiveT1 Framer block will detect both Unframed and Framed AIS pattern</td></tr>
<tr><td>11</td><td>Enable Framed AIS Alarm Detection
Receive T1 Framer block will detect only Framed AIS pattern</td></tr>
</table>
</td></tr>
</table>

TABLE 8: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	MFRAMEALIGN	R/W	0	**Transmit Multiframe Sync Alignment** This bit forces Transmit T1 framer block to align with the backplane multiframe boundary (TxMSYNC_n). 0 = Do not force the transmit T1 framer block to align with the TxMSYNC signal. 1 = Force the transmit T1 framer block to align with the TxMSYNC signal. ***NOTE:*** *This bit is not used in base rate (1.544MHz Clock) mode.*
5	MSYNC	R/W	O	**Transmit Super Frame Boundary** This bit provides an option to use the transmit single frame boundary (TxSYNC) as the transmit multi-frame boundary (TxMSYNC) in high speed or multiplexed modes. In 1.544MHz clock mode (base rate), the TxMSYNC is used as the transmit superframe boundary, in other clock modes (i.e. high speed or multiplexed modes), TxMSYNC is used as an input transmit clock for the backplane interface. 0 = Configures the TxSYNC as a single frame boundary. 1 = Configures the TxSYNC as a superframe boundary (TxMSYNC) in high-speed or multiplexed mode. ***NOTE:*** *This bit is not used in base rate (1.544MHz Clock) mode.*

TABLE 8: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	Transmit Frame Sync Select	R/W	0	**Transmit Frame Sync Select** This bit permits the user to configure the System-Side Terminal Equipment or the T1 Transmit Framer to dictate whenever the Transmit T1 Framer block will initiate its generation and transmission of the very next T1 frame. If the system side controls, then all of the following will be true. 1. The corresponding TxSync_n and TxMSync_n pins will function as input pins. 2. The Transmit T1 Framer block will initiate its generation of a new T1 frame whenever it samples the corresponding "TxSync_n" input pin "high" (via the TxSerClk_n input clock signal). 3. The Transmit T1 Framer block will initiate its generation of a new Multiframe whenever it samples the corresponding "TxMSync_n" input pin "high". This bit can also be used to select the direction of the transmit single frame boundary (TxSYNC) and multi-frame boundary (TxMSYNC) depending on whether TxSERCLK is chosen as the timing source for the transmit section of the framer. (CSS[1:0] = 01 in register 0xn100) **If TxSERCLK is chosen as the timing source:** 0 = Configures TxSYNC and TxMSYNC as inputs. (System Side Controls) 1 = Configures TxSYNC and TxMSYNC as outputs. (Chip Controls) **If either Recovered Line Clock, MCLK PLL is chosen as the timing source:** 0 = Configures TxSYNC and TxMSYNC as outputs. (Chip Controls) 1 = Configures TxSYNC and TxMSYNC as inputs. (System Side Controls) ***NOTE:*** *TxSERCLK is chosen as the transmit clock if CSS[1:0] of the Clock Select Register (Register Address: 0xn100) is set to b01. Recovered Clock is chosen as the transmit clock if CSS[1:0] is set to b00 or b11; Internal Clock is chosen as the transmit clock if CSS[1:0] is set to b10.*
3 - 2	Reserved	-	-	**Reserved**