Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

GENERAL DESCRIPTION

The XRT86VX38 is an eight-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and Long-haul/Short-hual LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy) and BITS Timing element. The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VX38 provides protection from power failures and hot swapping.

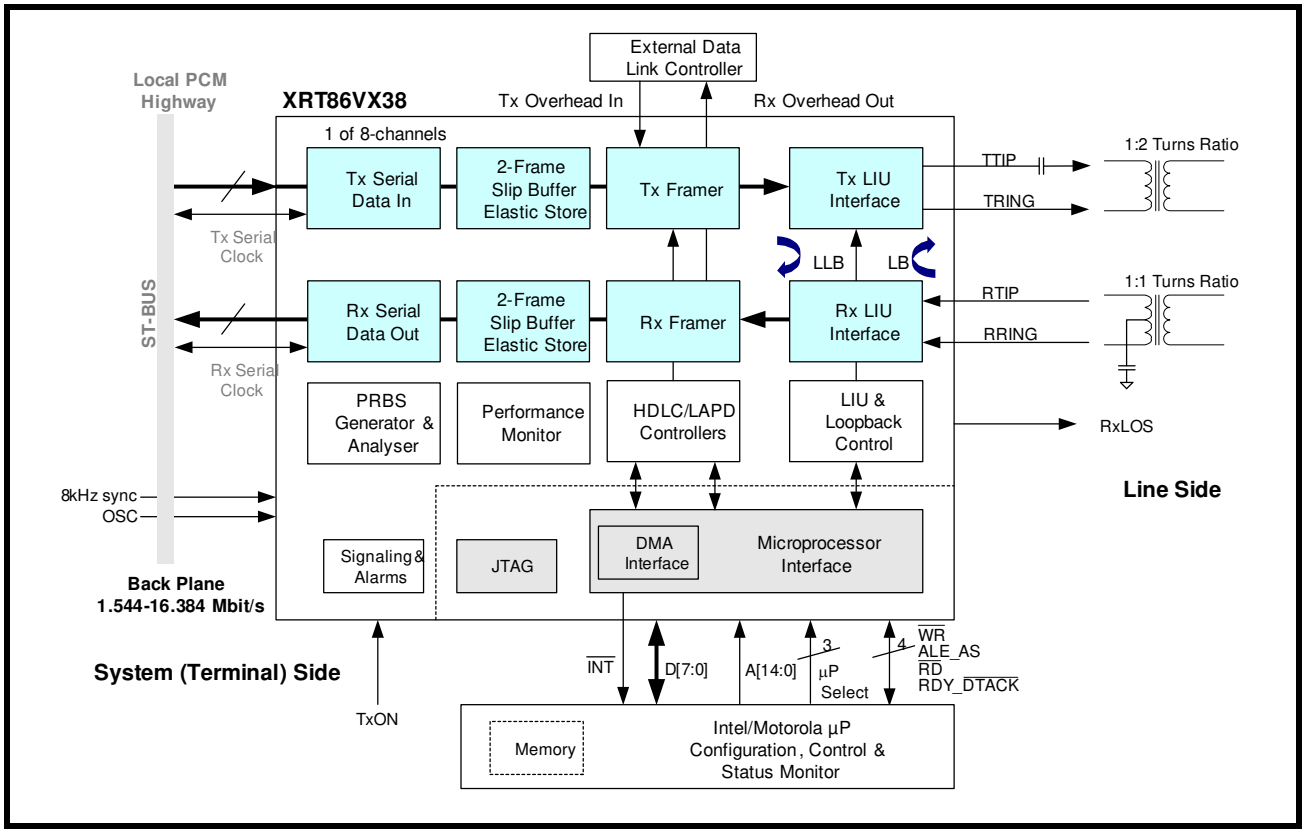
The XRT86VX38 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VX38 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VX38 8-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- BITS Timing
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Supports Section 13 - Synchronization Interface in ITU G.703 for both Transmit and Receive Paths
- Supports SSM Synchronous Messaging Generation (BOC for T1, National Bits for E1) on the Transmit Path
- Supports SSM Synchronous Messaging Extraction (BOC for T1, National Bits for E1) on the Receive Path
- Supports BITS timing generation on the Transmit Outputs
- Supports BITS timing extraction from NRZ data on the Analog Receive Path
- DS-0 Monitoring on both Transmit and Receive Time Slots
- Supports SSM Synchronization Messaging per ANSI T1.101-1999 and ITU G.704
- Supports a Customized Section 13 - Synchronization Interface in G.703 at 1.544MHz
- Independent, full duplex DS1 Tx and Rx Framer/LIUs
- Each channel has full featured Long-haul/Short-haul LIU
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 2-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling

- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Supports SPRM and NPRM
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- Full BERT Controller for generation and detection on system and line side of the chip
- PRBS, QRSS, and Network Loop Code generation and detection
- Seven Independent, simultaneous Loop Code Detectors per Channel
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- The framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core
- 3.3V CMOS operation with 5V tolerant inputs
- 256-pin fpBGA and 329-pin fpBGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VX38IB329	329 Fine Pitch Ball Grid Array	-40°C to +85°C
XRT86VX38IB256	256 Fine Pitch Ball Grid Array	-40°C to +85°C

329 BALL - FINE PITCH BALL GRID ARRAY (BOTTOM VIEW - SEE PIN LIST FOR DESCRIPTION)

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O										O	O	O	O	O	F
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	G
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	H
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	J
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	K
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	L
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	M
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	N
O	O	O	O	O										O	O	O	O	O	P
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	R
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	T
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	U
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	V
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	W

256 BALL - FINE PITCH BALL GRID ARRAY (BOTTOM VIEW - SEE PIN LIST FOR DESCRIPTION)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	F
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	G
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	H
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	J
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	K
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	L
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	M
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	N
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	P
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	R
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	T

LIST OF PARAGRAPHS

LIST OF FIGURES

LIST OF TABLES

1.0 PIN LISTS

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
A1	VDD
A2	VDDPLL18
A3	VSS
A4	DGND
A5	TDI
A6	VSS
A7	RXSIG0
A8	RXSYNC0
A9	TXSYNC0
A10	TXSIG0
A11	RXSERCLK1
A12	VDD
A13	TXSYNC1
A14	TXSER1
A15	VSS
A16	RXCASYNC2
A17	RXCRCSYNC2
A18	RxSCLK2
A19	VDD
B1	GNDPLL
B2	VDDPLL18
B3	VDDPLL18
B4	DVDD18
B5	RXTSEL
B6	VDD
B7	TMS
B8	RXLOS0
B9	VDD
B10	TXMSYNC0
B11	TXSERCLK0
B12	RXSIG1

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
B13	RXLOS1
B14	TXMSYNC1
B15	TXSIG1
B16	RXSERCLK2
B17	RXSER2
B18	TXSIG2
B19	RXSER3
C1	RTIP0
C2	RVDD0
C3	GNDPLL
C4	VDDPLL18
C5	VSS
C6	AGND
C7	aTEST
C8	MCLKIN
C9	TRST
C10	TCK
C11	RxSCLK0
C12	RXSER1
C13	RXSYNC1
C14	RXCASYNC1
C15	RXSYNC2
C16	RXSIG2
C17	TXSERCLK2
C18	TXMSYNC2
C19	RXCRCSYNC3
D1	RRING0
D2	RGND0
D3	TTIP0
D4	TVDD0
D5	GNDPLL
D6	AVDD18

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
D7	TDO
D8	RXSER0
D9	RXSERCLK0
D10	RXCRCSYNC0
D11	TXSER0
D12	RXCRCSYNC1
D13	VDD18
D14	TXSERCLK1
D15	RXLOS2
D16	TXSYNC2
D17	TXSER2
D18	RXSIG3
D19	RXCASYNC3
E1	RTIP1
E2	RVDD1
E3	TRING0
E4	TGND0
E5	ANALOG
E6	VDD18
E7	VSS
E8	VDD18
E9	VDD18
E10	RXCASYNC0
E11	VDD18
E12	VDD18
E13	VDD18
E14	RxSCLK1
E15	VDD18
E16	VDD
E17	RXSYNC3
E18	RXLOS3
E19	TXSYNC3

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
F1	RRING1
F2	VSS
F3	TTIP1
F4	TRING1
F5	VDD
F15	VDD18
F16	RXSERCLK3
F17	RxSCLK3
F18	TXSERCLK3
F19	TXSER3
G1	RVDD2
G2	RGND1
G3	TGND1
G4	TVDD1
G5	VDD18
G7	VDD18
G8	VSS
G9	VDD18
G10	VSS
G11	VDD18
G12	VSS
G13	VDD18
G15	DATA7
G16	TXMSYNC3
G17	$\overline{WR}$ / R/$\overline{W}$
G18	TXSIG3
G19	$\overline{CS}$
H1	RTIP2
H2	RGND2
H3	TRING2
H4	TTIP2
H5	VSS

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS
H12	VSS
H13	VSS
H15	ADDR12
H16	DATA6
H17	ADDR14
H18	DATA5
H19	ADDR13
J1	RRING2
J2	RVDD3
J3	TGND2
J4	TVDD2
J5	VDD18
J7	VDD18
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VDD18
J15	ADDR11
J16	ADDR9
J17	VDD
J18	$\overline{\text{INT}}$
J19	DATA4
K1	RTIP3
K2	RGND3
K3	TRING3

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
K4	TTIP3
K5	TVDD3
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VSS
K15	ADDR8
K16	DATA2
K17	ALE / $\overline{\text{AS}}$
K18	ADDR10
K19	PTYPE2
L1	RRING3
L2	RVDD4
L3	TTIP4
L4	TRING4
L5	TGND3
L7	VDD18
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L12	VSS
L13	VDD18
L15	VDD18
L16	ADDR4
L17	ADDR6
L18	DATA3
L19	ADDR7
M1	RTIP4

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
M2	RGND4
M3	TGND4
M4	TVDD4
M5	VDD18
M7	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VSS
M15	ADDR3
M16	$\overline{\text{RDY}}$ / $\overline{\text{DTACK}}$
M17	ADDR1
M18	ADDR2
M19	ADDR5
N1	RRING4
N2	RVDD5
N3	TTIP5
N4	TRING5
N5	TVDD5
N7	VDD18
N8	VSS
N9	VDD18
N10	VSS
N11	VDD18
N12	VSS
N13	VDD18
N15	VSS
N16	DATA0
N17	$\overline{\text{RD}}$ / $\overline{\text{DS}}$ / $\overline{\text{WE}}$
N18	PTYPE1

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
N19	ADDR0
P1	RTIP5
P2	VSS
P3	TGND5
P4	RVDD6
P5	TGND6
P15	VDD18
P16	VDD
P17	PTYPE0
P18	PCLK
P19	DATA1
R1	RRING5
R2	RGND5
R3	TVDD6
R4	TRING6
R5	TTIP6
R6	VSS
R7	RXCRCSYNC7
R8	TXMSYNC6
R9	VDD18
R10	VDD18
R11	VDD
R12	VDD18
R13	VDD
R14	VDD18
R15	VDD
R16	$\overline{\text{REQ1}}$
R17	RXSERCLK4
R18	VDD
R19	$\overline{\text{ACK1}}$
T1	RTIP6
T2	RGND6

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
T3	TTIP7
T4	TVDD7
T5	8KEXTOSC
T6	VDD18
T7	VDD
T8	RXSYNC7
T9	RXCASYNC7
T10	RXSYNC6
T11	TXSERCLK5
T12	RXSERCLK6
T13	TXMSYNC5
T14	RxSCLK5
T15	RXSERCLK5
T16	TXSYNC4
T17	RXSYNC4
T18	$\overline{\text{ACK0}}$
T19	$\overline{\text{REQ0}}$
U1	RRING6
U2	RVDD7
U3	TRING7
U4	VDD
U5	TXSERCLK7
U6	TXSIG7
U7	RXSERCLK7
U8	RxSCLK7
U9	RXSIG7
U10	TXSIG6
U11	RxSCLK6
U12	VSS
U13	TXSYNC5
U14	RXSYNC5
U15	RXLOS5

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
U16	TXMSYNC4
U17	RXCASYNC4
U18	RXSIG4
U19	RXLOS4
V1	VDD
V2	TGND7
V3	RGND7
V4	$\overline{\text{RESET}}$
V5	E1OSCCLK
V6	TXMSYNC7
V7	RXLOS7
V8	RXSER7
V9	TXSYNC6
V10	RXCRCSYNC6
V11	RXLOS6
V12	RXSIG6
V13	TXSER5
V14	RXSER5
V15	RXCASYNC5
V16	TXSIG4
V17	TXSERCLK4
V18	RXSER4
V19	RXCRCSYNC4
W1	VSS
W2	RTIP7
W3	RRING7
W4	TXON
W5	T1OSCCLK
W6	TXSER7
W7	TXSYNC7
W8	TXSERCLK6
W9	TXSER6

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
W10	RXCASYNC6
W11	VDD
W12	RXSER6
W13	TXSIG5
W14	RXSIG5
W15	VDD
W16	RXCRCSYNC5
W17	TXSER4
W18	RxSCLK4
W19	VSS

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
A1	GNDPLL
A2	GNDPLL
A3	VDDPLL18
A4	VDDPLL18
A5	RxTSEL
A6	TMS
A7	RXLOS0
A8	RXCRCSYNC0
A9	RXCASYNC0
A10	RXSERCLK1
A11	RXSYNC1
A12	TXMSYNC1
A13	RXSYNC2
A14	TXSYNC2
A15	RxSCLK2
A16	VDD
B1	RTIP0
B2	RVDD0
B3	VDDPLL18
B4	ANALOG
B5	AGND
B6	TDO
B7	RXSER0
B8	RXSERCLK0
B9	RXSYNC0
B10	RxSCLK0
B11	RXSER1
B12	TXSYNC1
B13	TXSERCLK1
B14	RXSER2
B15	TXSERCLK2

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
B16	RXSER3
C1	RRING0
C2	RGND0
C3	TTIP0
C4	GNDPLL
C5	AVDD18
C6	DVDD18
C7	aTEST
C8	TDI
C9	TXSYNC0
C10	RXCRCSYNC1
C11	RXLOS1
C12	TXSER1
C13	RXSERCLK2
C14	RXCRCSYNC2
C15	TXMSYNC2
C16	RXSYNC3
D1	RTIP1
D2	RVDD1
D3	TRING0
D4	TVDD0
D5	VDDPLL18
D6	DGND
D7	TRST
D8	TCK
D9	TXMSYNC0
D10	TXSERCLK0
D11	RXCASYNC1
D12	RxSCLK1
D13	RXCASYNC2
D14	TXSER2
D15	RXSERCLK3

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
D16	RXLOS3
E1	RRING1
E2	RGND1
E3	TTIP1
E4	TRING1
E5	TGND0
E6	MCLKIN
E7	VSS
E8	VDD
E9	VSS
E10	TXSER0
E11	VDD
E12	RXCRCSYNC3
E13	RXCASYNC3
E14	TXMSYNC3
E15	TXSYNC3
E16	TXSERCLK3
F1	RTIP2
F2	RVDD2
F3	TGND1
F4	TVDD1
F5	TVDD2
F6	VSS
F7	VSS
F8	VDD18
F9	VDD18
F10	VDD18
F11	RXLOS2
F12	RxSCLK3
F13	$\overline{WR}$ / R/$\overline{W}$
F14	$\overline{CS}$
F15	TXSER3

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
F16	ADDR13
G1	RRING2
G2	RGND2
G3	TTIP2
G4	TRING2
G5	TGND2
G6	VDD18
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	ADDR14
G12	DATA6
G13	DATA7
G14	DATA5
G15	VDD
G16	ADDR12
H1	RTIP3
H2	RVDD3
H3	TTIP3
H4	TRING3
H5	TVDD3
H6	VDD18
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VDD18
H12	PTYPE2
H13	DATA4
H14	ADDR10
H15	$\overline{INT}$

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
H16	ADDR11
J1	RRING3
J2	RGND3
J3	TTIP4
J4	TRING4
J5	TGND3
J6	VDD18
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VDD18
J12	DATA3
J13	ADDR9
J14	ADDR8
J15	ADDR7
J16	ALE / $\overline{AS}$
K1	RTIP4
K2	RVDD4
K3	TGND4
K4	TVDD4
K5	TVDD5
K6	VDD18
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VDD18
K12	DATA2
K13	ADDR4
K14	ADDR6
K15	ADDR2

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
K16	ADDR5
L1	RRING4
L2	RGND4
L3	TTIP5
L4	TRING5
L5	TGND5
L6	8KEXTOSC
L7	VDD18
L8	VDD18
L9	VDD18
L10	VDD18
L11	ADDR3
L12	DATA1
L13	ADDR0
L14	ADDR1
L15	$\overline{RD}$ / $\overline{DS}$ / $\overline{WE}$
L16	$\overline{RDY}$ / $\overline{DTACK}$
M1	RTIP5
M2	RVDD5
M3	TTIP6
M4	TRING6
M5	TVDD6
M6	VDD
M7	RxSCLK7
M8	RXCASYNC7
M9	VDD
M10	RXSERCLK6
M11	TXSYNC5
M12	PTYPE1
M13	PTYPE0
M14	DATA0
M15	$\overline{ACK1}$

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
M16	PCLK
N1	RRING5
N2	RGND5
N3	TGND6
N4	TVDD7
N5	TGND7
N6	TXMSYNC7
N7	RXCRCSYNC7
N8	TXSYNC6
N9	RXCASYNC6
N10	TXSERCLK5
N11	RXSYNC5
N12	TXSER4
N13	RXSYNC4
N14	VDD
N15	$\overline{ACK0}$
N16	$\overline{REQ0}$
P1	RTIP6
P2	RVDD6
P3	TTIP7
P4	TRING7
P5	TXSER7
P6	TXSERCLK7
P7	RXLOS7
P8	RXSER7
P9	RxSCLK6
P10	TXSER5
P11	RXSER5
P12	RXLOS5
P13	TXMSYNC4
P14	RXSERCLK4
P15	RXSER4

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
P16	RXLOS4
R1	RRING6
R2	RGND6
R3	RGND7
R4	$\overline{RESET}$
R5	E1OSCCLK
R6	RXSERCLK7
R7	RXSYNC7
R8	TXMSYNC6
R9	RXCRCSYNC6
R10	RXLOS6
R11	TXMSYNC5
R12	RXCASYNC5
R13	RXCRCSYNC5
R14	RXCASYNC4
R15	RXCRCSYNC4
R16	$\overline{REQ1}$
T1	RVDD7
T2	RTIP7
T3	RRING7
T4	TXON
T5	T1OSCCLK
T6	TXSYNC7
T7	TXSERCLK6
T8	TXSER6
T9	RXSYNC6
T10	RXSER6
T11	RxSCLK5
T12	RXSERCLK5
T13	TXSYNC4
T14	TXSERCLK4
T15	RxSCLK4

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
T16	VDD

2.0 PIN DESCRIPTIONS

There are six types of pins defined throughout this pin description and the corresponding symbol is presented in table below. The per-channel pin is indicated by the channel number or the letter 'n' which is appended at the end of the signal name, for example, TxSERn, where "n" indicates channels 0 to 7. All output pins are "tri-stated" upon hardware RESET.

SYMBOL	PIN TYPE
I	Input
O	Output
I/O	Bidirectional
GND	Ground
PWR	Power
NC	No Connect

The structure of the pin description is divided into eleven groups, as presented in the table below

TABLE 3: PIN DESCRIPTION STRUCTURE

SECTION	PAGE NUMBER
Transmit System Side Interface	page 13
Receive System Side Interface	page 18
Receive Line Interface	page 23
Transmit Line Interface	page 24
Timing Interface	page 25
JTAG Interface	page 26
Microprocessor Interface	page 26
Power Pins (3.3V)	page 35
Power Pins (1.8V)	page 36
Ground Pins	page 37
No Connect Pins	page 38

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSER0/ TxPOS0	D11	E10	I	-	**Transmit Serial Data Input (TxSERn)/Transmit Positive Digital Input (TxPOSn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - TxSERn** These pins function as the transmit serial data input on the system side interface, which are latched on the rising edge of the TxSERCLKn pin. Any payload data applied to this pin will be inserted into an outbound DS1/E1 frame and output to the line. In DS1 mode, the framing alignment bits, facility data link bits, CRC-6 bits, and signaling information can also be inserted from this input pin if configured appropriately. In E1 mode, all data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31 must be applied to this input pin. Data intended for Time Slots 0 and 16 can also be applied to this input pin If configured accordingly. **DS1 or E1 High-Speed Multiplexed Mode* - TxSERn** In this mode, these pins are used as the high-speed multiplexed data input pin on the system side. High-speed multiplexed data of channels 0-3 must be applied to TxSER0 and high-speed multiplexed data of channels 4-7 must be applied to TxSER4 in a byte or bit-interleaved way. The framer latches in the multiplexed data on TxSER0 and TxSER4 using TxMSYNC/TxINCLK and demultiplexes this data into 4 serial streams. The LIU block will then output the data to the line interface using TxSERCLKn. **DS1 or E1 Framer Bypass Mode - TxPOSn** In this mode, TxSERn is used for the positive digital input pin (TxPOSn) to the LIU. ***NOTE:*** 1. **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* 2. *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* 3. *These 8 pins are internally pulled "High" for each channel.*
TxSER1/ TxPOS1	A14	C12			
TxSER2/ TxPOS2	D17	D14			
TxSER3/ TxPOS3	F19	F15			
TxSER4/ TxPOS4	W17	N12			
TxSER5/ TxPOS5	V13	P10			
TxSER6/ TxPOS6	W9	T8			
TxSER7/ TxPOS7	W6	P5			

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSERCLK0/ TxLINECLK0	B11	D10	I/O	12	**Transmit Serial Clock (TxSERCLKn)/Transmit Line Clock (TxSERCLKn):** The exact function of these pins depends on the mode of operation selected, as described below. **In Base-Rate Mode (1.544MHz/2.048MHz) - TxSERCLKn:** This clock signal is used by the transmit serial interface to latch the contents on the TxSERn pins into the T1/E1 framer on the rising edge of the TxSERCLKn. These pins can be configured as input or output as described below. **When TxSERCLKn is configured as Input:** These pins will be inputs if the TxSERCLK is chosen as the timing source for the transmit framer. Users must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode. **When TxSERCLKn is configured as Output:** These pins will be outputs if either the recovered line clock or the MCLK PLL is chosen as the timing source for the T1/E1 transmit framer. The transmit framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode. **DS1/E1 High-Speed Backplane Modes* - TxSERCLKn as INPUT ONLY** In this mode, TxSERCLK is an optional clock signal input which is used as the timing source for the transmit line interface, and is only required if TxSERCLK is chosen as the timing source for the transmit framer. If TxSERCLK is chosen as the timing source, system equipment should provide 1.544MHz (For T1 mode) or 2.048MHz (For E1 mode) to the TxSERCLKn pins on each channel. TxSERCLK is not required if either the recovered clock or MCLK PLL is chosen as the timing source of the device. High speed or multiplexed data is latched into the device using the TxMSYNC/TxINCLK high-speed clock signal. **DS1 or E1 Framer Bypass Mode - TxLINECLKn** In this mode, TxSERCLKn is used as the transmit line clock (TxLINECLK) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*
TxSERCLK1/ TxLINECLK1	D14	B13			
TxSERCLK2/ TxLINECLK2	C17	B15			
TxSERCLK3/ TxLINECLK3	F18	E16			
TxSERCLK4/ TxLINECLK4	V17	T14			
TxSERCLK5/ TxLINECLK5	T11	N10			
TxSERCLK6/ TxLINECLK6	W8	T7			
TxSERCLK7/ TxLINECLK7	U5	P6			

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSYNC0/ TxNEG0 TxSYNC1/ TxNEG1 TxSYNC2/ TxNEG2 TxSYNC3/ TxNEG3 TxSYNC4/ TxNEG4 TxSYNC5/ TxNEG5 TxSYNC6/ TxNEG6 TxSYNC7/ TxNEG7	A9 A13 D16 E19 T16 U13 V9 W7	C9 B12 A14 E15 T13 M11 N8 T6	I/O	12	**Transmit Single Frame Sync Pulse (TxSYNCn) / Transmit Negative Digital Input (TxNEGn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxSYNCn:** These TxSYNCn pins are used to indicate the single frame boundary within an outbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, TxSYNCn can be configured as either input or output as described below. **When TxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. It is imperative that the TxSYNC input signal be synchronized with the TxSERCLK input signal. **When TxSYNCn is configured as an Output:** The transmit T1/E1 framer will output a signal which pulses "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - TxSYNCn as INPUT ONLY:** In this mode, TxSYNCn must be an input regardless of the clock source that is chosen to be the timing source for the transmit framer. In 2.048MVIP/4.096/8.192MHz high-speed modes, TxSYNCn pins must be pulsed 'High' for one period of TxSERCLK during the first bit of the outbound T1/E1 frame. In HMVIP mode, TxSYNC0 and TxSYNC4 must be pulsed 'High' for 4 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, TxSYNC0 and TxSYNC4 must be pulsed 'High' for 2 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - TxNEGn** In this mode, TxSYNCn is used as the negative digital input pin (TxNEG) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxMSYNC0/ TxINCLK0	B10	D9	I/O	12	**Multiframe Sync Pulse (TxMSYNCn) / Transmit Input Clock (TxINCLKn)** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxMSYNCn** In this mode, these pins are used to indicate the multi-frame boundary within an outbound DS1/E1 frame. In DS1 ESF mode, TxMSYNCn repeats every 3ms. In DS1 SF mode, TxMSYNCn repeats every 1.5ms. In E1 mode, TxMSYNCn repeats every 2ms. If TxMSYNCn is configured as an input, TxMSYNCn must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 multi-frame. It is imperative that the TxMSYNC input signal be synchronized with the TxSERCLK input signal. If TxMSYNCn is configured as an output, the transmit section of the T1/E1 framer will output and pulse TxMSYNC "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - (TxINCLKn as INPUT ONLY)** In this mode, this pin must be used as the high-speed input clock pin (TxINCLKn) for the backplane interface to latch in high-speed or multiplexed data on the TxSERn pin. The frequency of TxINCLK is presented in the table below.
TxMSYNC1/ TxINCLK1	B14	A12			
TxMSYNC2/ TxINCLK2	C18	C15			
TxMSYNC3/ TxINCLK3	G16	E14			
TxMSYNC4/ TxINCLK4	U16	P13			
TxMSYNC5/ TxINCLK5	T13	R11			
TxMSYNC6/ TxINCLK6	R8	R8			
TxMSYNC7/ TxINCLK7	V6	N6			

OPERATION MODE	FREQUENCY OF TxINCLK(MHz)
2.048MVIP non-multiplexed	2.048
4.096MHz non-multiplexed	4.096
8.192MHz non-multiplexed	8.192
12.352MHz Bit-multiplexed (DS1 ONLY)	12.352
16.384MHz Bit-multiplexed	16.384
16.384 HMVIP Byte-multiplexed	16.384
16.384 H.100 Byte-multiplexed	16.384

NOTES:

1. **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.*
2. *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*
3. *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSIG0 TxSIG1 TxSIG2 TxSIG3 TxSIG4 TxSIG5 TxSIG6 TxSIG7	A10 B15 B18 G18 V16 W13 U10 U6		I/O	8	**Transmit Time Slot Octet Identifier Output 0 (TxCHNn_0) / Transmit Serial Signaling Input (TxSIGn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled -** - No function **If transmit fractional/signaling interface is enabled - TxSIGn:** These pins can be used to input robbed-bit signaling data to be inserted within an outbound DS1 frame or to input Channel Associated Signaling (CAS) data within an outbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel must be provided on bit 4,5,6,7 of each time slot on the TxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel must be provided on bit 4, 5 of each time slot on the TxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel must be provided on bit 4 of each time slot on the TxSIG pin. **E1 Mode:** Signaling data in E1 mode can be provided on the TxSIGn pins on a time-slot-basis as in T1 mode, or it can be provided on time slot 16 only via the TxSIGn input pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSYNC0/ RxNEG0 RxSYNC1/ RxNEG1 RxSYNC2/ RxNEG2 RxSYNC3/ RxNEG3 RxSYNC4/ RxNEG4 RxSYNC5/ RxNEG5 RxSYNC6/ RxNEG6 RxSYNC7/ RxNEG7	A8 C13 C15 E17 T17 U14 T10 T8	B9 A11 A13 C16 N13 N11 T9 R7	I/O	12	**Receive Single Frame Sync Pulse (RxSYNCn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - RxSYNCn:** These RxSYNCn pins are used to indicate the single frame boundary within an inbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, RxSYNCn can be configured as either input or output depending on the slip buffer configuration as described below. **When RxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of RxSERCLK and repeats every 125μS. The receive serial Interface will output the first bit of an inbound DS1/E1 frame during the provided RxSYNC pulse. ***NOTE:*** *It is imperative that the RxSYNC input signal be synchronized with the RxSERCLK input signal.* **When RxSYNCn is configured as an Output:** The receive T1/E1 framer will output a signal which pulses "High" for one period of RxSERCLK during the first bit of an inbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - RxSYNCn as INPUT ONLY:** In this mode, RxSYNCn must be an input regardless of the slip buffer configuration. In 2.048MVIP/4.096/ 8.192MHz high-speed modes, RxSYNCn pins must be pulsed 'High' for one period of RxSERCLK during the first bit of the inbound T1/E1 frame. In HMVIP mode, RxSYNCn must be pulsed 'High' for 4 clock cycles of the RxSERCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, RxSYNCn must be pulsed 'High' for 2 clock cycles of the RxSERCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - RxNEGn** In this mode, RxSYNCn is used as the Receive negative digital output pin (RxNEG) from the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/ E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCRCSYNC0 RxCRCSYNC1 RxCRCSYNC2 RxCRCSYNC3 RxCRCSYNC4 RxCRCSYNC5 RxCRCSYNC6 RxCRCSYNC7	D10 D12 A17 C19 V19 W16 V10 R7	A8 C10 C14 E12 R15 R13 R9 N7	O	12	**Receive Multiframe Sync Pulse (RxCRCSYNCn):** The RxCRCSYNCn pins are used to indicate the receive multi-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an inbound DS1/E1 Multi-frame is being output on the RxCRCSYNCn pin. • In DS1 ESF mode, RxCRCSYNCn repeats every 3ms • In DS1 SF mode, RxCRCSYNCn repeats every 1.5ms • In E1 mode, RxCRCSYNCn repeats every 2ms.
RxCASYNC0 RxCASYNC1 RxCASYNC2 RxCASYNC3 RxCASYNC4 RxCASYNC5 RxCASYNC6 RxCASYNC7	E10 C14 A16 D19 U17 V15 W10 T9	A9 D11 D13 E13 R14 R12 N9 M8	O	12	**Receive CAS Multiframe Sync Pulse (RxCASYNCn):** **- E1 Mode Only** The RxCASYNCn pins are used to indicate the E1 CAS Multif-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an E1 CAS Multi-frame is being output on the RxCASYNCn pin.

RECEIVE SYSTEM SIDE INTERFACE

<table>
<tr><th>Signal Name</th><th>329 Pkg Ball#</th><th>256 Pkg Ball #</th><th>Type</th><th>Output Drive (mA)</th><th>Description</th></tr>
<tr><td>RxSERCLK0/ RxLINECLK0
RxSERCLK1/ RxLINECLK1
RxSERCLK2/ RxLINECLK2
RxSERCLK3/ RxLINECLK3
RxSERCLK4/ RxLINECLK4
RxSERCLK5/ RxLINECLK5
RxSERCLK6/ RxLINECLK6
RxSERCLK7/ RxLINECLK7</td><td>D9
A11
B16
F16
R17
T15
T12
U7</td><td>B8
A10
C13
D15
P14
T12
M10
R6</td><td>I/O</td><td>12</td><td>
Receive Serial Clock Signal (RxSERCLKn) / Receive Line Clock (RxLINECLKn):
The exact function of these pins depends on the mode of operation selected, as described below.
In Base-Rate Mode (1.544MHz/2.048MHz) - RxSERCLKn:
These pins are used as the receive serial clock on the system side interface which can be configured as either input or output. The receive serial interface outputs data on RxSERn on the rising edge of RxSERCLKn.
When RxSERCLKn is configured as Input:
These pins will be inputs if the slip buffer on the Receive path is enabled. System side equipment must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode.
When RxSERCLKn is configured as Output:
These pins will be outputs if slip buffer is bypassed. The receive framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode.
DS1/E1 High-Speed Backplane Modes* - (RxSERCLK as INPUT ONLY)
In this mode, this pin must be used as the high-speed input clock for the backplane interface to output high-speed or multiplexed data on the RxSERn pin. The frequency of RxSERCLK is presented in the table below.
<table>
<tr><th>Operation Mode</th><th>Frequency of RxSERCLK(MHz)</th></tr>
<tr><td>2.048MVIP non-multiplexed</td><td>2.048</td></tr>
<tr><td>4.096MHz non-multiplexed</td><td>4.096</td></tr>
<tr><td>8.192MHz non-multiplexed</td><td>8.192</td></tr>
<tr><td>12.352MHz Bit-multiplexed (DS1 ONLY)</td><td>12.352</td></tr>
<tr><td>16.384MHz Bit-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 HMVIP Byte-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 H.100 Byte-multiplexed</td><td>16.384</td></tr>
</table>
NOTES:
1. *High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.
2. For DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).
</td></tr>
</table>

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSERCLK0/ RxLINECLK0 RxSERCLK1/ RxLINECLK1 RxSERCLK2/ RxLINECLK2 RxSERCLK3/ RxLINECLK3 RxSERCLK4/ RxLINECLK4 RxSERCLK5/ RxLINECLK5 RxSERCLK6/ RxLINECLK6 RxSERCLK7/ RxLINECLK7	D9 A11 B16 F16 R17 T15 T12 U7	B8 A10 C13 D15 P14 T12 M10 R6	I/O	12	**(Continued)** **DS1 or E1 Framer Bypass Mode - RxLINECLKn** In this mode, RxSERCLKn is used as the Receive Line Clock output pin (RxLineClk) from the LIU. ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*
RxSER0/ RxPOS0 RxSER1/ RxPOS1 RxSER2/ RxPOS2 RxSER3/ RxPOS3 RxSER4/ RxPOS4 RxSER5/ RxPOS5 RxSER6/ RxPOS6 RxSER7/ RxPOS7	D8 C12 B17 B19 V18 V14 W12 V8	B7 B11 B14 B16 P15 P11 T10 P8	O	12	**Receive Serial Data Output (RxSERn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - RxSERn** These pins function as the receive serial data output on the system side interface, which are updated on the rising edge of the RxSERCLKn pin. All the framing alignment bits, facility data link bits, CRC bits, and signaling information will also be extracted to this output pin. **DS1 or E1 High-Speed Multiplexed Mode* - RxSERn** In this mode, these pins are used as the high-speed multiplexed data output pin on the system side. High-speed multiplexed data of channels 0-3 will output on RxSER0 and high-speed multiplexed data of channels 4-7 will output on RxSER4 in a byte or bit-interleaved way. The framer outputs the multiplexed data on RxSER0 and RxSER4 using the high-speed input clock (RxSERCLKn). **DS1 or E1 Framer Bypass Mode** In this mode, RxSERn is used as the positive digital output pin (RxPOSn) from the LIU. ***NOTE:*** **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSig0 RxSig1 RxSig2 RxSig3 RxSig4 RxSig5 RxSig6 RxSig7	A7 B12 C16 D18 U18 W14 V12 U9		O	8	**Receive Serial Signaling Output (RxSIGn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled :** -No function **If receive fractional/signaling interface is enabled - RxSIGn:** These pins can be used to output robbed-bit signaling data within an inbound DS1 frame or to output Channel Associated Signaling (CAS) data within an inbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel will be output on bit 4,5,6,7 of each time slot on the RxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel will be output on bit 4, 5 of each time slot on the RxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel will be output on bit 4 of each time slot on the RxSIG pin. **E1 Mode:** Signaling data in E1 mode will be output on the RxSIGn pins on a time-slot-basis as in T1 mode, or it can be output on time slot 16 only via the RxSIGn output pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 will be output on the RxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 will be output on the RxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) will be output on the RxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Receive Fractional/signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*
RxSCLK0 RxSCLK1 RxSCLK2 RxSCLK3 RxSCLK4 RxSCLK5 RxSCLK6 RxSCLK7	C11 E14 A18 F17 W18 T14 U11 U8	B10 D12 A15 F12 T15 T11 P9 M7	O	8	**Receive Recovered Line Clock Output (RxSCLKn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled -** -No function **If receive fractional/signaling interface is enabled - Receive Recovered Line Clock Output (RxSCLKn):** These pins output the recovered T1/E1 line clock (1.544MHz in T1 mode and 2.048MHz in E1 mode) for each channel. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*