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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





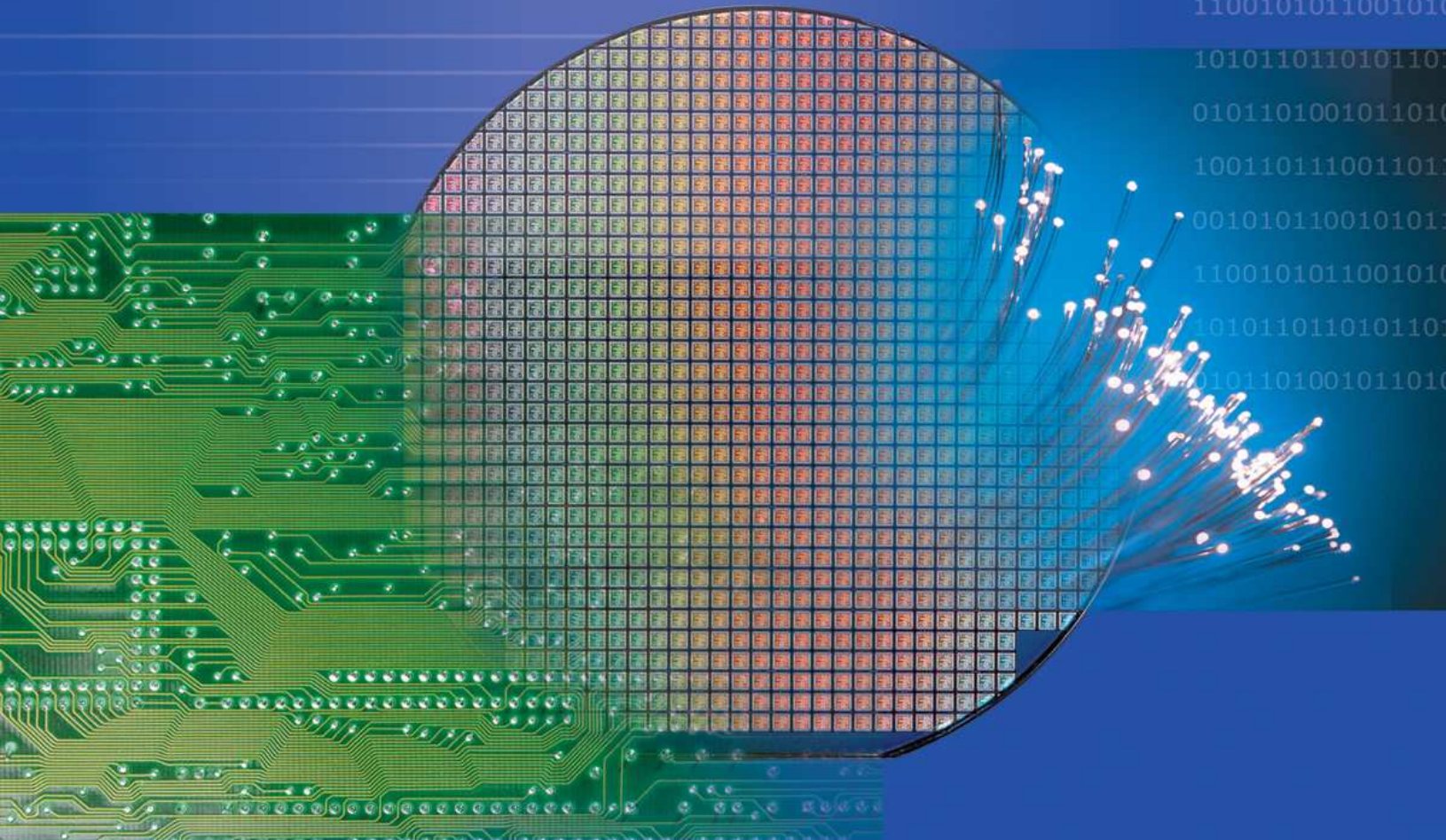
JUNE 2007

Rev. 1.0.2

XRT91L30

STS-12/STM-4 or STS-3/STM-1 SONET/SDH TRANSCEIVER

Experience *Our* Connectivity™



Network & Transmission Products

**EXAR**

**XRT91L30**

**STS-12/STM-4 OR STS-3/STM-1 SONET/SDH TRANSCEIVER**

***NOTES:***

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**STS-12/STM-4 OR STS-3/STM-1 SONET/SDH TRANSCEIVER**

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## GENERAL DESCRIPTION

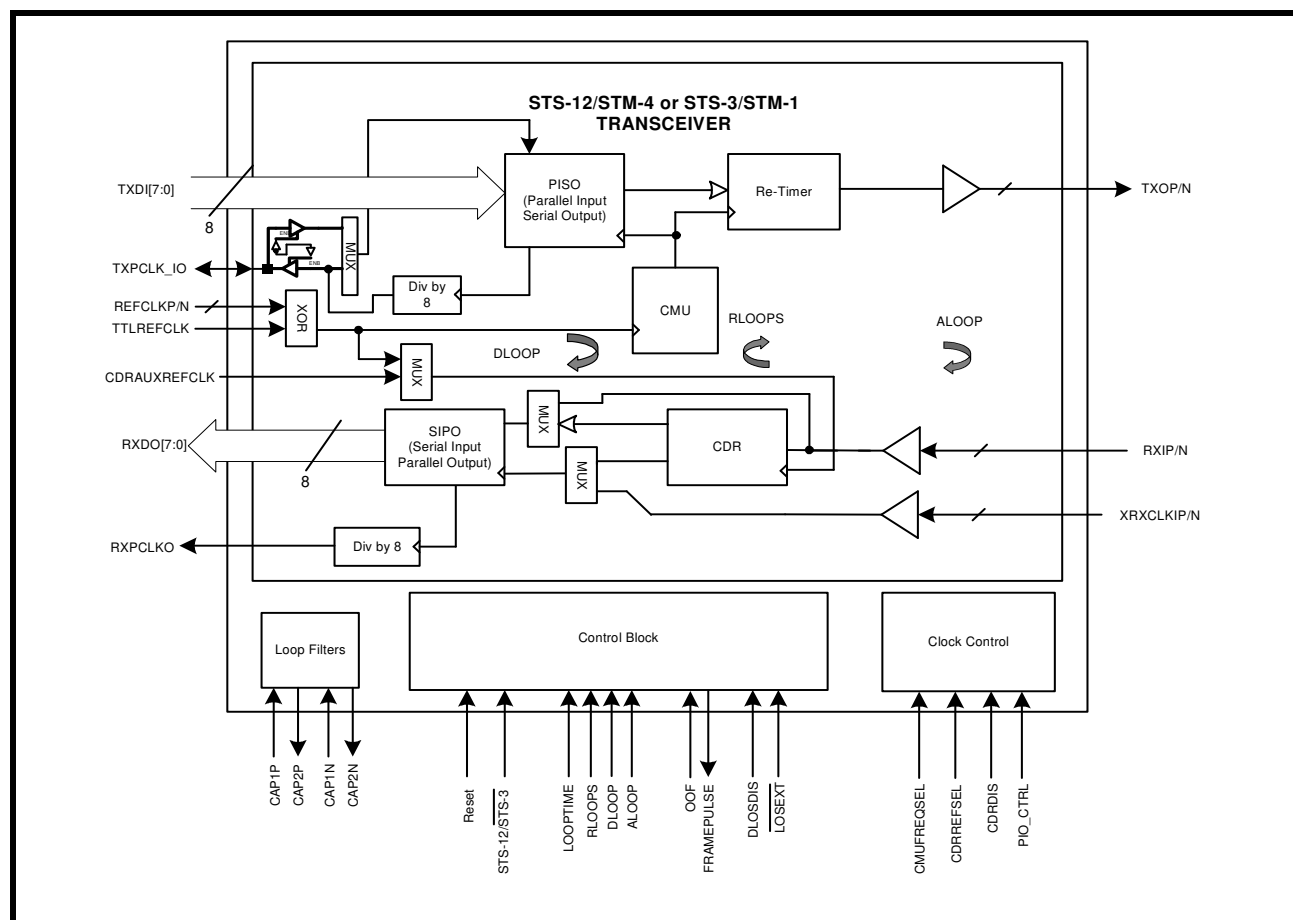
The XRT91L30 is a fully integrated SONET/SDH transceiver for SONET/SDH 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 applications. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from a slower external clock reference. It also provides Clock and Data Recovery (CDR) function by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The internal CDR unit can be disabled and bypassed in lieu of an externally recovered received clock from the optical module. Either the internally recovered clock or the externally recovered clock can be used for loop timing applications. The chip provides serial-to-parallel and parallel-to-serial converters using an 8-bit wide LVTTTL system interface in both receive and transmit directions. The transmit section includes an option to accept a parallel clock signal from the framer/mapper to

synchronize the transmit section timing. The device can internally monitor Loss of Signal (LOS) condition and automatically mute received data upon LOS. An on-chip SONET/SDH frame byte and boundary detector and frame pulse generator offers the ability recover SONET/SDH framing and to byte align the receive serial data stream into the 8-bit parallel bus.

## APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

**FIGURE 1. BLOCK DIAGRAM OF XRT91L30**

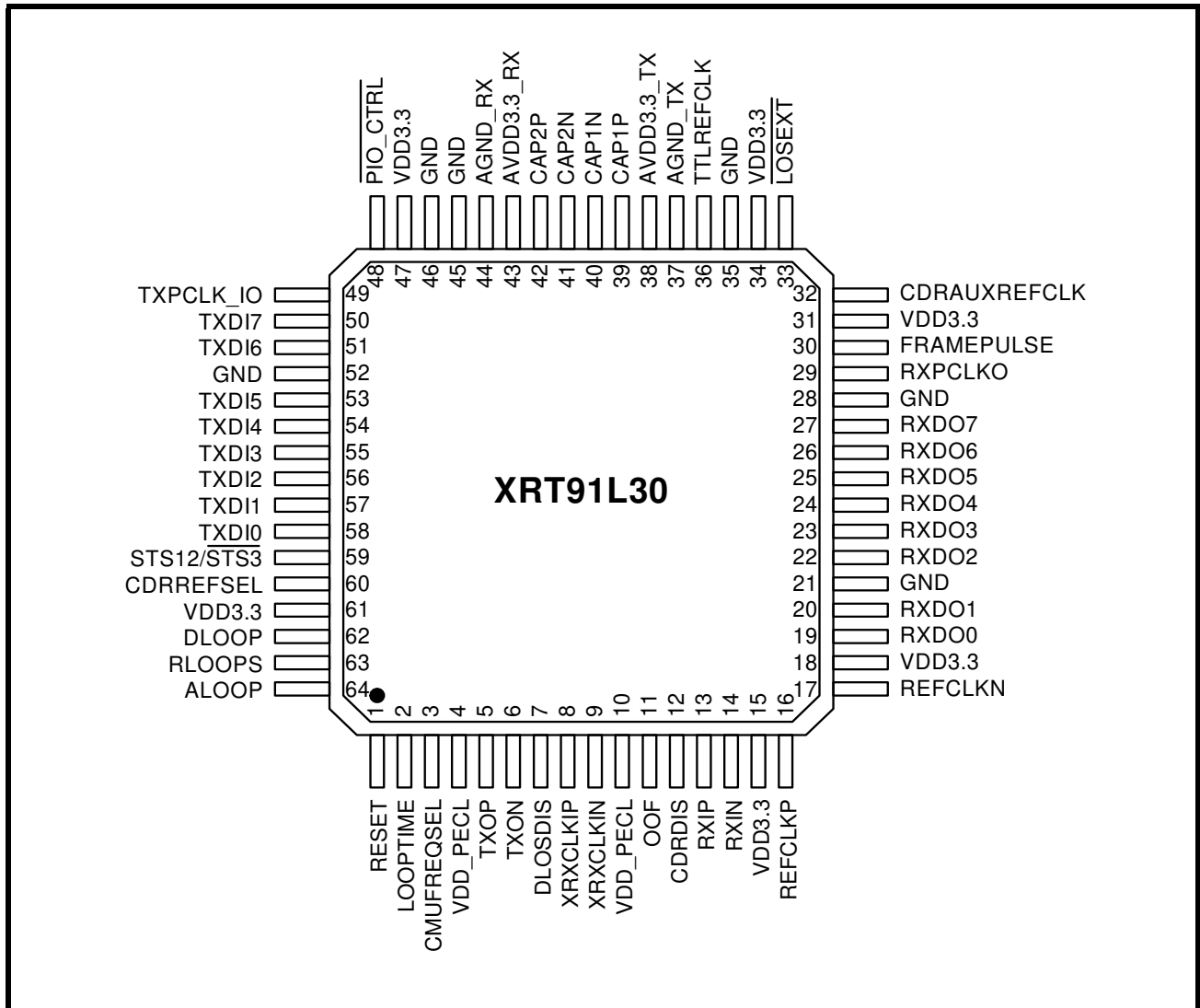




**FEATURES**

- Targeted for SONET STS-12/STS-3 and SDH STM-4/STM-1 Applications
- Selectable full duplex operation between STS-12/STM-4 standard rate of 622.08 Mbps or STS-3/STM-1 155.52 Mbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, clock data recovery (CDR) functions, and a SONET/SDH frame and byte boundary detection circuit
- Ability to disable and bypass onchip CDR for external based received reference clock recovery thru Differential LVPECL input pins XRXCLKIP/N
- 8-bit LVTTTL parallel data bus paths running at 77.76 Mbps in STS-12/STM-4 or 19.44 Mbps in STS-3/STM-1 mode of operation
- Uses Differential LVPECL or Single-Ended LVTTTL CMU reference clock frequencies of either 19.44 MHz or 77.76 MHz for both STS-12/STM-1 or STS-3/STM-1 operations
- Optional use of 77.76 MHz Single-Ended LVTTTL input for independent CDR reference clock operation
- Able to Detect and Recover SONET/SDH frame boundary and byte align received data on the parallel bus
- Diagnostics features include LOS monitoring and automatic received data mute upon LOS
- Provides Local, Remote and Split Loop-Back modes as well as Loop Timing mode
- Optional flexibility to re-configure the transmit parallel bus clock output to a clock input and accept timing signal from the framer/mapper device to permit the framer/mapper device time domain to be synchronized with the transceiver transmit timing.
- Meets Telcordia, ANSI and ITU-T G.783 and G.825 SDH jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, Bellcore TR-NWT-000253 and GR-253-CORE, GR-253 ILR SONET Jitter specifications.
- Complies with ANSI/TIA/EIA-644 and IEEE P1596.3 3.3V LVDS standard, 3.3V LVPECL, and JESD 8-B LVTTTL and LVCMOS standard.
- Operates at 3.3V Core with 3.3V I/O
- Less than 660mW in STS-3/STM-1 mode or 800mW in STS-12/STM-4 mode Typical Power Dissipation
- Package: 10 x 10 x 2.0 mm 64-pin QFP

**FIGURE 2. 64 QFP PIN OUT OF THE XRT91L30 (TOP VIEW)**



### ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L30IQ	64 Pin Lead QFP	-40°C to +85°C



## STS-12/STM-4 OR STS-3/STM-1 SONET/SDH TRANSCEIVER

## PIN DESCRIPTIONS

## HARDWARE CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION																				
RESET	LVTTL, LVCMOS	I	1	<b>Master Reset Input</b> Active "High." When this pin is pulled "High" , the internal state machines are set to their default state. "Low" = Normal Operation "High" = Master Hardware Reset (100nS minimum)																				
STS12/STS3	LVTTL, LVCMOS	I	59	<b>Data Rate Selection</b> Selects SONET/SDH transmission and reception speed rate "Low" = STS-3/STM-1 155.52 Mbps "High" = STS-12/STM-4 622.08 Mbps																				
CMUFREQSEL	LVTTL, LVCMOS	I	3	<b>Clock Multiplier Unit Reference Frequency Select</b> This pin is used to select the frequency of the REFCLKP/N or TTLREFCLK input to the CMU. "Low" = 77.76 MHz reference clock "High" = 19.44 MHz reference clock  <b>TABLE 1:</b> <table><tr><th>CMU-FREQSEL</th><th>STS12/ STS3</th><th>REFCLKP/N OR TTLREFCLK REFERENCE FREQUENCY</th><th>DATA RATE</th></tr><tr><td>0</td><td>0</td><td>77.76 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr><tr><td>0</td><td>1</td><td>77.76 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr><tr><td>1</td><td>0</td><td>19.44 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr><tr><td>1</td><td>1</td><td>19.44 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr></table> <b>NOTE:</b> REFCLKP/N or TTLREFCLK input should be generated from an LVPECL/LVTTL crystal oscillator which has a frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems..	CMU-FREQSEL	STS12/ STS3	REFCLKP/N OR TTLREFCLK REFERENCE FREQUENCY	DATA RATE	0	0	77.76 MHz	STS-3/STM-1 155.52 Mbps	0	1	77.76 MHz	STS-12/STM-4 622.08 Mbps	1	0	19.44 MHz	STS-3/STM-1 155.52 Mbps	1	1	19.44 MHz	STS-12/STM-4 622.08 Mbps
CMU-FREQSEL	STS12/ STS3	REFCLKP/N OR TTLREFCLK REFERENCE FREQUENCY	DATA RATE																					
0	0	77.76 MHz	STS-3/STM-1 155.52 Mbps																					
0	1	77.76 MHz	STS-12/STM-4 622.08 Mbps																					
1	0	19.44 MHz	STS-3/STM-1 155.52 Mbps																					
1	1	19.44 MHz	STS-12/STM-4 622.08 Mbps																					

NAME	LEVEL	TYPE	PIN	DESCRIPTION																
CDRREFSEL	LVTTL, LVCMOS	I	60	<p><b>Clock and Data Recover Unit Reference Frequency Select</b></p> <p>Selects the Clock and Data Recovery Unit reference frequency based on the table below.</p> <p>"Low" = CDR uses CMU's reference clock</p> <p>"High" = CDR reference clock from CDRAUXREFCLK</p> <table><tr><th>CDRREFSEL</th><th>STS12/ STS3</th><th>CDRAUXREFCLK FREQUENCY</th><th>DATA RATE</th></tr><tr><td>0</td><td colspan="3">CDR uses CMU's reference clock (see CMUFREQSEL pin)</td></tr><tr><td>1</td><td>0</td><td>77.76 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr><tr><td>1</td><td>1</td><td>77.76 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr></table> <p><b>NOTE:</b> CDRAUXREFCLK requires accuracy of 77.76 MHz +/- 500ppm.</p>	CDRREFSEL	STS12/ STS3	CDRAUXREFCLK FREQUENCY	DATA RATE	0	CDR uses CMU's reference clock (see CMUFREQSEL pin)			1	0	77.76 MHz	STS-3/STM-1 155.52 Mbps	1	1	77.76 MHz	STS-12/STM-4 622.08 Mbps
CDRREFSEL	STS12/ STS3	CDRAUXREFCLK FREQUENCY	DATA RATE																	
0	CDR uses CMU's reference clock (see CMUFREQSEL pin)																			
1	0	77.76 MHz	STS-3/STM-1 155.52 Mbps																	
1	1	77.76 MHz	STS-12/STM-4 622.08 Mbps																	
LOOPTIME	LVTTL, LVCMOS	I	2	<p><b>Loop Timing Mode</b></p> <p>When the loop timing mode is activated the external reference clock to the input of the Retimer is replaced with the high-speed recovered receive clock from the CDR.</p> <p>"Low" = Disabled</p> <p>"High" = Loop timing Activated</p>																
CDRDIS	LVTTL, LVCMOS	I	12	<p><b>Clock and Data Recovery Unit Disable</b></p> <p>Active "High." Disables internal Clock and Data Recovery unit. Received serial data bypasses the integrated CDR block. RXINP/N is then sampled on the rising edge of externally recovered differential clock XRXCLKIP/N coming from the optical module.</p> <p>"Low" = Internal CDR unit is Enabled</p> <p>"High" = Internal CDR unit is Disabled and Bypassed</p>																
PIO_CTRL	LVTTL, LVCMOS	I	48	<p><b>Transmit Parallel Clock Directional Control</b></p> <p><b>Transmit Parallel Clock Output Operation</b></p> <p>If this pin is asserted "High", TXPCLK_IO is a parallel bus clock output. Data on the TXDI[7:0] must be synchronously applied prior to the sampling by the PISO at the rising edge of TXPCLK_IO clock output driven by the XRT91L30.</p> <p><b>Alternate Transmit Parallel Clock Input Operation</b></p> <p>Asserting this control pin "Low" or if left unconnected, it configures TXPCLK_IO to serve as a parallel bus clock input rather than a parallel bus clock output and permits the XRT91L30 to accept the external clock input. Data on the TXDI[7:0] is then sampled at the rising edge of the TXPCLK_IO clock input driven by the framer/mapper device.</p> <p>"Low" = TXPCLK_IO is a Parallel Clock Input.</p> <p>"High" = TXPCLK_IO is a Parallel Clock Output.</p> <p><b>NOTE:</b> Parallel Clock Input operation has the advantage of permitting the framer/mapper device timing to be synchronized with the transceiver transmitter timing.</p> <p>This pin is provided with an internal pull-down.</p>																

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RLOOPS	LVTTL, LVCMOS	I	63	<b>Serial Remote Loopback</b> The serial remote loopback mode interconnects the receive serial data input to the transmit serial data output. If serial remote loopback is enabled, the 8-bit parallel transmit data input is ignored while the 8-bit parallel receive data output is maintained. "Low" = Disabled "High" = Serial Remote Loopback Mode Enabled <i><b>NOTE:</b> DLOOP and RLOOPS can be enabled simultaneously to achieve a SPLIT loopback diagnostic feature in normal operation.</i>
DLOOP	LVTTL, LVCMOS	I	62	<b>Digital Local Loopback</b> The digital local loopback mode interconnects the 8-bit parallel transmit data input and TxCLK to the 8-bit parallel receive data output and RxCLK respectively while maintaining the transmit serial data output. If digital local loopback is enabled, the receive serial data input is ignored. "Low" = Disabled "High" = Digital Local Loopback Mode Enabled <i><b>NOTE:</b> DLOOP and RLOOPS can be enabled simultaneously to achieve a SPLIT loopback diagnostic feature in normal operation.</i>
ALoop	LVTTL, LVCMOS	I	64	<b>Analog Local Loopback</b> This loopback feature serializes the 8-bit parallel transmit data input and presents the data to the transmit serial output and in addition it also internally routes the serialized data back to the Clock and Data Recovery block for serial to parallel conversion. The received serial data input is ignored. "Low" = Disabled "High" = Analog Local Loopback Mode Enabled

**TRANSMITTER SECTION**

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXDI0 TXDI1 TXDI2 TXDI3 TXDI4 TXDI5 TXDI6 TXDI7	LVTTL, LVCMOS	I	58 57 56 55 54 53 51 50	<b>Transmit Parallel Data Input</b> <b>Transmit Parallel Clock Output Operation</b> The 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel transmit data should be applied to the transmit parallel bus and simultaneously referenced to the rising edge of the TXPCLK_IO clock output. The 8-bit parallel interface is multiplexed into the transmit serial output interface with the MSB first (TXDI[7:0]).  <b>Alternate Transmit Parallel Clock Input Operation</b> When operating in this mode, TXPCLK_IO is no longer a parallel clock output reference but reverses direction and serves as the parallel transmit clock input reference for the PISO (Parallel Input to Serial Output) block. The 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel transmit data should be applied to the transmit parallel bus and simultaneously referenced to the rising edge of the TXPCLK_IO clock input.
TXOP TXON	LVPECL Diff	O	5 6	<b>Transmit Serial Data Output</b> The transmit serial data stream is generated by multiplexing the 8-bit parallel transmit data input into a 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 serial data stream.
TXPCLK_IO	LVTTL, LVCMOS	I/O	49	<b>Transmit Parallel Clock Input/Output (77.76/19.44 MHz)</b> <b>Transmit Parallel Clock Output Operation</b> When the <u>PIO_CTRL</u> pin 48 is asserted "High," this pin will output a 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock output reference for the 8-bit parallel transmit data input TXDI[7:0]. This clock is used by the framer/mapper device to present the TXDI[7:0] data which the XRT91L30 will latch on the rising edge of this clock. This enables the framer/mapper device and the XRT91L30 transceiver to be in synchronization.  <b>Alternate Transmit Parallel Clock Input Operation</b> When the <u>PIO_CTRL</u> pin 48 is asserted "Low," this pin will accept a 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock input reference for the 8-bit parallel transmit data input TXDI[7:0]. The XRT91L30 will latch data at TXDI[7:0] on the rising edge of this clock. This has the enormous advantage of enabling the framer/mapper device transmit timing to be synchronized with the transceiver transmit timing.



## TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
REFCLKP REFCLKN	LVPECL Diff	I	16 17	<p><b>Reference Clock Input (77.76 MHz or 19.44 MHz)</b></p> <p>This differential clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high speed clock reference for this device. It will accept either a 77.76 MHz or a 19.44 MHz Differential LVPECL clock source. Pin CMUFREQSEL determines the value used as the reference. See Pin CMUFREQSEL for more details. REFCLKP/N inputs are internally biased to 1.65V.</p> <p><b>NOTE:</b> In the event that TTLREFCLK LVTTTL input is used instead of these differential inputs for clock reference, the REFCLKP should be tied to ground.</p>
TTLREFCLK	LVTTTL, LVCMOS	I	36	<p><b>TTL Reference Clock Input (77.76 MHz or 19.44 MHz)</b></p> <p>This optional LVTTTL clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high speed clock reference for this device rather than a differential clock source. It will accept either a 77.76 MHz or a 19.44 MHz LVTTTL clock source. Pin CMUFREQSEL determines the value used as the reference. See Pin CMUFREQSEL for more details.</p> <p><b>NOTE:</b> In the event that REFCLKP/N differential inputs are used instead of this LVTTTL input for clock reference, the TTLREFCLK should be tied to ground.</p>

**RECEIVER SECTION**

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXDO0 RXDO1 RXDO2 RXDO3 RXDO4 RXDO5 RXDO6 RXDO7	LVTTL, LVCMOS	O	19 20 22 23 24 25 26 27	<b>Receive Parallel Data Output</b> 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel receive data output is updated simultaneously on the falling edge of the RXPCLKO output. The 8-bit parallel interface is de-multiplexed from the receive serial data input MSB first (RXDO[7]). The XRT91L30 will output the data on the falling edge of RXPCLKO clock.
RXIP RXIN	Diff LVPECL	I	13 14	<b>Receive Serial Data Input</b> The differential receive serial data stream of 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 is applied to these input pins.
XRCLKIP XRCLKIN	Diff LVPECL	I	8 9	<b>External Recovered Receive Clock Input</b> The differential receive serial data stream of 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 is sampled on the rising edge of this externally recovered differential clock coming from the optical module. It is used when the internal CDR unit is disabled and bypassed by the CDRDIS pin. <b>NOTE:</b> In the event that XRCLKIP/N differential input pins are unused, XRCLKIP should be tied to VCC with a 1k Ohm pull-up and XRCLKIN should be tied to Ground with a 1k Ohm pull-down.
RXPCLKO	LVTTL, LVCMOS	O	29	<b>Receive Parallel Clock Output (77.76 MHz or 19.44 MHz)</b> 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock output reference for the 8-bit parallel receive data output RXDO[7:0]. The parallel received data output bus will be updated on the falling edge of this clock.
CDRAUX- REFCLK	LVTTL, LVCMOS	I	32	<b>Clock and Data Recovery Auxillary Reference Clock</b> 77.76 MHz $\pm$ 500 ppm auxillary reference clock for the CDR. <b>NOTE:</b> In the event that CDRAUXREFCLK LVTTL input pin is unused, CDRAUXREFCLK should be tied to ground.
OOF	LVTTL, LVCMOS	I	11	<b>Out of Frame Input Indicator</b> This level sensitive input pin is used to initiate frame detection and byte alignment recovery when OOF is declared by the downstream device. When this pin is held High, FRAME-PULSE will pulse for a single RXPCLKO period upon the detection of every third frame alignment A2 byte in the incoming SONET/SDH Frame. "Low" = Normal Operation "High" = OOF Indication initiating frame detection and byte boundary recovery and activating FRAMEPULSE
FRAMEPULSE	LVTTL, LVCMOS	O	30	<b>Sonet Frame Alignment Pulse</b> This pin will generate a single pulse for an RXPCLKO clock period upon the detection of the third frame alignment A2 byte whenever the OOF input pin is held High. The parallel received data output bus will then be byte aligned to this newly recovered SONET/SDH frame.

## STS-12/STM-4 OR STS-3/STM-1 SONET/SDH TRANSCEIVER

NAME	LEVEL	TYPE	PIN	DESCRIPTION
CAP1P CAP2P	Analog	-	39 42	<b>CDR Non-polarized External Filter Capacitor</b> C1 = 0.47 $\mu$ F $\pm$ 10% tolerance (Isolate from noise and place close to pin)
CAP1N CAP2N	Analog	-	40 41	<b>CDR Non-polarized External Filter Capacitor</b> C2 = 0.47 $\mu$ F $\pm$ 10% tolerance (Isolate from noise and place close to pin)
DLOSDIS	LVTTL, LVCMOS	I	7	<b>LOS (Los of Signal) Detect Disable</b> Disables internal LOS monitoring and automatic muting of RXDO[7:0] upon LOS detection (according to gating shown in figure 7). LOS is declared when a string of 128 consecutive zeros occur on the line. LOS condition is cleared when the 16 or more pulse transitions is detected for 128 bit period sliding window. "Low" = Monitor and Mute received data upon LOS declaration "High" = Disable LOS monitoring (see <b>Figure 7</b> for logical operation).
$\overline{\text{LOSEXT}}$	SE-LVPECL	I	33	<b>LOS or Signal Detect Input from Optical Module</b> Active "Low." When active, this pin can force the received data output bus RXDO[7:0] to a logic state of '0' per <b>Figure 7</b> . "Low" = Forced LOS "High" = Normal Operation

## POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
VDD3.3	PWR	15, 18, 31, 34, 47, 61	<b>3.3V CMOS Power Supply</b> VDD3.3 should be isolated from the Analog VDD power supplies. Use a ferrite bead along with an internal power plane separation. The VDD3.3 power supply pins should have bypass capacitors to the nearest ground. For best results, refer to Application notes about board layout guidelines.
AVDD3.3_TX	PWR	38	<b>Analog 3.3V Transmitter Power Supply</b> AVDD3.3_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_TX power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_RX	PWR	43	<b>Analog 3.3V Receiver Power Supply</b> AVDD3.3_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_RX power supply pins should have bypass capacitors to the nearest ground.
VDD_PECL	PWR	4, 10	<b>3.3V Input/Output LVPECL Bus Power Supply</b> These pins require a 3.3V potential voltage for properly biasing the Differential LVPECL input and output pins.
AGND_TX	PWR	37	<b>Transmitter Analog Ground for 3.3V Analog Power Supplies</b> It is recommended that all ground pins of this device be tied together.

NAME	TYPE	PIN	DESCRIPTION
AGND_RX	PWR	44	<b>Receiver Analog Ground for 3.3V Analog Power Supplies</b> It is recommended that all ground pins of this device be tied together.
GND	GND	21, 28, 35, 45, 46, 52	<b>Power Supply and Thermal Ground</b> It is recommended that all ground pins of this device be tied together.



**STS-12/STM-4 OR STS-3/STM-1 SONET/SDH TRANSCEIVER****1.0 FUNCTIONAL DESCRIPTION**

The XRT91L30 transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The transceiver converts 8-bit parallel data running at 77.76 Mbps (STS-12/STM-4) or 19.44 Mbps (STS-3/STM-1) to a serial Differential LVPECL bit stream at 622.08 Mbps or 155.52 Mbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), receive clock and data recovery (CDR) unit and a SONET/SDH frame and byte boundary detection circuit. The transceiver is divided into Transmit and Receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

**1.1 STS-12/STM-4 and STS-3/STM-1 Mode of Operation**

Functionality of the transceiver can be configured by using the appropriate signal level on the STS-12/STS-3 pin. STS-3/STM-1 mode is selected by pulling STS-12/STS-3 "Low" as described in the Hardware Pin Descriptions. However, if STS-12/STM-4 mode is desired, it is selected by pulling STS-12/STS-3 "High." Therefore, the following sections describe the functionality rather than how each function is controlled. Hence, the Hardware Pin and register bit descriptions focus on device configuration.

**1.2 Clock Input Reference for Clock Multiplier (Synthesizer) Unit**

The XRT91L30 can accept both a 19.44 MHz or a 77.76 MHz Differential LVPECL clock input at REFCLKP/N or a Single-Ended LVTTTL clock at TTLREFCLK as its internal timing reference for generating higher speed clocks. The REFCLKP/N or TTLREFCLK input should be generated from an LVPECL/LVTTTL crystal oscillator which has a frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems. The reference clock can be provided with one of two frequencies chosen by CMUFREQSEL. The reference frequency options for the XRT91L30 are listed in Table 1.

**TABLE 2: CMU REFERENCE FREQUENCY OPTIONS (DIFFERENTIAL OR SINGLE-ENDED)**

CMUFREQSEL	STS12/STS3	REFCLKP/N or TTLREFCLK REFERENCE FREQUENCY	DATA RATE
0	0	77.76 MHz	STS-3/STM-1 155.52 Mbps
0	1	77.76 MHz	STS-12/STM-4 622.08 Mbps
1	0	19.44 MHz	STS-3/STM-1 155.52 Mbps
1	1	19.44 MHz	STS-12/STM-4 622.08 Mbps

**1.3 Data Latency**

Due to different operating modes and data logic paths through the device, there is an associated latency from data ingress to data egress. **Table 3** specifies the data latency for a typical path.

**TABLE 3: DATA INGRESS TO DATA EGRESS LATENCY**

MODE OF OPERATION	DATA PATH	CLOCK REFERENCE	RANGE OF CLOCK CYCLES
Thru-mode	MSB at RXIP/N to data on RXDO[7:0]	Recovered RXIP/N Clock	25 to 35
Serial Remote Loopback	MSB at RXIP/N to MSB at TXOP/N	Recovered RXIP/N Clock	2 to 4

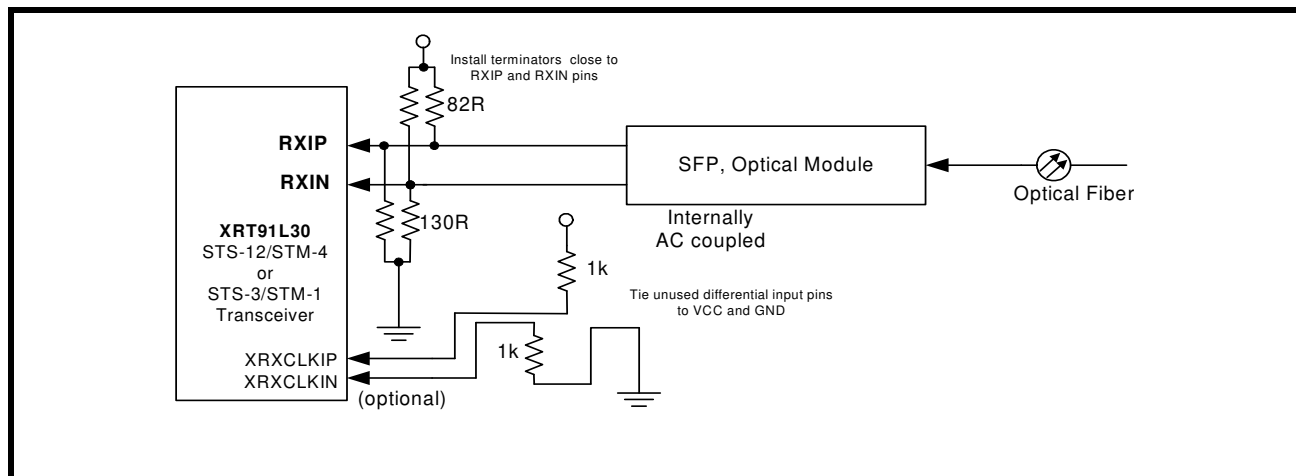
## 2.0 RECEIVE SECTION

The receive section of XRT91L30 include the inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter. The receiver accepts the high speed Non-Return to Zero (NRZ) serial data at 622.08 Mbps or 155.52 Mbps through the input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into an 8-bit-wide, 77.76 Mbps or 19.44 Mbps parallel data and presented to the RXDO[7:0] parallel interface. This parallel interface is designed for Single-Ended LVTTTL operation. A divide-by-8 version of the high-speed recovered clock RXPCLKOP/N, is used to synchronize the transfer of the 8-bit RXDO[7:0] data with the receive portion of the framer/mapper device. Upon initialization or loss of signal or loss of lock, the external reference clock signal of 19.44 MHz or 77.76 MHz is used to start-up the clock recovery phase-locked loop for proper operation. In certain applications, the CDR block on the XRT91L30 can be disabled and bypassed by enabling the CDRDIS pin to permit the flexibility of using an externally recovered receive clock thru the XRXCLKIP/N pins.

### 2.1 Receive Serial Input

The receive serial inputs are applied to RXIP/N. The receive serial inputs can be AC or DC coupled to an optical module or an electrical interface. A simplified AC coupled block diagram is shown in **Figure 3**. (Refer

**FIGURE 3. RECEIVE SERIAL INPUT INTERFACE BLOCK**

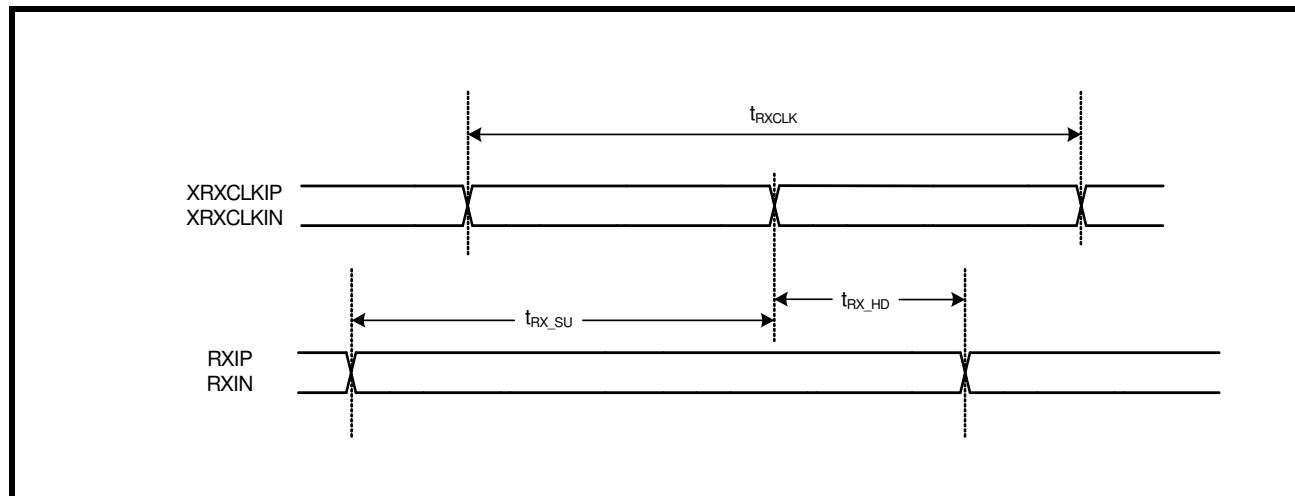


also to Application Note TAN-9130 for other line interface options)

**NOTE:** Some optical modules integrate AC coupling capacitors within the module. AC or DC coupling is largely specific to system design and optical module of choice.

**2.2 Recieve Serial Data Input Timing**

The received High-Speed Serial Differential Data Input must adhere to the set-up and hold time timing specifications below.

**FIGURE 4. RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING DIAGRAM****TABLE 4: RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING (STS-12/STM-4 OPERATION)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{RXCLK}$	Receive external recovered clock period		1.608		ns
$t_{RX\_SU}$	Serial data setup time with respect to XRXCLKIP/N	400			ps
$t_{RX\_HD}$	Serial data hold time with respect to XRXCLKIP/N	100			ps

**TABLE 5: RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING (STS-3/STM-1 OPERATION)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{RXCLK}$	Receive external recovered clock period		6.43		ns
$t_{RX\_SU}$	Serial data setup time with respect to XRXCLKIP/N	1.5			ns
$t_{RX\_HD}$	Serial data hold time with respect to XRXCLKIP/N	1.5			ns

### 2.3 Receive Clock and Data Recovery

The clock and data recovery (CDR) unit accepts the high speed NRZ serial data from the Differential LVPECL receiver and generates a clock that is the same frequency as the incoming data. The clock recovery can either utilize the transmitter's CMU reference clock from either REFCLKP/N or TTLREFCLK or it can use independent clock source CDRAUXREFCLK to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the local reference clock within  $\pm 500$  ppm. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately  $\pm 500$  ppm, the clock recovery PLL will switch and lock back onto the local reference clock. Whenever a Loss of Lock or a Loss of Signal event occurs, the CDR will continue to supply a receive clock (based on the local reference) to the framer/mapper device. When the LOSEXT is asserted by the optical module or when LOS is detected, the receive parallel data output will be forced to a logic zero state for the entire duration that a LOS condition is detected. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data. When the LOSEXT becomes inactive and the recovered clock is determined to be within  $\pm 500$  ppm accuracy with respect to the local reference source and LOS is no longer declared, the clock recovery PLL will switch and lock back onto the incoming receive data stream. **Table 6** shows Clock and Data Recovery reference clock settings. **Table 7** specifies the Clock and Data Recovery Unit performance characteristics.

**TABLE 6: CLOCK DATA RECOVERY UNIT REFERENCE CLOCK SETTINGS**

CMUFREQSEL	CDRREFSEL	STS12/ STS3	REFCLKP/N <sup>1</sup> OR TTLREFCLK <sup>1</sup> FREQUENCY (MHz)	CDRAUXREFCLK <sup>2</sup> FREQUENCY (MHz)	CDR OUTPUT FREQUENCY (MHz)
0	0	0	77.76 MHz	not used	155.52
0	0	1	77.76 MHz	not used	622.08
1	0	0	19.44 MHz	not used	155.52
1	0	1	19.44 MHz	not used	622.08
X	1	0	not referenced by CDR	77.76 MHz	155.52
X	1	1	not referenced by CDR	77.76 MHz	622.08

<sup>1</sup>Requires frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems.

<sup>2</sup>CDRAUXREFCLK requires accuracy of 77.76 MHz +/- 200ppm.

**TABLE 7: CLOCK AND DATA RECOVERY UNIT PERFORMANCE**

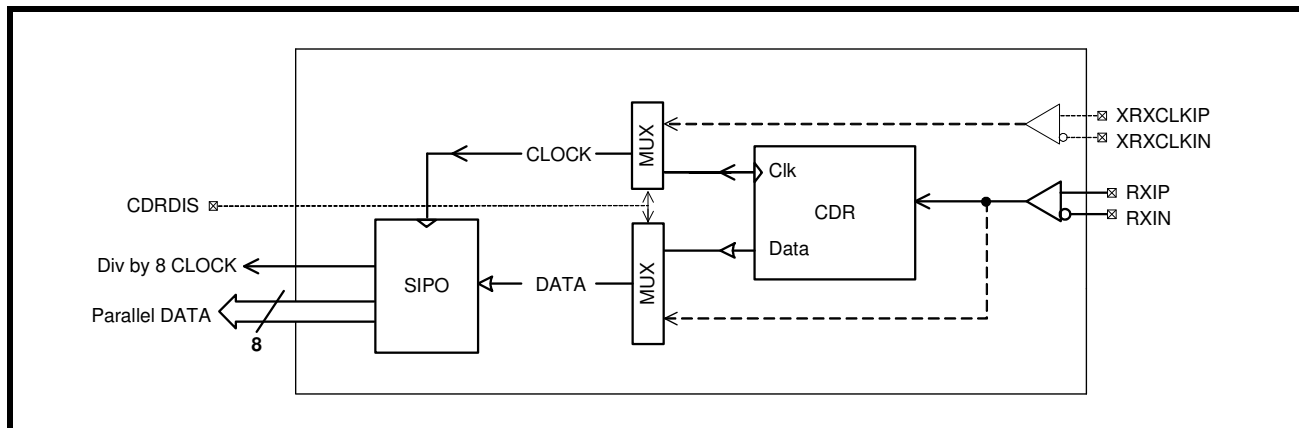
NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF <sub>DUTY</sub>	Reference clock duty cycle	40		60	%
REF <sub>TOL</sub>	Reference clock frequency tolerance	-200		+200	ppm



### 2.3.1 Internal Clock and Data Recovery Bypass

Optionally, the internal CDR unit can be disabled and bypassed in lieu of an externally recovered clock. Asserting the CDRDIS "High" disables the internal Clock and Data Recovery unit and the received serial data bypasses the integrated CDR block. RXINP/N is then sampled on the rising edge of the externally recovered differential clock XRXCLKIP/N coming from the optical module or an external clock recovery unit. **Figure 5** shows the possible internal paths of the recovered clock and data.

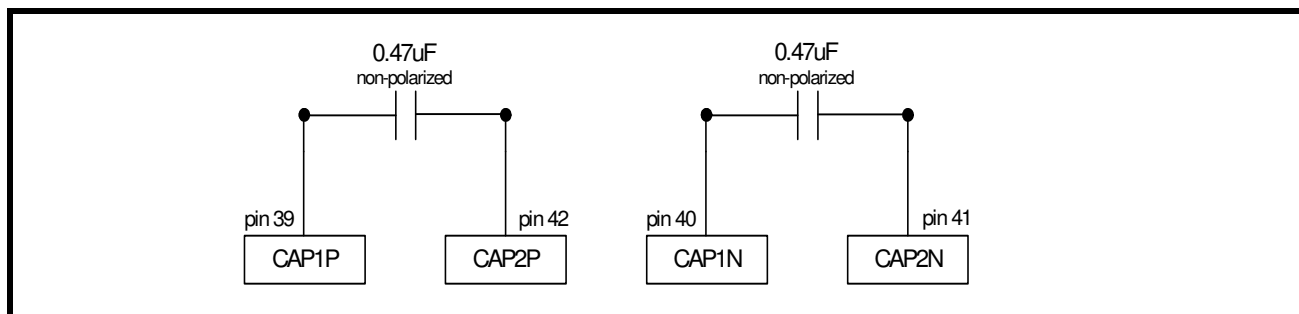
**FIGURE 5. INTERNAL CLOCK AND DATA RECOVERY BYPASS**



### 2.4 External Receive Loop Filter Capacitors

These 0.47 $\mu$ F non-polarized external loop filter capacitors provide the necessary components to achieve the required receiver jitter performance. They must be well isolated to prohibit noise entering the CDR block and should be placed as close to the pins as much as possible. **Figure 6** shows the pin connections and external loop filter components. These two non-polarized capacitors should be of +/- 10% tolerance.

**FIGURE 6. EXTERNAL LOOP FILTERS**

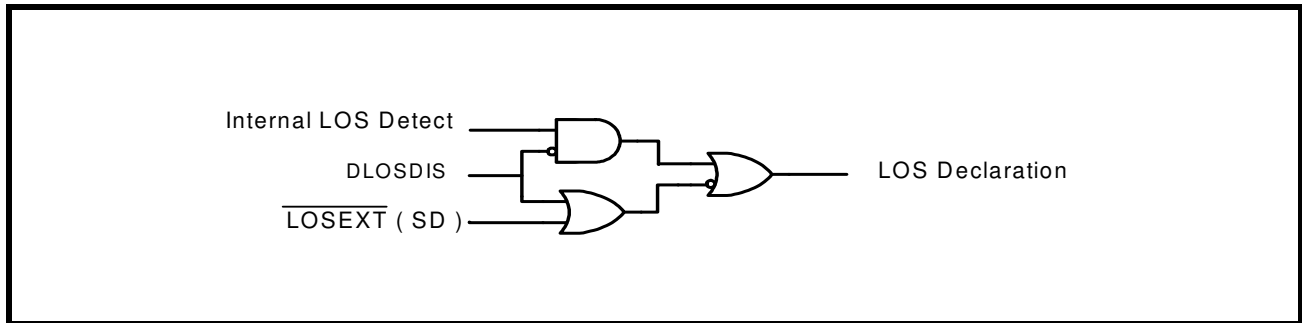


### 2.5 Loss Of Signal

XRT91L30 supports internal Loss of Signal detection (LOS) and external LOS detection. The internal Loss of Signal Detector monitors the incoming data stream and if the incoming data stream has no transition continuously for more than 128 bit periods, Loss of Signal is declared. This LOS detection will be removed when the circuit detects 16 transitions in a 128 bit period sliding window. Pulling the corresponding DLOSDIS signal to a high level will disable the internal LOS detection circuit. The external LOS function is supported by the LOSEXT input. The Single-Ended LVPECL input usually comes from the optical module through an output usually called "SD" or "FLAG" which indicates the lack or presence of optical power. Depending on the manufacturer of these devices the polarity of this signal can be either active "Low" or active "High." LOSEXT is an active "Low" signal requiring a low level to assert or invoke a forced LOS. The external LOSEXT input pin and internal LOS detector are gated to control detection and declaration of Loss of Signal (see figure 7). Whenever LOS is internally detected or an external LOS is asserted thru the LOSEXT pin, the XRT91L30 will automatically force the receive parallel data output to a logic state "0" for the entire duration that a LOS

condition is declared. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data.

**FIGURE 7. LOS DECLARATION CIRCUIT**



## 2.6 SONET Frame Boundary Detection and Byte Alignment Recovery

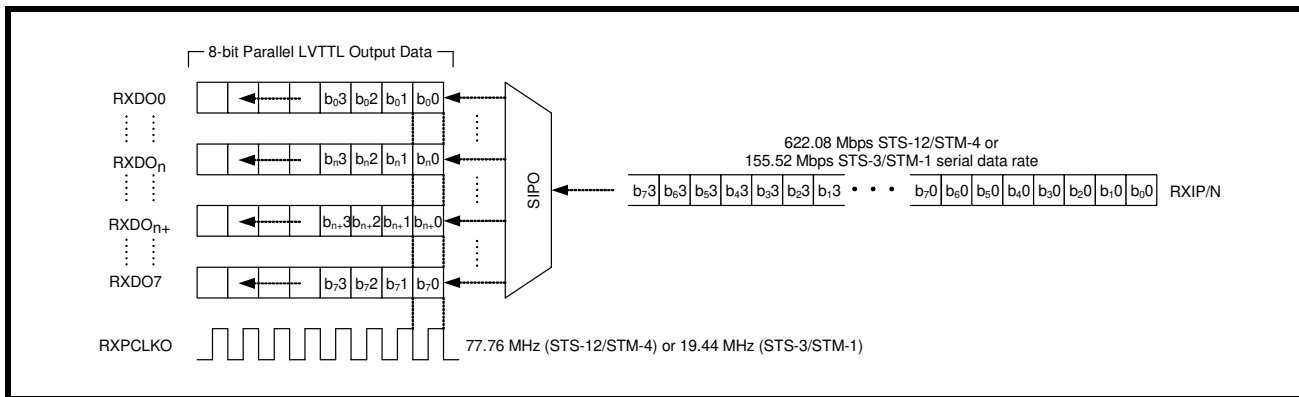
A Frame and Byte Boundary Detection circuit searches the incoming data channel for three consecutive A1 (0xF6 Hex) bytes followed by three consecutive A2 (0x28 Hex) bytes. The detector operates under the control of the OOF (Out of Frame) signals provided from the SONET Framer. Detection is enabled when OOF is held "High" and remains active until OOF goes "Low." When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming receive data stream. The receive serial-to-parallel converter block uses the located byte boundary to assemble the incoming data stream into bytes for output on the parallel data output bus RXDO[7:0]. The frame boundary is reported on the frame pulse (FRAMEPULSE) output at the onset of detecting the third A2 byte pattern when any serial 48-bit pattern matching the framing pattern is detected on the incoming data stream. While in the pattern search and detection state and so long as OOF is active, the frame pulse (FRAMEPULSE) output is activated for one byte clock cycle (RXPCLKO = 12.86 ns pulse duration for STS-12/STM-4 or 51.44 ns pulse duration for STS-3/STM-1) anytime a 48-bit pattern matching the framing pattern is detected on the incoming data stream. Once the SONET Framer Overhead Circuitry has verified that frame and byte synchronization are correct, the OOF input pin should be de-asserted by the SONET Framer to disable the XRT91L30 frame search process from trying to synchronize repeatedly and to de-activate FRAMEPULSE. When the XRT91L30's framing pattern detection is disabled upon the de-assertion of OOF input pin from the SONET Framer, the byte boundary will lock to the detected location and will remain locked to that location found when detection was previously enabled.

## 2.7 Receive Serial Input to Parallel Output (SIPO)

During STS-12/STM-4 operation, the SIPO is used to convert the 622.08 Mbps serial data input to 77.76 Mbps parallel data output which can interface to a SONET Framer/ASIC. If the XRT91L30 is operating in STS-3/STM-1, the SIPO will convert the 155.52 Mbps serial data input to 19.44 Mbps parallel data output. The SIPO

bit de-interleaves the serial data input into an 8-bit parallel output to RXDO[7:0]. A simplified block diagram is shown in **Figure 8**. XRT91L30 clocks data out on RXDO[7:0] at the falling edge of RXPCLKO.

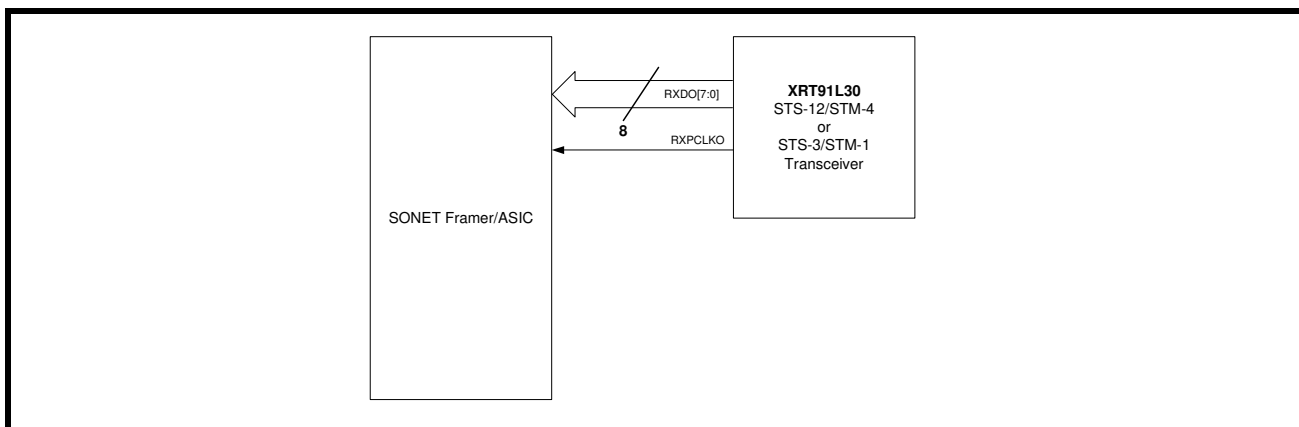
**FIGURE 8. SIMPLIFIED BLOCK DIAGRAM OF SIPO**



## 2.8 Receive Parallel Output Interface

The 8-bit Single-Ended LVTTTL running at 77.76 Mbps (STS-12/STM-4) or 19.44 Mbps (STS-3/STM-1) parallel data output of the receive path is used to interface to a SONET Framer/ASIC synchronized to the recovered clock. A simplified block diagram is shown in **Figure 9**.

**FIGURE 9. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK**



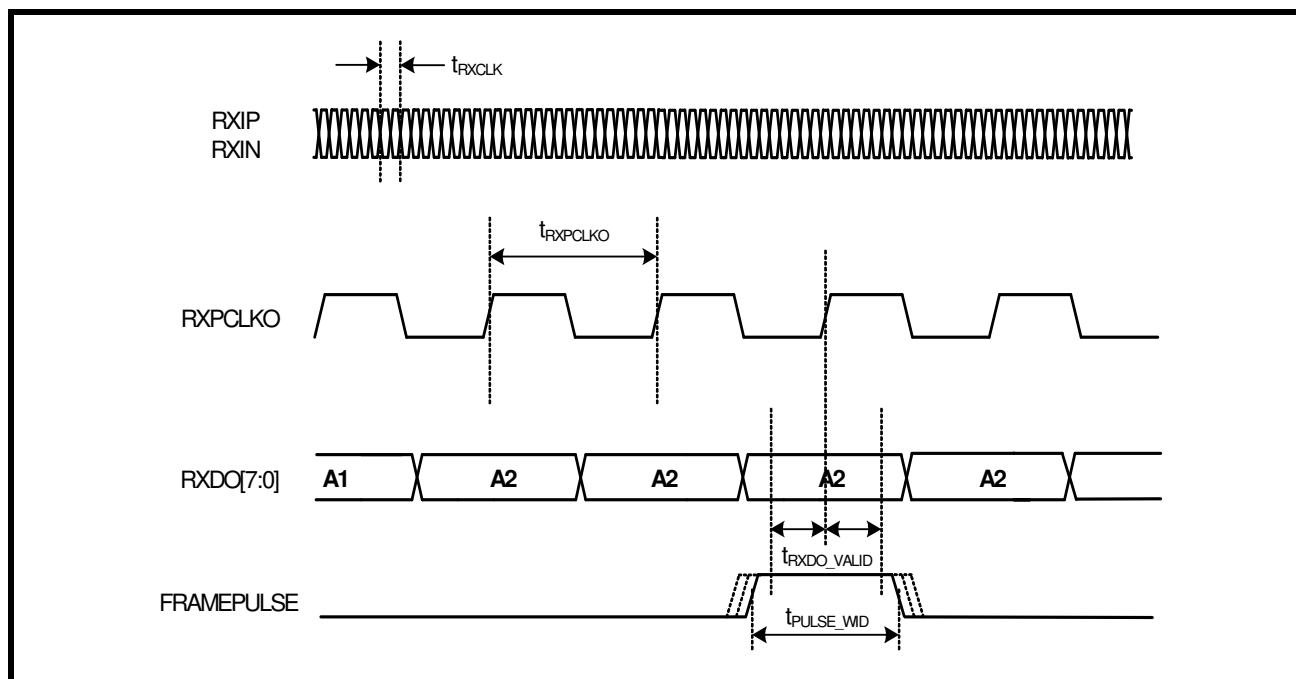
## 2.9 Disable Parallel Receive Data Output Upon LOS

The parallel receiver outputs are automatically pulled "Low" or forced to a logic state of "0" during a LOS condition to prevent data chattering unless LOS detection is disabled by asserting DLOSDIS and keeping LOSEXT input pin "high." In addition, the user can also assert LOSEXT input pin "low" from the optical module to force an LOS and mute the parallel receiver outputs as well (while DLOSDIS input is also low, see **Figure 7**).

## 2.10 Receive Parallel Data Output Timing

The receive parallel data output from the STS-12/STM-4 or STS-3/STM-1 receiver will adhere to the setup and hold times shown in **Figure 10**, **Table 8**, and **Table 9**. **Table 10** shows the PECL and TTL output timing specifications.

**FIGURE 10. RECEIVE PARALLEL OUTPUT TIMING**



**TABLE 8: RECEIVE PARALLEL DATA OUTPUT TIMING (STS-12/STM-4 OPERATION)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{RXCLK}$	Receive high-speed serial clock period		1.608		ns
$t_{RXPCLKO}$	Receive parallel data output byte clock period		12.86		ns
$t_{RXDO\_VALID}$	Time the data is valid on RXDO[7:0] and FRAMEPULSE before and after the rising edge of RXPCLKO	4			ns
$t_{PULSE\_WID}$	Pulse width of frame detection pulse on FRAMEPULSE		12.86		ns

**TABLE 9: RECEIVE PARALLEL DATA OUTPUT TIMING (STS-3/STM-1 OPERATION)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{RXCLK}$	Receive high-speed serial clock period		6.43		ns
$t_{RXPCLKO}$	Receive parallel data output byte clock period		51.44		ns
$t_{RXDO\_VALID}$	Time the data is valid on RXDO[7:0] and FRAMEPULSE before and after the rising edge of RXPCLKO	22			ns
$t_{PULSE\_WID}$	Pulse width of frame detection pulse on FRAMEPULSE		51.44		ns



**TABLE 10: PECL AND TTL RECEIVE OUTPUTS TIMING SPECIFICATION**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{R\_PECL}$	PECL output rise time (20% to 80%)		350		ps
$t_{F\_PECL}$	PECL output fall time (80% to 20%)		350		ps
$t_{R\_TTL}$	TTL output rise time (10% to 90%)		2		ns
$t_{F\_TTL}$	TTL output fall time (90% to 10%)		1.5		ns

### 3.0 TRANSMIT SECTION

The transmit section of the XRT91L30 accepts 8-bit parallel data and converts it to serial Differential LVPECL data output intended to interface to an optical module. It consists of an 8-bit parallel Single-Ended LVTTTL interface, Parallel-to-Serial Converter, a clock multiplier unit (CMU), a Low Voltage Positive-referenced Emitter-Coupled Logic (LVPECL) differential line driver, and Loop Timing modes. The LVPECL serial data output rate is 622.08 Mbps for STS-12/STM-4 applications and 155.52 Mbps for STS-3/STM-1 applications. The high frequency serial clock is synthesized by a PLL, which uses a low frequency clock as its input reference. In order to synchronize the data transfer process, the synthesized 622.08 MHz for STS-12/STM-4 or 155.52 MHz STS-3/STM-1 serial clock output is divided by eight and the 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock respectively is presented to the framer/mapper device to be used as its timing source.

#### 3.1 Transmit Parallel Input Interface

The parallel data from an framer/mapper device is presented to the XRT91L30 through an 8-bit Single-Ended LVTTTL parallel bus interface TXDI[7:0]. To directly interface to the XRT91L30, the SONET Framer/ASIC must be synchronized to the same timing source TXPCLK\_IO in presenting data on the parallel bus interface. The data must meet setup and hold times with respect to TXPCLK\_IO. This clock output source is used to synchronize the SONET Framer/ASIC to the XRT91L30. The framer/mapper device should use TXPCLK\_IO as its timing source so that parallel data is phase aligned with the serial transmit data. The data is latched into a parallel input register on the rising edge of TXPCLK\_IO. TXPCLK\_IO is derived from a divide-by-8 of the high speed synthesized clock resulting in a 77.76/ 19.44 MHz Single-Ended LVTTTL clock output source to be used by the framer/mapper device for parallel bus synchronization. A simplified block diagram of the transmit parallel bus clock output system interface is shown in **Figure 11**.

**FIGURE 11. TRANSMIT PARALLEL INPUT INTERFACE BLOCK**

