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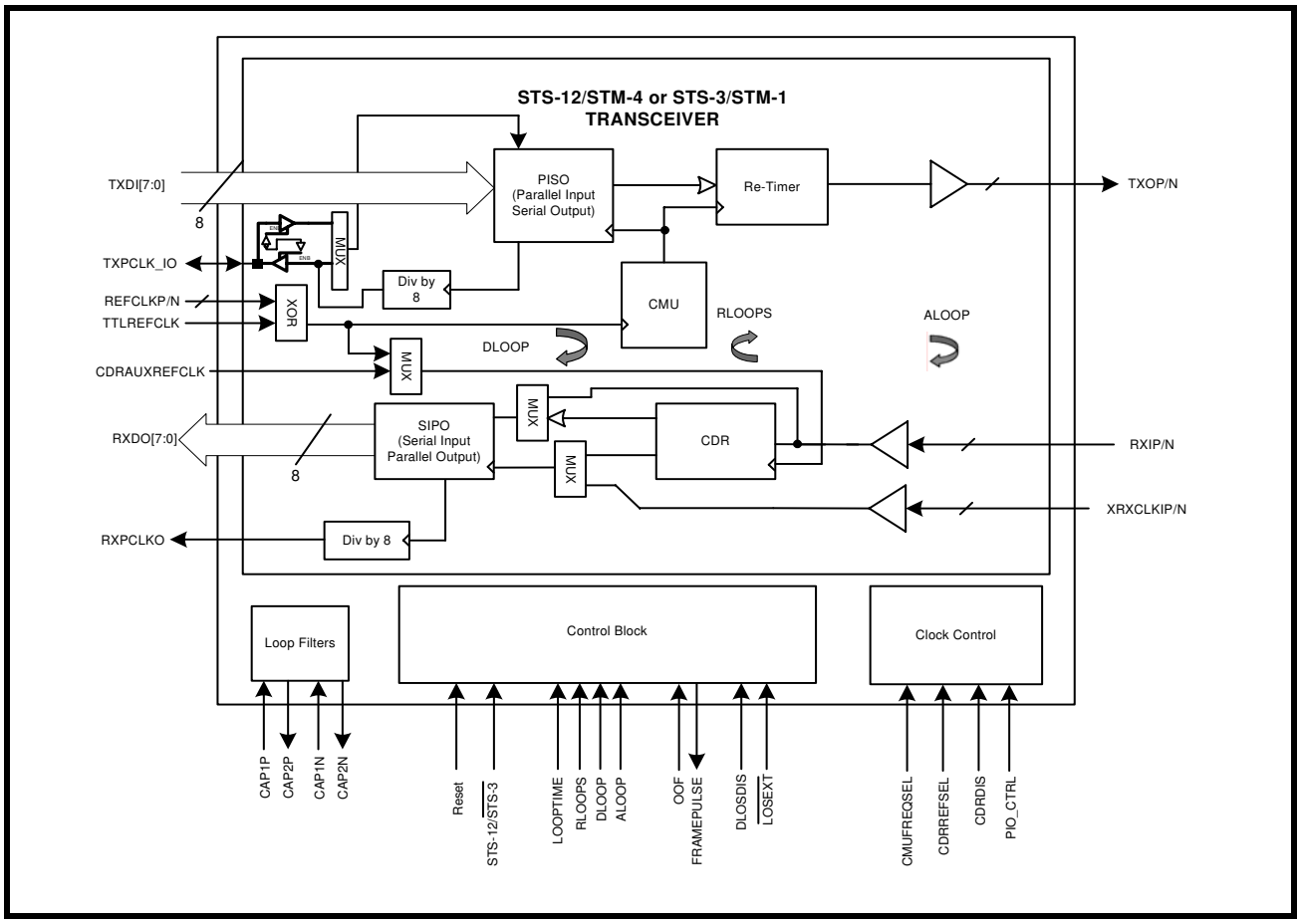
GENERAL DESCRIPTION

The XRT91L31 is a fully integrated SONET/SDH transceiver for SONET/SDH 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 applications. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from a slower external clock reference. It also provides Clock and Data Recovery (CDR) function by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The internal CDR unit can be disabled and bypassed in lieu of an externally recovered received clock from the optical module. Either the internally recovered clock or the externally recovered clock can be used for loop timing applications. The chip provides serial-to-parallel and parallel-to-serial converters using an 8-bit wide LVTTL system interface in both receive and transmit directions. The transmit section includes an option to accept a parallel clock signal from the framer/mapper to synchronize the transmit section timing. The device can internally monitor Loss of Signal (LOS) condition and automatically mute received data upon LOS. An on-chip SONET/SDH frame byte and boundary detector and frame pulse generator offers the ability recover SONET/SDH framing and to byte align the receive serial data stream into the 8-bit parallel bus.

APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

FIGURE 1. BLOCK DIAGRAM OF XRT91L31



FEATURES

- Targeted for SONET STS-12/STS-3 and SDH STM-4/STM-1 Applications
- Selectable full duplex operation between STS-12/STM-4 standard rate of 622.08 Mbps or STS-3/STM-1 155.52 Mbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, clock data recovery (CDR) functions, and a SONET/SDH frame and byte boundary detection circuit
- Ability to disable and bypass onchip CDR for external based received reference clock recovery thru Differential LVPECL input pins XRXCLKIP/N
- 8-bit LVTTL parallel data bus paths running at 77.76 Mbps in STS-12/STM-4 or 19.44 Mbps in STS-3/STM-1 mode of operation
- Uses Differential LVPECL or Single-Ended LVTTL CMU reference clock frequencies of either 19.44 MHz or 77.76 MHz for both STS-12/STM-1 or STS-3/STM-1 operations
- Optional use of 77.76 MHz Single-Ended LVTTL input for independent CDR reference clock operation
- Able to Detect and Recover SONET/SDH frame boundary and byte align received data on the parallel bus
- Diagnostics features include LOS monitoring and automatic received data mute upon LOS
- Provides Local, Remote and Split Loop-Back modes as well as Loop Timing mode
- Optional flexibility to re-configure the transmit parallel bus clock output to a clock input and accept timing signal from the framer/mapper device to permit the framer/mapper device time domain to be synchronized with the transceiver transmit timing.
- Meets Telcordia, ANSI and ITU-T G.783 and G.825 SDH jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, Bellcore TR-NWT-000253 and GR-253-CORE, GR-253 ILR SONET Jitter specifications.
- Complies with ANSI/TIA/EIA-644 and IEEE P1596.3 3.3V LVDS standard, 3.3V LVPECL, and JESD 8-B LVTTL and LVCMOS standard.
- Operates at 3.3V with 3.3V I/O
- Less than 660mW in STS-3/STM-1 mode or 800mW in STS-12/STM-4 mode Typical Power Dissipation
- Package: 10 x 10 x 2.0 mm 64-pin QFP

FIGURE 2. 64 QFP PIN OUT OF THE XRT91L31 (TOP VIEW)

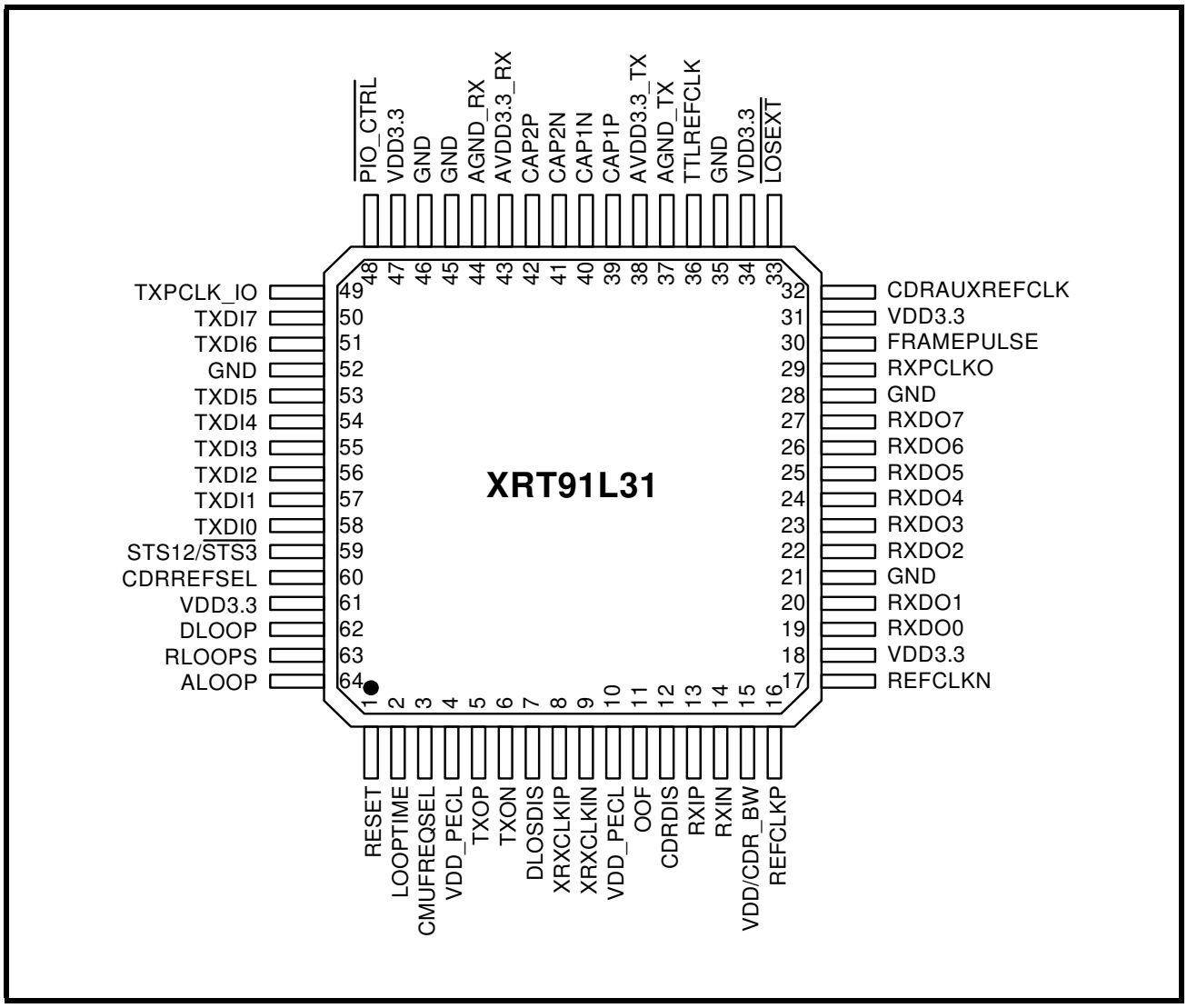


TABLE 1: ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L31IQ	64 Pin Lead QFP	-40°C to +85°C

PIN DESCRIPTIONS

TABLE 2: HARDWARE CONTROL

PIN DESCRIPTION

<table>
<tr><th>NAME</th><th>LEVEL</th><th>TYPE</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>RESET</td><td>LVTTL, LVCMOS</td><td>I</td><td>1</td><td>Master Reset Input
Active "High." When this pin is pulled "High" , the internal state machines are set to their default state.
"Low" = Normal Operation
"High" = Master Hardware Reset</td></tr>
<tr><td>STS12/$\overline{\text{STS3}}$</td><td>LVTTL, LVCMOS</td><td>I</td><td>59</td><td>Data Rate Selection
Selects SONET/SDH transmission and reception speed rate
"Low" = STS-3/STM-1 155.52 Mbps
"High" = STS-12/STM-4 622.08 Mbps</td></tr>
<tr><td>CMUFREQSEL</td><td>LVTTL, LVCMOS</td><td>I</td><td>3</td><td>Clock Multiplier Unit Reference Frequency Select
This pin is used to select the frequency of the REFCLKP/N or TTLREFCLK input to the CMU.
"Low" = 77.76 MHz reference clock
"High" = 19.44 MHz reference clock
<table>
<tr><th>CMU-FREQSEL</th><th>STS12/STS3</th><th>REFCLKP/N OR TTLREFCLK REFERENCE FREQUENCY</th><th>DATA RATE</th></tr>
<tr><td>0</td><td>0</td><td>77.76 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr>
<tr><td>0</td><td>1</td><td>77.76 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr>
<tr><td>1</td><td>0</td><td>19.44 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr>
<tr><td>1</td><td>1</td><td>19.44 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr>
</table>
NOTE: REFCLKP/N or TTLREFCLK input should be generated from an LVPECL/LVTTL crystal oscillator which has a frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems..</td></tr>
<tr><td>CDR_BW/VDD</td><td>LVTTL, LVCMOS</td><td>I</td><td>15</td><td>CDR Bandwidth Select
This pin is used to select the CDR Bandwidth
"Low" = Narrow BW, (Meets SONET jitter transfer requirement)
"High" (VDD) = Wide Band Width.</td></tr>
</table>

PIN DESCRIPTION

<table>
<tr><th>NAME</th><th>LEVEL</th><th>TYPE</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>CDRREFSEL</td><td>LVTTL, LVCMOS</td><td>I</td><td>60</td><td>Clock and Data Recover Unit Reference Frequency Select
Selects the Clock and Data Recovery Unit reference frequency based on the table below.
"Low" = CDR uses CMU's reference clock
"High" = CDR reference clock from CDRAUXREF-CLK
<table><tr><th>CDRREF-SEL</th><th>STS12/ STS3</th><th>CDRAUXREF-CLK Frequency</th><th>Data Rate</th></tr><tr><td>0</td><td colspan="3">CDR uses CMU's reference clock (see CMUFREQSEL pin)</td></tr><tr><td>1</td><td>0</td><td>77.76 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr><tr><td>1</td><td>1</td><td>77.76 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr></table>NOTE: CDRAUXREFCLK requires accuracy of 77.76 MHz ∓200 ppm.</td></tr>
<tr><td>LOOPTIME</td><td>LVTTL, LVCMOS</td><td>I</td><td>2</td><td>Loop Timing Mode
When the loop timing mode is activated the external reference clock to the input of the Retimer is replaced with the high-speed recovered receive clock from the CDR.
"Low" = Disabled
"High" = Loop timing Activated</td></tr>
<tr><td>CDRDIS</td><td>LVTTL, LVCMOS</td><td>I</td><td>12</td><td>Clock and Data Recovery Unit Disable
Active "High." Disables internal Clock and Data Recovery unit. Received serial data bypasses the integrated CDR block. RXINP/N is then sampled on the rising edge of externally recovered differential clock XRXCLKIP/N coming from the optical module.
"Low" = Internal CDR unit is Enabled
"High" = Internal CDR unit is Disabled and Bypassed</td></tr>
</table>

PIN DESCRIPTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
$\overline{\text{PIO\_CTRL}}$	LVTTL, LVCMOS	I	48	**Transmit Parallel Clock Directional Control** **Transmit Parallel Clock Output Operation** If this pin is asserted "High", TXPCLK_IO is a parallel bus clock output. Data on the TXDI[7:0] must be synchronously applied prior to the sampling by the PISO at the rising edge of TXPCLK_IO clock output driven by the XRT91L31. **Alternate Transmit Parallel Clock Input Operation** Asserting this control pin "Low" or if left unconnected, it configures TXPCLK_IO to serve as a parallel bus clock input rather than a parallel bus clock output and permits the XRT91L31 to accept the external clock input. Data on the TXDI[7:0] is then sampled at the rising edge of the TXPCLK_IO clock input driven by the framer/mapper device. "Low" = TXPCLK_IO is a Parallel Clock Input. "High" = TXPCLK_IO is a Parallel Clock Output. ***NOTE:*** *Parallel Clock Input operation has the advantage of permitting the framer/mapper device timing to be synchronized with the transceiver transmitter timing.* This pin is provided with an internal pull-down.
RLOOPS	LVTTL, LVCMOS	I	63	**Serial Remote Loopback** The serial remote loopback mode interconnects the receive serial data input to the transmit serial data output. If serial remote loopback is enabled, the 8-bit parallel transmit data input is ignored while the 8-bit parallel receive data output is maintained. "Low" = Disabled "High" = Serial Remote Loopback Mode Enabled ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature in normal operation.*
DLOOP	LVTTL, LVCMOS	I	62	**Digital Local Loopback** The digital local loopback mode interconnects the 8-bit parallel transmit data input and TxCLK to the 8-bit parallel receive data output and RxCLK respectively while maintaining the transmit serial data output. If digital local loopback is enabled, the receive serial data input is ignored. "Low" = Disabled "High" = Digital Local Loopback Mode Enabled ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature in normal operation.*
ALOOP	LVTTL, LVCMOS	I	64	**Analog Local Loopback** This loopback feature serializes the 8-bit parallel transmit data input and presents the data to the transmit serial output and in addition it also internally routes the serialized data back to the Clock and Data Recovery block for serial to parallel conversion. The received serial data input is ignored. "Low" = Disabled "High" = Analog Local Loopback Mode Enabled

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXDI0 TXDI1 TXDI2 TXDI3 TXDI4 TXDI5 TXDI6 TXDI7	LVTTL, LVCMOS	I	58 57 56 55 54 53 51 50	**Transmit Parallel Data Input** Transmit Parallel Clock Output Operation The 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel transmit data should be applied to the transmit parallel bus and simultaneously referenced to the rising edge of the TXPCLK_IO clock output. The 8-bit parallel interface is multiplexed into the transmit serial output interface with the MSB first (TXDI[7:0]). **Alternate Transmit Parallel Clock Input Operation** When operating is this mode, TXPCLK_IO is no longer a parallel clock output reference but reverses direction and serves as the parallel transmit clock input reference for the PISO (Parallel Input to Serial Output) block. The 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel transmit data should be applied to the transmit parallel bus and simultaneously referenced to the rising edge of the TXPCLK_IO clock input.
TXOP TXON	LVPECL Diff	O	5 6	**Transmit Serial Data Output** The transmit serial data stream is generated by multiplexing the 8-bit parallel transmit data input into a 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 serial data stream.
TXPCLK_IO	LVTTL, LVCMOS	I/O	49	**Transmit Parallel Clock Input/Output (77.76/19.44 MHz)** **Transmit Parallel Clock Output Operation** When the $\overline{\text{PIO\_CTRL}}$ pin 48 is asserted "High," this pin will output a 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock output reference for the 8-bit parallel transmit data input TXDI[7:0]. This clock is used by the framer/mapper device to present the TXDI[7:0] data which the XRT91L31 will latch on the rising edge of this clock. This enables the framer/mapper device and the XRT91L31 transceiver to be in synchronization. **Alternate Transmit Parallel Clock Input Operation** When the $\overline{\text{PIO\_CTRL}}$ pin 48 is asserted "Low," this pin will accept a 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock input reference for the 8-bit parallel transmit data input TXDI[7:0]. The XRT91L31 will latch data at TXDI[7:0] on the rising edge of this clock. This has the enormous advantage of enabling the framer/mapper device transmit timing to be synchronized with the transceiver transmit timing.

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
REFCLKP REFCLKN	LVPECL Diff	I	16 17	**Reference Clock Input (77.76 MHz or 19.44 MHz)** This differential clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high speed clock reference for this device. It will accept either a 77.76 MHz or a 19.44 MHz Differential LVPECL clock source. Pin CMUFREQSEL determines the value used as the reference. See Pin CMUFREQSEL for more details. REFCLKP/N inputs are internally biased to 1.65V. ***NOTE:*** *In the event that TTLREFCLK LVTTL input is used instead of these differential inputs for clock reference, the REFCLKP should be tied to ground.*
TTLREFCLK	LVTTL, LVCMOS	I	36	**Auxillary Reference Clock Input (77.76 MHz or 19.44 MHz)** This LVTTL clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high speed clock reference for this device. It will accept either a 77.76 MHz or a 19.44 MHz LVTTL clock source. Pin CMUFREQSEL determines the value used as the reference. See Pin CMUFREQSEL for more details. ***NOTE:*** *In the event that REFCLKP/N differential inputs is used instead of this LVTTL input for clock reference, the TTLREFCLK should be tied to ground.*

RECEIVER SECTION

PIN DESCRIPTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXDO0 RXDO1 RXDO2 RXDO3 RXDO4 RXDO5 RXDO6 RXDO7	LVTTL, LVCMOS	O	19 20 22 23 24 25 26 27	**Receive Parallel Data Output** 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel receive data output is updated simultaneously on the falling edge of the RXPCLKO output. The 8-bit parallel interface is de-multiplexed from the receive serial data input MSB first (RXDO[7]). The XRT91L31 will output the data on the falling edge of RXPCLKO clock.
RXIP RXIN	Diff LVPECL	I	13 14	**Receive Serial Data Input** The differential receive serial data stream of 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 is applied to these input pins. These pins have internal LVPECL common-mode biasing circuit. External 100R termination is required between RXIP/N pins.
XRXCLKIP XRXCLKIN	Diff LVPECL	I	8 9	**External Recovered Receive Clock Input** The differential receive serial data stream of 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 is sampled on the rising edge of this externally recovered differential clock coming from the optical module. It is used when the internal CDR unit is disabled and bypassed by the CDRDIS pin. These pins have internal LVPECL common-mode biasing circuit. External 100R termination is required between XRXCLKIP/N pins. ***NOTE:*** *In the event that XRXCLKIP/N differential input pins are unused, XRXCLKIP should be tied to VCC with a 1k Ohm pull-up and XRXCLKIN should be tied to Ground with a 1k Ohm pull-down.*
RXPCLKO	LVTTL, LVCMOS	O	29	**Receive Parallel Clock Output (77.76 MHz or 19.44 MHz)** 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock output reference for the 8-bit parallel receive data output RXDO[7:0]. The parallel received data output bus will be updated on the falling edge of this clock.
CDRAUX- REFCLK	LVTTL, LVCMOS	I	32	**Clock and Data Recovery Auxillary Reference Clock** 77.76 MHz ± 200 ppm auxillary reference clock for the CDR. ***NOTE:*** *In the event that CDRAUXREFCLK LVTTL input pin is unused, CDRAUXREFCLK should be tied to ground.*
OOF	LVTTL, LVCMOS	I	11	**Out of Frame Input Indicator** This level sensitive input pin is used to initiate frame detection and byte alignment recovery when OOF is declared by the downstream device. When this pin is held High, FRAMEPULSE will pulse for a single RXPCLKO period upon the detection of every third frame alignment A2 byte in the incoming SONET/SDH Frame. "Low" = Normal Operation "High" = OOF Indication initiating frame detection and byte boundary recovery and activating FRAMEPULSE

PIN DESCRIPTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
FRAMEPULSE	LVTTL, LVCMOS	O	30	**Sonet Frame Alignment Pulse** This pin will generate a single pulse for an RXPCLKO clock period upon the detection of the third frame alignment A2 byte whenever the OOF input pin is held High. The parallel received data output bus will then be byte aligned to this newly recovered SONET/SDH frame.
CAP1P CAP2P	Analog	-	39 42	**CDR Non-polarized External Filter Capacitor** C1 = 0.47μF ± 10% tolerance (Isolate from noise and place close to pin)
CAP1N CAP2N	Analog	-	40 41	**CDR Non-polarized External Filter Capacitor** C2 = 0.47μF ± 10% tolerance (Isolate from noise and place close to pin)
DLOSDIS	LVTTL, LVCMOS	I	7	**LOS (Los of Signal) Detect Disable** Disables internal LOS monitoring and automatic muting of RXDO[7:0] upon LOS detection. LOS is declared when a string of 128 consecutive zeros occur on the line. LOS condition is cleared when the 16 or more pulse transitions is detected for 128 bit period sliding window (see **Figure 7**.) "Low" = Monitor and Mute received data upon LOS declaration "High" = Disable internal LOS monitoring
$\overline{\text{LOSEXT}}$	SE-LVPECL	I	33	**LOS or Signal Detect Input from Optical Module** Active "Low." When active, this pin can force the received data output bus RXDO[7:0] to a logic state of '0' per **Figure 7**. "Low" = Forced LOS "High" = Normal Operation

POWER AND GROUND

PIN DESCRIPTION

NAME	TYPE	PIN	DESCRIPTION
VDD3.3	PWR	18, 31, 34, 47, 61	**3.3V CMOS Power Supply** VDD3.3 should be isolated from the Analog VDD power supplies. Use a ferrite bead along with an internal power plane separation. The VDD3.3 power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_TX	PWR	38	Analog 3.3V Transmitter Power Supply AVDD3.3_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_TX power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_RX	PWR	43	**Analog 3.3V Receiver Power Supply** AVDD3.3_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_RX power supply pins should have bypass capacitors to the nearest ground.

PIN DESCRIPTION

NAME	TYPE	PIN	DESCRIPTION
VDD_PECL	PWR	4, 10	**3.3V Input/Output LVPECL Bus Power Supply** These pins require a 3.3V potential voltage for properly biasing the Differential LVPECL input and output pins.
AGND_TX	PWR	37	**Transmitter Analog Ground for 3.3V Analog Power Supplies** It is recommended that all ground pins of this device be tied together.
AGND_RX	PWR	44	**Receiver Analog Ground for 3.3V Analog Power Supplies** It is recommended that all ground pins of this device be tied together.
GND	GND	21, 28, 35, 45, 46, 52	**Power Supply and Thermal Ground** It is recommended that all ground pins of this device be tied together.

1.0 FUNCTIONAL DESCRIPTION

The XRT91L31 transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The transceiver converts 8-bit parallel data running at 77.76 Mbps (STS-12/STM-4) or 19.44 Mbps (STS-3/STM-1) to a serial Differential LVPECL bit stream at 622.08 Mbps or 155.52 Mbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), receive clock and data recovery (CDR) unit and a SONET/SDH frame and byte boundary detection circuit. The transceiver is divided into Transmit and Receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

1.1 STS-12/STM-4 and STS-3/STM-1 Mode of Operation

Functionality of the transceiver can be configured by using the appropriate signal level on the STS-12/$\overline{\text{STS-3}}$ pin. STS-3/STM-1 mode is selected by pulling STS-12/$\overline{\text{STS-3}}$ "Low" as described in the Hardware Pin Descriptions. However, if STS-12/STM-4 mode is desired, it is selected by pulling STS-12/$\overline{\text{STS-3}}$ "High." Therefore, the following sections describe the functionality rather than how each function is controlled. Hence, the Hardware Pin and Register Bit Descriptions focus on device configuration.

1.2 Clock Input Reference for Clock Multiplier (Synthesizer) Unit

The XRT91L31 can accept both a 19.44 MHz or a 77.76 MHz Differential LVPECL clock input at REFCLKP/N or a Single-Ended LVTTL clock at TTLREFCLK as its internal timing reference for generating higher speed clocks. The REFCLKP/N or TTLREFCLK input should be generated from an LVPECL/LVTTL crystal oscillator which has a frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems. The reference clock can be provided with one of two frequencies chosen by CMUFREQSEL. The reference frequency options for the XRT91L31 are listed in Table 1.

TABLE 3: CMU REFERENCE FREQUENCY OPTIONS (DIFFERENTIAL OR SINGLE-ENDED)

CMUFREQSEL	STS12/$\overline{\text{STS3}}$	REFCLKP/N OR TTLREFCLK REFERENCE FREQUENCY	DATA RATE
0	**0**	77.76 MHz	STS-3/STM-1 155.52 Mbps
0	**1**	77.76 MHz	STS-12/STM-4 622.08 Mbps
1	**0**	19.44 MHz	STS-3/STM-1 155.52 Mbps
1	**1**	19.44 MHz	STS-12/STM-4 622.08 Mbps

1.3 Data Latency

Due to different operating modes and data logic paths through the device, there is an associated latency from data ingress to data egress. Table 4 specifies the data latency for a typical path.

TABLE 4: DATA INGRESS TO DATA EGRESS LATENCY

Mode Of Operation	Data Path	Clock Reference	Range Of Clock Cycles
Thru-mode	MSB at RXIP/N to data on RXDO[7:0]	Recoved RXIP/N Clock	25 to 35
Serial Remote Loopback	MSB at RXIP/N to MSB at TXOP/N	Recoved RXIP/N Clock	2 to 4

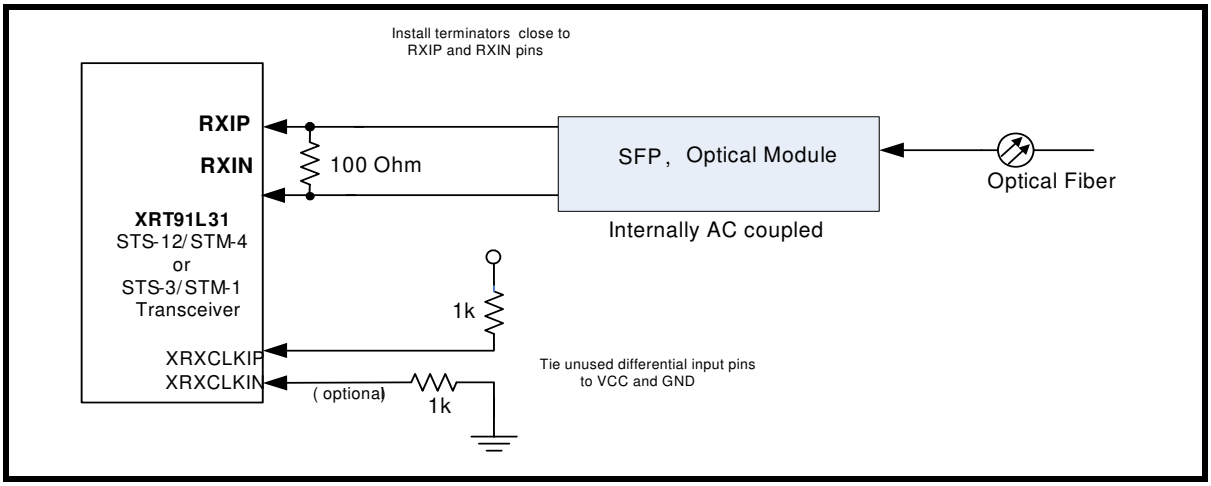
2.0 RECEIVE SECTION

The receive section of XRT91L31 include the inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter. The receiver accepts the high speed Non-Return to Zero (NRZ) serial data at 622.08 Mbps or 155.52 Mbps through the input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into an 8-bit-wide, 77.76 Mbps or 19.44 Mbps parallel data and presented to the RXDO[7:0] parallel interface. This parallel interface is designed for Single-Ended LVTTL operation. A divide-by-8 version of the high-speed recovered clock RXPCLKOP/N, is used to synchronize the transfer of the 8-bit RXDO[7:0] data with the receive portion of the framer/mapper device. Upon initialization or loss of signal or loss of lock, the external reference clock signal of 19.44 MHz or 77.76 MHz is used to start-up the clock recovery phase-locked loop for proper operation. In certain applications, the CDR block on the XRT91L31 can be disabled and bypassed by enabling the CDRDIS pin to permit the flexibility of using an externally recovered receive clock thru the XRXCLKIP/N pins.

2.1 Receive Serial Input

The receive serial inputs are applied to RXIP/N and originate from an AC coupled environement (i.e. AC-coupled SFP). A simplified block diagram is shown in **Figure 3**. Since this dievice has internal pull up/pull down biasing resitors, a 100 Ω line-to-line termination is the only resistor needed and must be installed as close to the RXI pins as possible. See Applications note for further clarifications.

FIGURE 3. RECEIVE SERIAL INPUT INTERFACE BLOCK



2.2 Recieve Serial Data Input Timing

The received High-Speed Serial Differential Data Input must adhere to the set-up and hold time timing specifications below.

FIGURE 4. RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING DIAGRAM

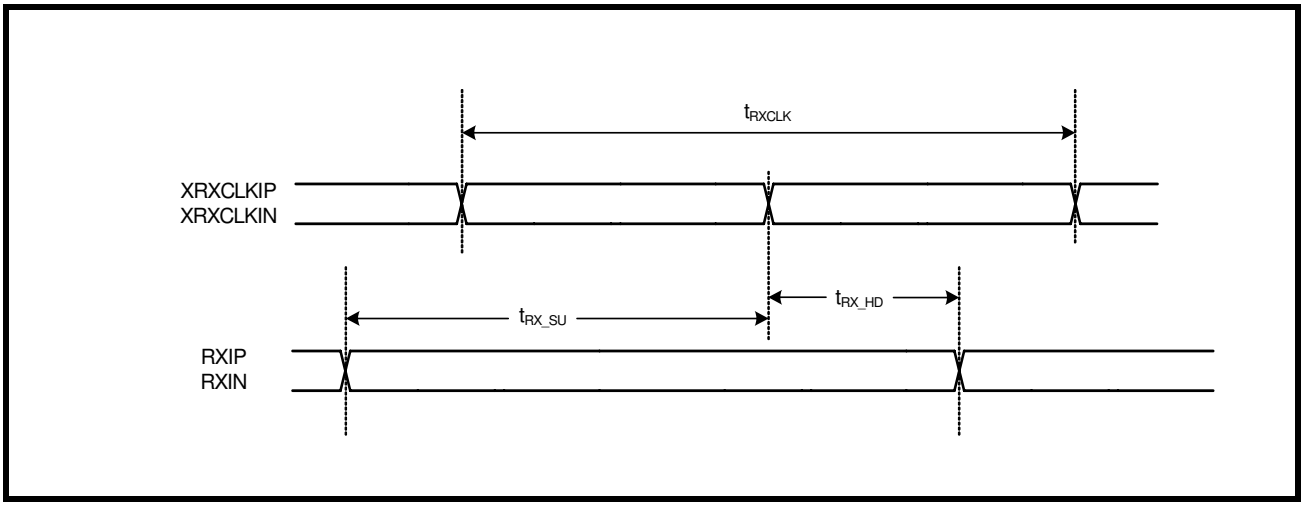


TABLE 5: RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive external recovered clock period		1.608		ns
t_{RX_SU}	Serial data setup time with respect to XRXCLKIP/N	400			ps
t_{RX_HD}	Serial data hold time with respect to XRXCLKIP/N	100			ps

TABLE 6: RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING (STS-3/STM-1 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive external recovered clock period		6.43		ns
t_{RX_SU}	Serial data setup time with respect to XRXCLKIP/N	1.5			ns
t_{RX_HD}	Serial data hold time with respect to XRXCLKIP/N	1.5			ns

2.3 Receive Clock and Data Recovery

The clock and data recovery (CDR) unit accepts the high speed NRZ serial data from the Differential LVPECL receiver and generates a clock that is the same frequency as the incoming data. The clock recovery can either utilize the transmitter's CMU reference clock from either REFCLKP/N or TTLREFCLK (+/- 20ppm) or it can use independent clock source CDRAUXREFCLK (+/- 200ppm) to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the local reference clock. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock. Whenever a Loss of Lock or a Loss of Signal event occurs, the CDR will continue to supply a receive clock (based on the local reference) to the framer/mapper device. When the LOSEXT is asserted by the optical module or when LOS is detected, the receive parallel data output will be forced to a logic zero state for the entire duration that a LOS condition is detected. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data. When the LOSEXT becomes inactive and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source and LOS is no longer declared, the clock recovery PLL will switch and lock back onto the incoming receive data stream. Table 7 shows Clock and Data Recovery reference clock settings. Table 8 specifies the Clock and Data Recovery Unit performance characteristics.

TABLE 7: CLOCK DATA RECOVERY UNIT REFERENCE CLOCK SETTINGS

CMUFREQSEL	CDRREFSEL	STS12/ STS3	REFCLKP/N[1] OR TTLREFCLK[1] FREQUENCY (MHZ)	CDRAUXREFCLK[2] FREQUENCY (MHZ)	CDR OUTPUT FREQUENCY (MHZ)
0	0	0	77.76 MHz	not used	155.52
0	0	1	77.76 MHz	not used	622.08
1	0	0	19.44 MHz	not used	155.52
1	0	1	19.44 MHz	not used	622.08
X	1	0	not referenced by CDR	77.76 MHz	155.52
X	1	1	not referenced by CDR	77.76 MHz	622.08

1Requires frequency accuracy better than +/- 20 ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems.

2CDRAUXREFCLK requires accuracy of 77.76 MHz +/- 200 ppm.

TABLE 8: CDR AUXREFCLK REFERENCE FREQUENCY REQUIREMENT FOR CLOCK AND DATA RECOVERY

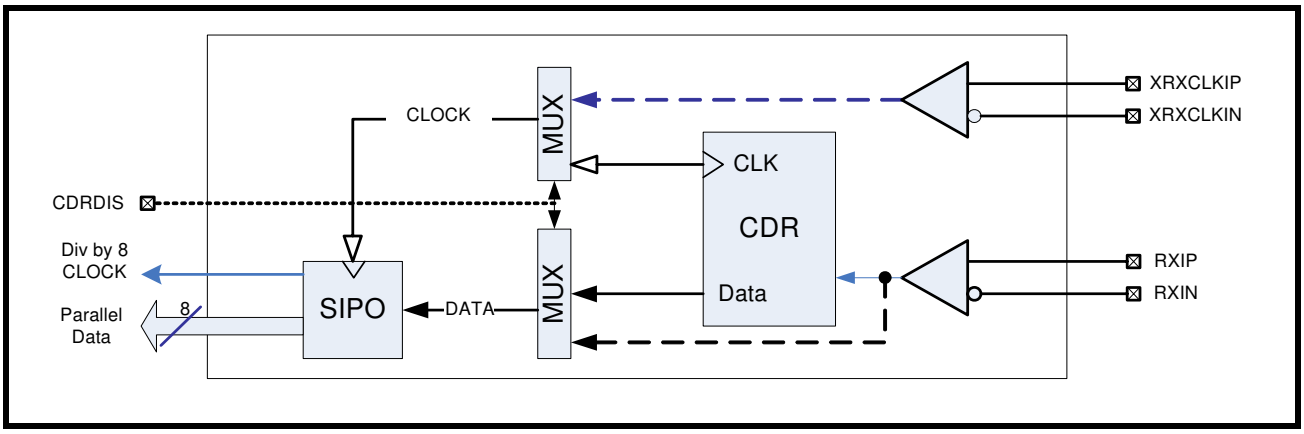
NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	40		60	%
REF_{TOL}	Reference clock frequency tolerance	-200		+200	ppm

2.3.1 Internal Clock and Data Recovery Bypass

Optionally, the internal CDR unit can be disabled and bypassed in lieu of an externally recovered clock. Asserting the CDRDIS "High" disables the internal Clock and Data Recovery unit and the received serial data bypasses the integrated CDR block. RXINP/N is then sampled on the rising edge of the externally recovered

differential clock XRXCLKIP/N coming from the optical module or an external clock recovery unit. Figure 5 shows the possible internal paths of the recovered clock and data.

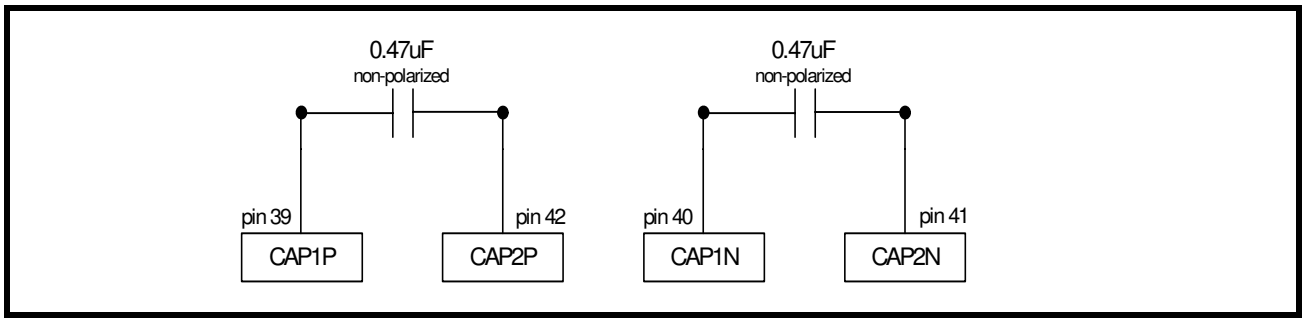
FIGURE 5. INTERNAL CLOCK AND DATA RECOVERY BYPASS



2.4 External Receive Loop Filter Capacitors

These external loop filter 0.47µF non-polarized capacitors provide the necessary components to achieve the required receiver jitter performance. They must be well isolated to prohibit noise entering the CDR block and should be placed as close to the pins as much as possible. Figure 6 shows the pin connections and external loop filter components. These two non-polarized capacitors should be of +/- 10% tolerance.

FIGURE 6. EXTERNAL LOOP FILTERS

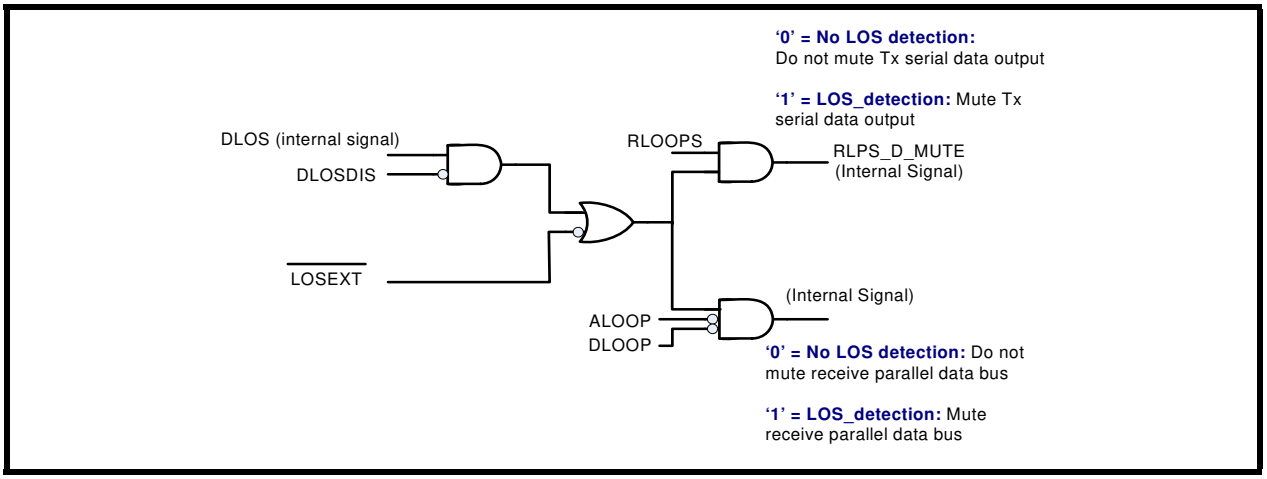


2.5 Loss Of Signal

XRT91L31 supports internal Loss of Signal detection (LOS) and external LOS detection. The internal Loss of Signal Detector monitors the incoming data stream and if the incoming data stream has no transition continuously for more than 128 bit periods, Loss of Signal is declared. This LOS detection will be removed when the circuit detects 16 transitions in a 128 bit period sliding window. Pulling the corresponding DLOSDIS signal to a high level will disable the internal LOS detection circuit. The external LOS function is supported by the $\overline{\text{LOSEXT}}$ input. The Single-Ended LVPECL input usually comes from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices, the polarity of this signal can be either active "Low" or active "High". $\overline{\text{LOSEXT}}$ is an active "Low" signal requiring a low level to assert or invoke a forced LOS. The external $\overline{\text{LOSEXT}}$ input pin and internal LOS detector are gated to control detection and declaration of Loss of Signal (see Figure 7.)

Whenever LOS is internally detected or an external LOS is asserted thru the $\overline{\text{LOSEXT}}$ pin, and none of the local loopback loops is enabled, the XRT91L31 will automatically force the receive parallel data output to a logic state "0" for the entire duration that a LOS condition is declared. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data. When the local loopbacks DLOOP or ALOOP is enabled, then LOS conditions will not mute the RX parallel output.

FIGURE 7. LOS DECLARATION CIRCUIT



During RLOOPS operation, the 91L31 mutes the RLOOPS data going to Tx output upon detection of DLOS while DLOSDIS is not enabled. During RLOOPS operation, the 91L31 also mutes the RLOOPS data going to

Tx output while the LOSEXT input is set to a “LOW” state. Note that the DLOSDIS control pin has no impact on the CDR muting function due to LOSEXT. DLOSDIS only applies to muting as a result of DLOS detection.

Also, note that serial muting function (RLPS_D_MUTE) only impacts RLOOPS data going to Tx output.

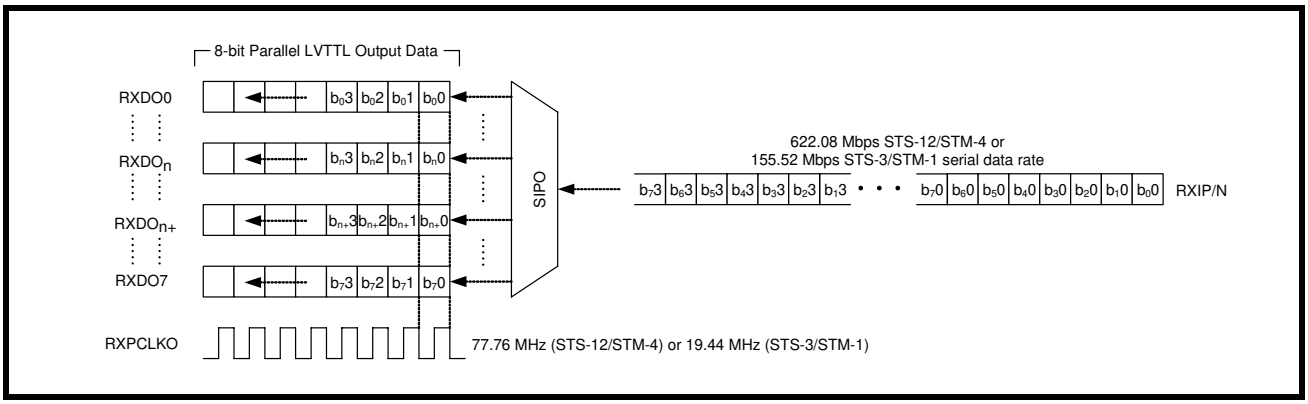
2.6 SONET Frame Boundary Detection and Byte Alignment Recovery

A Frame and Byte Boundary Detection circuit searches the incoming data channel for three consecutive A1 (0xF6 Hex) bytes followed by three consecutive A2 (0x28 Hex) bytes. The detector operates under the control of the OOF (Out of Frame) signals provided from the SONET Framer. Detection is enabled when OOF is held "High" and remains active until OOF goes "Low." When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming receive data stream. The receive serial-to-parallel converter block uses the located byte boundary to assemble the incoming data stream into bytes for output on the parallel data output bus RXDO[7:0]. The frame boundary is reported on the frame pulse (FRAMEPULSE) output at the onset of detecting the third A2 byte pattern when any serial 48-bit pattern matching the framing pattern is detected on the incoming data stream. While in the pattern search and detection state and so long is OOF is active, the frame pulse (FRAMEPULSE) output is activated for one byte clock cycle (RXPCLKO = 12.86 ns pulse duration for STS-12/STM-4 or 51.44 ns pulse duration for STS-3/STM-1) anytime a 48-bit pattern matching the framing pattern is detected on the incoming data stream. Once the SONET Framer Overhead Circuitry has verified that frame and byte synchronization are correct, the OOF input pin should be de-asserted by the SONET Framer to disable the XRT91L31 frame search process from trying to synchronize repeatedly and to de-activate FRAMEPULSE. When the XRT91L31’s framing pattern detection is disabled upon the de-assertion of OOF input pin from the SONET Framer, the byte boundary will lock to the detected location and will remain locked to that location found when detection was previously enabled.

2.7 Receive Serial Input to Parallel Output (SIPO)

During STS-12/STM-4 operation, the SIPO is used to convert the 622.08 Mbps serial data input to 77.76 Mbps parallel data output which can interface to a SONET Framer/ASIC. If the XRT91L31 is operating in STS-3/STM-1, the SIPO will convert the 155.52 Mbps serial data input to 19.44 Mbps parallel data output. The SIPO bit de-interleaves the serial data input into an 8-bit parallel output to RXDO[7:0]. A simplified block diagram is shown in **Figure 8**. XRT91L31 clocks data out on RXDO[7:0] at the falling edge of RXPCLKO.

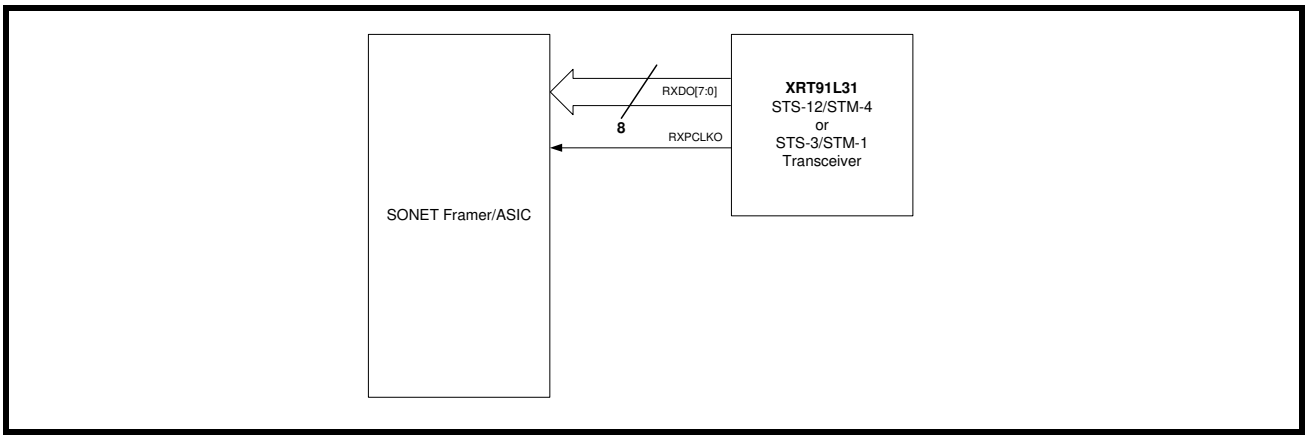
FIGURE 8. SIMPLIFIED BLOCK DIAGRAM OF SIPO



2.8 Receive Parallel Output Interface

The 8-bit Single-Ended LVTTL running at 77.76 Mbps (STS-12/STM-4) or 19.44 Mbps (STS-3/STM-1) parallel data output of the receive path is used to interface to a SONET Framer/ASIC synchronized to the recovered clock. A simplified block diagram is shown in **Figure 9**.

FIGURE 9. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK



2.9 Disable Parallel Receive Data Output Upon LOS

The parallel receiver outputs are automatically pulled "Low" or forced to a logic state of "0" during a LOS condition (DLOOP or ALOOP not activated) to prevent data chattering unless LOS detection is disabled by asserting DLOSDIS and keeping $\overline{\text{LOSEXT}}$ input pin "high." In addition, the user can also assert $\overline{\text{LOSEXT}}$ input pin from the optical module to force an LOS and mute the parallel receiver outputs as well when DLOSDIS is not enabled (LOW), see **Figure 7**).

2.10 Receive Parallel Data Output Timing

The receive parallel data output from the STS-12/STM-4 or STS-3/STM-1 receiver will adhere to the setup and hold times shown in Figure 10 ,Table 9, and Table 10. Table 11 shows the PECL and TTL output timing specifications.

FIGURE 10. RECEIVE PARALLEL OUTPUT TIMING

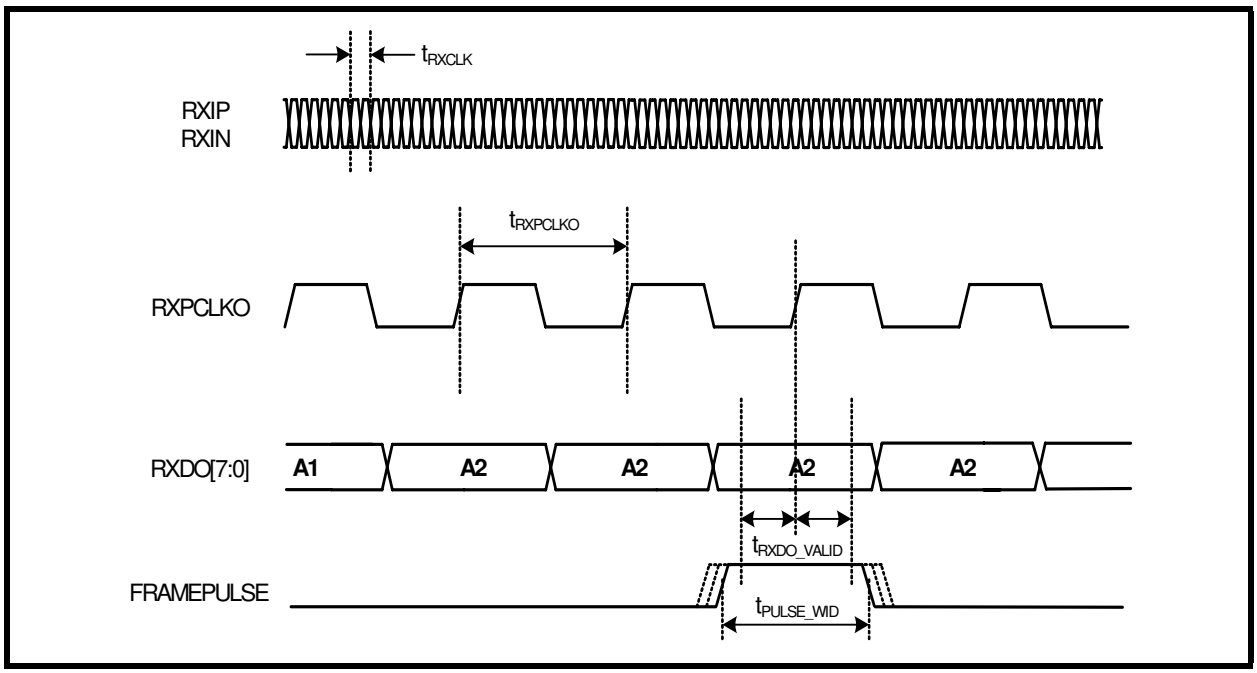


TABLE 9: RECEIVE PARALLEL DATA OUTPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive high-speed serial clock period		1.608		ns
$t_{RXPCLKO}$	Receive parallel data output byte clock period		12.86		ns
t_{RXDO_VALID}	Time the data is valid on RXDO[7:0] and FRAMEPULSE before and after the rising edge of RXPCLKO	4			ns
t_{PULSE_WID}	Pulse width of frame detection pulse on FRAMEPULSE		12.86		ns

TABLE 10: RECEIVE PARALLEL DATA OUTPUT TIMING (STS-3/STM-1 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive high-speed serial clock period		6.43		ns
$t_{RXPCLKO}$	Receive parallel data output byte clock period		51.44		ns
t_{RXDO_VALID}	Time the data is valid on RXDO[7:0] and FRAMEPULSE before and after the rising edge of RXPCLKO	22			ns
t_{PULSE_WID}	Pulse width of frame detection pulse on FRAMEPULSE		51.44		ns

TABLE 11: PECL AND TTL RECEIVE OUTPUTS TIMING SPECIFICATION

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{R_PECL}	PECL output rise time (20% to 80%)		350		ps
t_{F_PECL}	PECL output fall time (80% to 20%)		350		ps
t_{R_TTL}	TTL output rise time (10% to 90%)		2		ns
t_{F_TTL}	TTL output fall time (90% to 10%)		1.5		ns

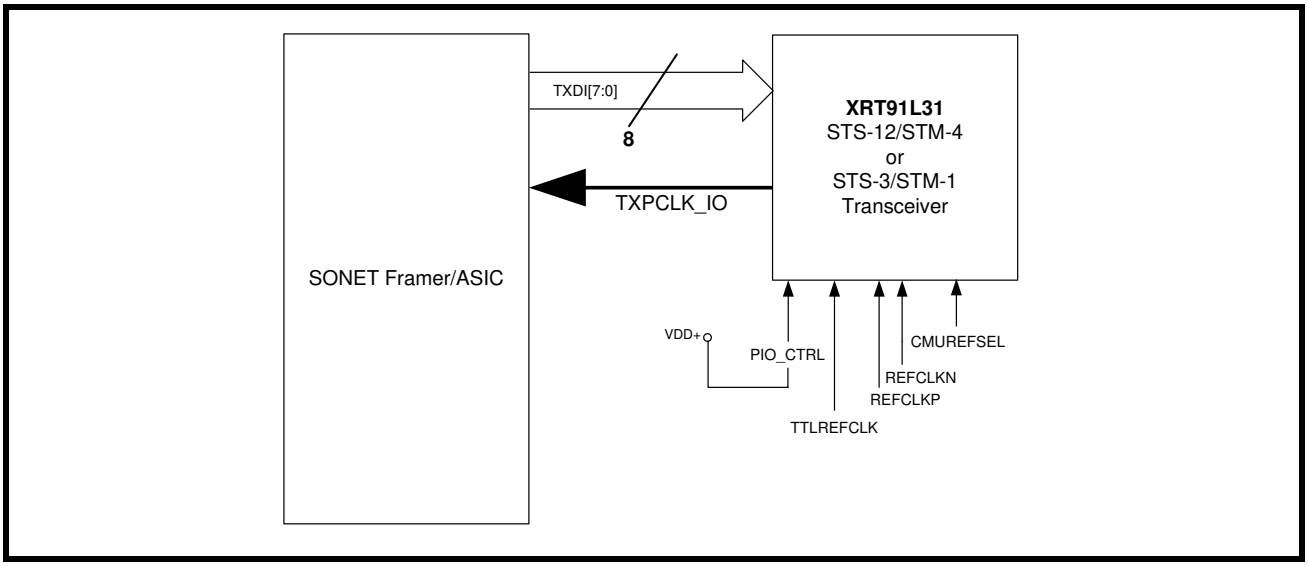
3.0 TRANSMIT SECTION

The transmit section of the XRT91L31 accepts 8-bit parallel data and converts it to serial Differential LVPECL data output intented to interface to an optical module. It consists of an 8-bit parallel Single-Ended LVTTL interface, Parallel-to-Serial Converter, a clock multiplier unit (CMU), a Low Voltage Positive-referenced Emitter-Coupled Logic (LVPECL) differential line driver, and Loop Timing modes. The LVPECL serial data output rate is 622.08 Mbps for STS-12/STM-4 applications and 155.52 Mbps for STS-3/STM-1 applications. The high frequency serial clock is synthesized by a PLL, which uses a low frequency clock as its input reference. In order to synchronize the data transfer process, the synthesized 622.08 MHz for STS-12/STM-4 or 155.52 MHz STS-3/STM-1 serial clock output is divided by eight and the 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock respectively is presented to the framer/mapper device to be used as its timing source.

3.1 Transmit Parallel Input Interface

The parallel data from an framer/mapper device is presented to the XRT91L31 through an 8-bit Single-Ended LVTTL parallel bus interface TXDI[7:0]. To directly interface to the XRT91L31, the SONET Framer/ASIC must be synchronized to the same timing source TXPCLK_IO in presenting data on the parallel bus interface. The data must meet setup and hold times with respect to TXPCLK_IO. This clock output source is used to synchronize the SONET Framer/ASIC to the XRT91L31. The framer/mapper device should use TXPCLK_IO as its timing source so that parallel data is phase aligned with the serial transmit data. The data is latched into a parallel input register on the rising edge of TXPCLK_IO. TXPCLK_IO is derived from a divide-by-8 of the high speed synthesized clock resulting in a 77.76/ 19.44 MHz Single-Ended LVTTL clock output source to be used by the framer/mapper device for parallel bus synchronization. A simplified block diagram of the transmit parallel bus clock output system interface is shown in **Figure 11**.

FIGURE 11. TRANSMIT PARALLEL INPUT INTERFACE BLOCK



3.2 Transmit Parallel Data Input Timing

When applying parallel data input to the transmitter, the setup and hold times should be followed as shown in Figure 12, Table 12 and Table 13.

FIGURE 12. TRANSMIT PARALLEL INPUT TIMING

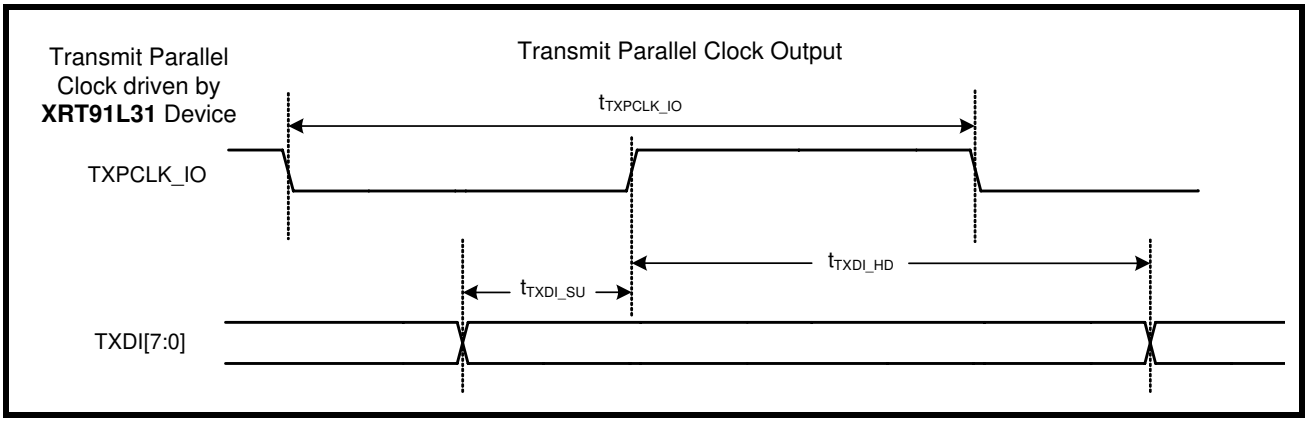


TABLE 12: TRANSMIT PARALLEL DATA INPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TXPCLK_IO}	Transmit Clock **Output** period		12.86		ns
t_{TXDI_SU}	Transmit data setup time with respect to TXPCLK_IO	2.0			ns
t_{TXDI_HD}	Transmit data hold time with respect to TXPCLK_IO	1.0			ns

TABLE 13: TRANSMIT PARALLEL DATA INPUT TIMING (STS-3/STM-1 OPERATION).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TXPCLK_IO}	Transmit Clock **Output** period		51.44		ns
t_{TXDI_SU}	Transmit data setup time with respect to TXPCLK_IO	2.0			ns
t_{TXDI_HD}	Transmit data hold time with respect to TXPCLK_IO	1.0			ns