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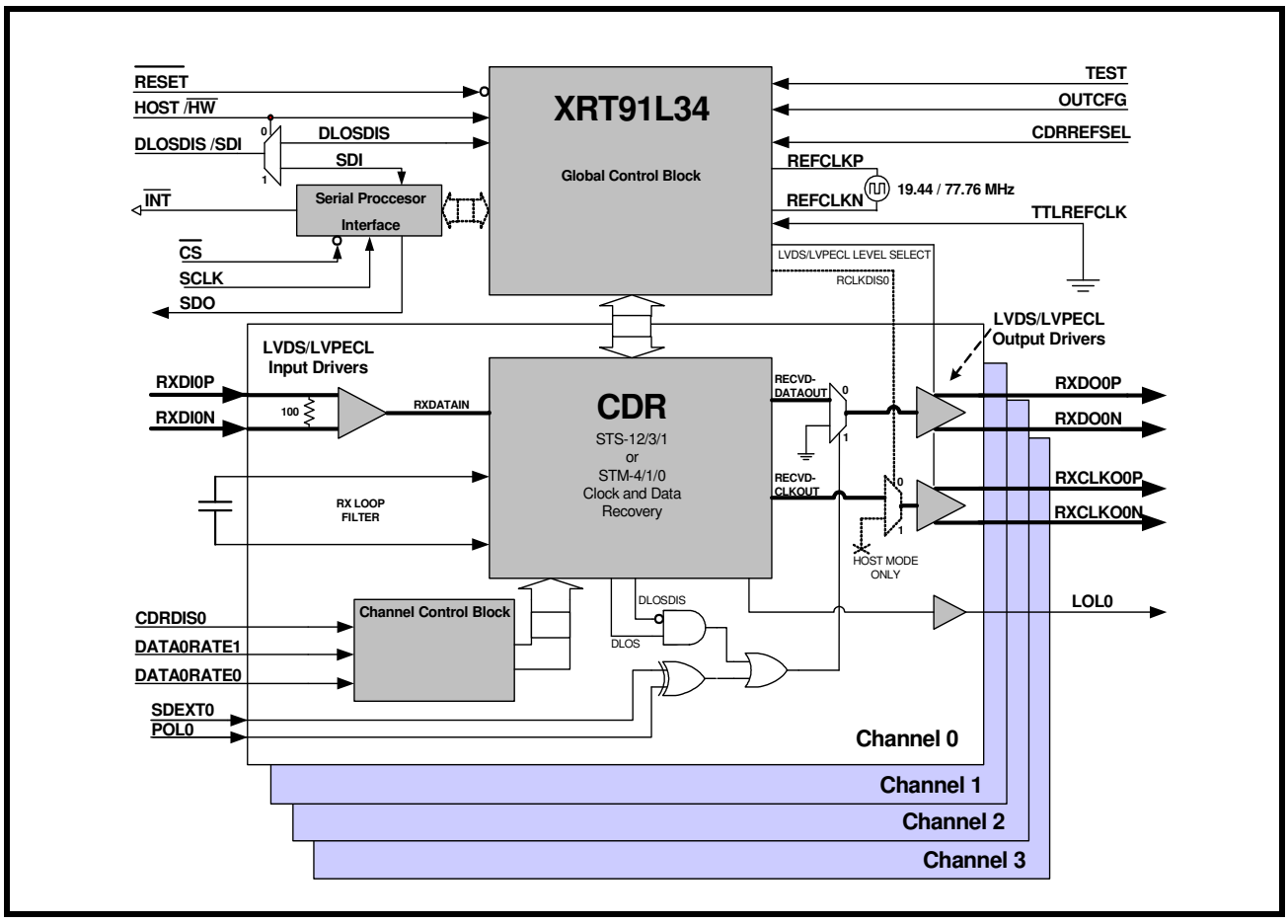
GENERAL DESCRIPTION

The XRT91L34 is a fully integrated quad channel multirate Clock and Data Recovery (CDR) device for SONET/SDH 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 or 51.84 Mbps STS-1/STM-0 applications. The device provides Clock and Data Recovery (CDR) function by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The device internally monitors Loss of Lock (LOL) conditions and automatically mutes recovered data upon Loss of Signal (LOS) conditions.

CLOCK AND DATA RECOVERY OVERVIEW

The clock and data recovery (CDR) unit accepts the high speed NRZ serial data from the LVDS or Differential LVPECL receiver and generates a clock that is the same frequency as the incoming data. The CDR block uses a reference clock to train and monitor its clock recovery PLL. All four channels share a single 77.76MHz or 19.44MHz reference clock. Upon startup, the PLL locks to the local reference clock. Once this is achieved, the PLL attempts to lock onto the incoming receive serial data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock and declare a Loss of Lock. Whenever a Loss of Lock or a Loss of Signal event occurs, the CDR will continue to supply a recovered clock (based on the local reference) to the framer/ mapper device. When the SDEXT is de-asserted by the optical module or when internal DLOS is asserted, the receive serial data output will be forced to a logic zero state for the entire duration that a LOS condition is declared. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data. When the SDEXT becomes active and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source and LOS is no longer declared, the clock recovery PLL will switch and lock back onto the incoming receive serial data stream. Figure 1 shows the block diagram of the XRT91L34.

FIGURE 1. BLOCK DIAGRAM OF XRT91L34



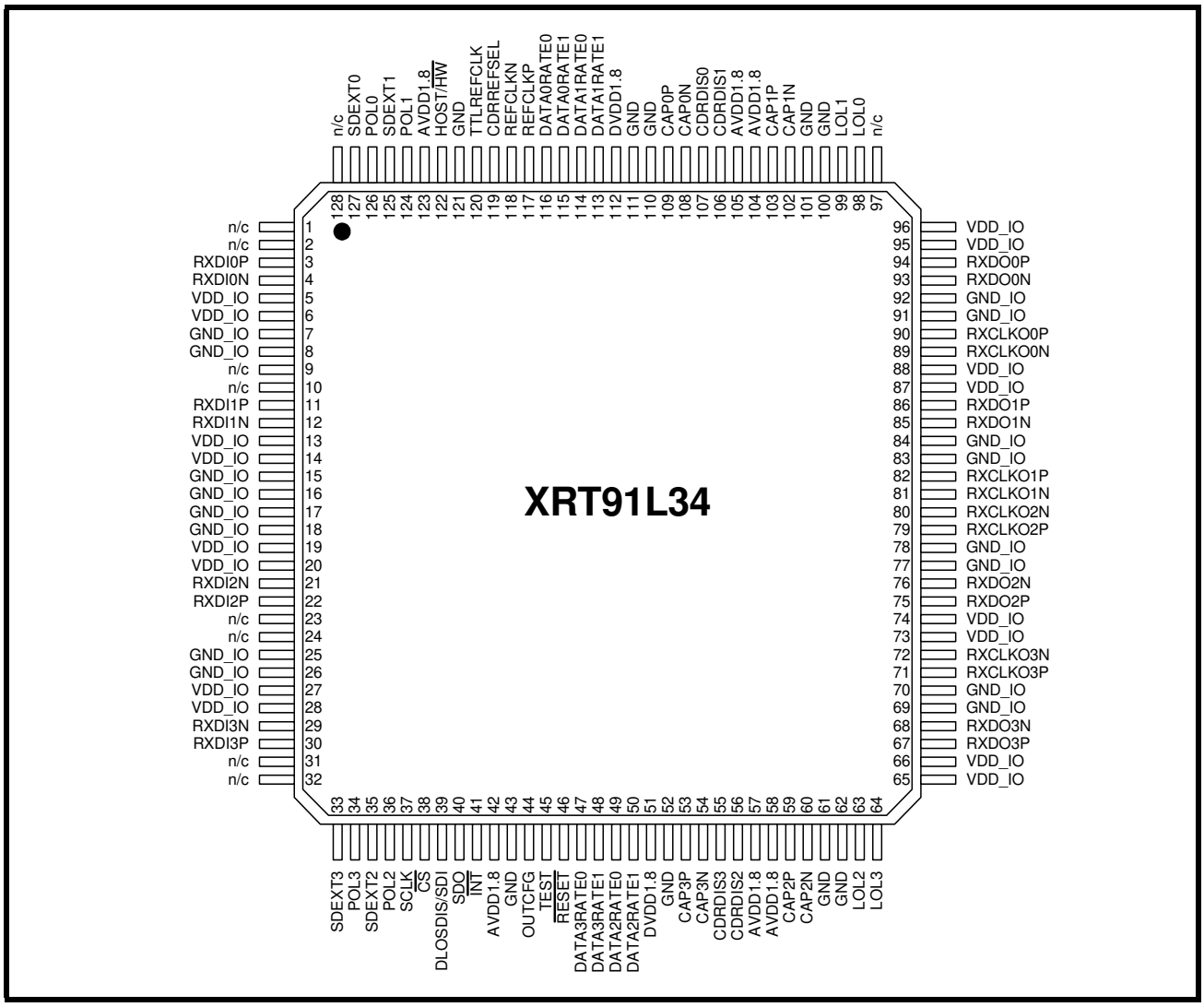
APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

FEATURES

- Quad Channel CDR targeted for SONET STS-12/STS-3/STS-1 and SDH STM-4/STM-1/STM-0 Applications
- Selectable data rate operation between 622.08 Mbps, 155.52 Mbps, or 51.84 Mbps.
- Single-chip fully integrated solution containing quad-channel clock and data recovery (CDR) functions
- Optional flexibility to configure for LVDS or Differential LVPECL High Speed I/O Interface
- Internal 100Ω termination for the high speed LVDS/Differential LVPECL inputs included
- Utilizes reference clock frequency of either 19.44 MHz or 77.76 MHz
- Host mode serial microprocessor interface simplifies monitor and control, including LOS monitoring
- Diagnostics features include LOS monitoring in Host Mode and automatic recovered data mute upon LOS
- Loss of Lock Detect output for each channel
- Permits mixed data rate configuration of the four channels
- Independent power down control of unused channels for lower power operation
- Meets Telcordia, ANSI and ITU-T G.783 and G.825 SDH jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, and GR-253 CORE, GR-253 ILR SONET Jitter specifications.
- Complies with ANSI/TIA/EIA-644 and IEEE P1596.3 3.3V LVDS standard, 3.3V Differential LVPECL, and JESD 8-B LVTTL and LVCMOS standard.
- Operates with dual power supply of 1.8V core and 3.3V IO supply
- 90mW LVDS/ 350mW Differential LVPECL per channel Typical Power Dissipation
- Package: 14 x 14 x 1.4 mm 128-pin LQFP
- RoHS Compliant Lead-Free package availability
- ESD greater than 2kV on all pins

FIGURE 2. 128 LQFP PIN OUT OF THE XRT91L34 (TOP VIEW)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L34IV	128 Pin Lead LQFP	-40°C to +85°C
XRT91L34IV-F	128 Pin Lead-Free LQFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS

HARDWARE CONTROL

<table>
<tr><th>NAME</th><th>LEVEL</th><th>TYPE</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>LVTTL, LVCMOS</td><td>I</td><td>46</td><td>Master Reset Input
Active "Low." When this pin is pulled "Low", the internal state machines and registers are set to their default state.
"Low" = Master Hardware Reset
"High" = Normal Operation
This pin is provided with an internal pull-up.</td></tr>
<tr><td>TEST</td><td>LVTTL, LVCMOS</td><td>I</td><td>45</td><td>Test Input
Active "High." When this pin is pulled "High", the 91L34 internal state machines will enter into a factory test mode.
"Low" = Normal Operation
"High" = Factory Test Diagnostic Mode
NOTE: This pin should be pulled Low for normal operation.
This pin is provided with an internal pull-down.</td></tr>
<tr><td>DATA0RATE[1:0]</td><td>LVTTL, LVCMOS</td><td>I</td><td>115, 116</td><td rowspan="4">Data Rate Selection
Selects SONET/SDH reception speed rate for each of the four channels independently according to the logic below.
<table><tr><th colspan="2">DATANRATE[1:0]</th><th>DATA RATE</th></tr><tr><td>0</td><td>0</td><td>STS-1/STM-0
51.84 Mbps</td></tr><tr><td>0</td><td>1</td><td>STS-3/STM-1
155.52 Mbps</td></tr><tr><td>1</td><td>0</td><td>STS-12/STM-4
622.08 Mbps</td></tr><tr><td>1</td><td>1</td><td>STS-12/STM-4
622.08 Mbps</td></tr></table>NOTE: These pins have no function in Host Mode.
These pins are provided with internal pull-down.</td></tr>
<tr><td>DATA1RATE[1:0]</td><td>LVTTL, LVCMOS</td><td>I</td><td>113, 114</td></tr>
<tr><td>DATA2RATE[1:0]</td><td>LVTTL, LVCMOS</td><td>I</td><td>50, 49</td></tr>
<tr><td>DATA3RATE[1:0]</td><td>LVTTL, LVCMOS</td><td>I</td><td>48, 47</td></tr>
</table>

<table>
<tr><th>NAME</th><th>LEVEL</th><th>TYPE</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>CDRREFSEL</td><td>LVTTL, LVCMOS</td><td>I</td><td>119</td><td>Clock and Data Recovery Unit Reference Frequency Select
Selects the Clock and Data Recovery Unit reference frequency on REFCLKP/N pins or TTLREFCLK pin based on the table below.
"Low" = 77.76 MHz reference clock
"High" = 19.44 MHz reference clock
<table><tr><th>CDRREFSEL</th><th>REFCLKP/N OR TTLREFCLK FREQUENCY</th><th>CHANNEL 0 - 3 AVAILABLE DATA RATES</th></tr><tr><td>0</td><td>77.76 MHz</td><td rowspan="2">STS-12/STM-4 622.08 Mbps
STS-3/STM-1 155.52 Mbps
STS-1/STM-0 51.84 Mbps</td></tr><tr><td>1</td><td>19.44 MHz</td></tr></table>
NOTE: REFCLKP/N or TTLREFCLK input should be generated from a crystal oscillator which has a frequency accuracy better than 100ppm in order for the received data rate frequency to have the necessary accuracy required for SONET systems.
NOTE: This pin has no function in Host Mode.
This pin is provided with an internal pull-down.</td></tr>
<tr><td>OUTCFG</td><td>LVTTL, LVCMOS</td><td>I</td><td>44</td><td>Output Configuration
Globally selects recovered clock and data outputs to be LVDS or Differential LVPECL on all four channels based on table below.
"Low" = LVDS Standard Output
"High" = Differential LVPECL Standard Output
<table><tr><th>OUTCFG</th><th>Input Configuration</th><th>Output Configuration</th></tr><tr><td>0</td><td>LVDS/ Differential LVPECL</td><td>LVDS</td></tr><tr><td>1</td><td>LVDS/ Differential LVPECL</td><td>Differential LVPECL</td></tr></table>
This pin is provided with an internal pull-down.</td></tr>
<tr><td>CDRDIS0
CDRDIS1
CDRDIS2
CDRDIS3</td><td>LVTTL, LVCMOS</td><td>I</td><td>107
106
56
55</td><td>Clock and Data Recovery Unit Disable
Active "High." Disables internal Clock and Data Recovery unit for respective channel. This enables lower power operation when channel is unused.
"Low" = Internal CDR unit is Enabled
"High" = Internal CDR unit is Disabled
NOTE: These pins have no function in Host Mode.
These pins are provided with internal pull-down.</td></tr>
</table>

NAME	LEVEL	TYPE	PIN	DESCRIPTION
DLOSDIS /SDI	LVTTL, LVCMOS	I	39	**DLOS (Digital Loss of Signal) Disable** **Hardware Mode** Disables internal DLOS monitoring and automatic muting of RXDO[3:0]P/N recovered data output pins upon DLOS detection. DLOS is declared when the incoming data stream has no transition for more than 2.5µs. DLOS is cleared when transitions are detected within a 128µs interval sliding window. "Low" = Monitor & Mute recovered data upon DLOS declaration "High" = Disable internal DLOS monitoring This pin is provided with an internal pull-down. **Host Mode** This pin is functions as the microprocessor Serial Data Input.
POL0 POL1 POL2 POL3	LVTTL, LVCMOS	I	126 124 36 34	**Polarity for SDEXT Input** Controls the Signal Detect polarity convention of SDEXT. "Low" = SDEXT is active "Low." "High" = SDEXT is active "High." ***NOTE:*** *These pins have no function in Host Mode.* These pins are provided with internal pull-down.
SDEXT0 SDEXT1 SDEXT2 SDEXT3	LVTTL, LVCMOS,	I	127 125 35 33	**Signal Detect Input from Optical Module** When inactive, it will immediately declare a Loss of Signal (LOS) condition and assert LOS register bit and mute the activity of the RXDO[3:0]P/N serial data output on the respective channel. "Active" = Normal Operation "Inactive" = LOS Condition (SDEXT detects signal absence) These pins are provided with internal pull-down.
REFCLKP REFCLKN	LVDS, Diff LVPECL	I	117 118	**Reference Clock Input (77.76 MHz or 19.44 MHz)** This differential reference clock input will accept either a 77.76 MHz or a 19.44 MHz LVDS/Differential LVPECL clock source. Pin CDRREFSEL determines the value used as the reference. See Pin CDRREFSEL for more details. REFCLKP/N inputs are internally biased to 1.2V via 15kΩ resistance. These pins are equipped with a 100Ω line-to-line internal termination. ***NOTE:*** *In the event that TTLREFCLK LVTTL/LVCMOS input is used instead of these differential inputs for clock reference, the REFCLKP should be left unconnected and REFCLKN should be tied to GND.*
TTLREFCLK	LVTTL, LVCMOS	I	120	**TTL Reference Clock Input (77.76 MHz or 19.44 MHz)** This optional single-ended clock input reference can be used instead of the differential REFCLKP/N input. It will accept either a 77.76 MHz or a 19.44 MHz LVTTL clock source. Pin CDRREFSEL determines the value used as the reference. See Pin CDRREFSEL for more details. ***NOTE:*** *In the event that REFCLKP/N differential inputs are used instead of this LVTTL/LVCMOS input for clock reference, the TTLREFCLK should be tied to ground.* This pin is provided with an internal pull-down.

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXDI0P RXDI0N RXDI1P RXDI1N RXDI2P RXDI2N RXDI3P RXDI3N	LVDS, Diff LVPECL	I	3 4 11 12 22 21 30 29	**Receive Serial Data Input** The differential receive serial data stream of 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 or 51.84 Mbps STS-1/STM-0 is applied to these differential input pins. These pins accept LVDS or Differential LVPECL input standard. These pins are internally biased to 1.2V via 15kΩ resistance and are equipped with a 100Ω line-to-line internal termination.
RXDO0P RXDO0N RXDO1P RXDO1N RXDO2P RXDO2N RXDO3P RXDO3N	LVDS, Diff LVPECL	O	94 93 86 85 75 76 67 68	**Recovered Serial Data Output** 622.08 Mbps STS-12/STM-4 / 155.52 Mbps STS-3/STM-1 / 51.84 Mbps STS-1/STM-0 differential recovered serial data output that is updated simultaneously on the **falling edge** of the corresponding channel RXCLKO output. User selectable LVDS standard or Differential LVPECL standard output based on OUTCFG pin state.
RXCLKO0P RXCLKO0N RXCLKO1P RXCLKO1N RXCLKO2P RXCLKO2N RXCLKO3P RXCLKO3N	LVDS, Diff LVPECL	O	90 89 82 81 79 80 71 72	**Recovered Clock Output** **(622.08 MHz/ 155.52 MHz/ 51.84 MHz)** 622.08 MHz STS-12/STM-4 / 155.52 MHz STS-3/STM-1 / 51.84 MHz STS-1/STM-0 differential clock output for the corresponding recovered data output RXDO[0:3]P/N. The recovered serial data output port will be updated on the **falling edge** of this clock. User selectable LVDS standard or Differential LVPECL standard output based on OUTCFG pin state.
LOL0 LOL1 LOL2 LOL3	LVCMOS	O	98 99 63 64	**CDR LOL Detect Output** This pin is used to monitor the lock condition of the PLL in the clock and data recovery unit of each channel. "Low" = CDR Locked "High" = CDR Out of Lock
CAP0P CAP0N	Analog	-	109 108	**CDR Non-polarized External Loop Filter Capacitors** **Mode of Operation:** 1. STS12/STM4: CAP[0:3]P/N = 0.47µF ± 10% tolerance 2. STS3/STM1: CAP[0:3]P/N = 0.47µF ± 10% tolerance 3. STS1/STM0: CAP[0:3]P/N = 1.0µF ± 10% tolerance Use type X7R or X5R for improved stability over temperature. (Isolate from noise and place close to pin)
CAP1P CAP1N	Analog	-	103 102	
CAP2P CAP2N	Analog	-	59 60	
CAP3P CAP3N	Analog	-	53 54	

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
AVDD1.8	PWR	42, 57, 58, 104, 105, 123	**1.8V Analog Core Power Supply** AVDD1.8 should be isolated from DVDD1.8 and 3.3V VDD_IO power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD1.8 power supply pins should have bypass capacitors to the nearest ground.
DVDD1.8	PWR	51, 112	**1.8V Digital Core Power Supply** DVDD1.8 should be isolated from AVDD1.8 and 3.3V VDD_IO power supplies. For best results, use an internal power plane separation. The DVDD1.8 power supply pins should have bypass capacitors to the nearest ground.
VDD_IO	PWR	5, 6, 13, 14, 19, 20, 27, 28, 65, 66, 73, 74, 87, 88, 95, 96	**3.3V Input/Output Bus Power Supply** These pins require a 3.3V potential voltage for properly biasing the Differential LVDS/Differential LVPECL and LVCMOS/LVTTL input and output pins. VDD_IO should be isolated from the AVDD1.8 and DVDD1.8 Core power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDD_IO power supply pins should have bypass capacitors to the nearest ground.
GND_IO	GND	7, 8, 15, 16, 17, 18, 25, 26, 69, 70, 77, 78, 83, 84, 91, 92	**Ground for 3.3V VDD Input/Output Power Supplies** It is recommended that all ground pins of this device be tied together.
GND	GND	43, 52, 61, 62, 100, 101, 110, 111, 121	**Power Supply and Thermal Ground** It is recommended that all ground pins of this device be tied together.
NC		1, 2, 9, 10, 23, 24, 31, 32, 97, 128	**No Connect**

SERIAL MICROPROCESSOR INTERFACE

NAME	LEVEL	TYPE	PIN	DESCRIPTION
HOST/$\overline{HW}$	LVTTL, LVCMOS	I	122	**Host or Hardware Mode Select Input** The XRT91L34 offers two modes of operation for interfacing to the device. The Host mode uses a serial microprocessor interface for programming individual registers. The Hardware mode is controlled by the state of the hardware pins set by the user. When left unconnected, by default, the device is configured in the Hardware mode. "Low" = Hardware Mode "High" = Host Mode This pin is provided with an internal pull-down.
$\overline{CS}$	LVTTL, LVCMOS	I	38	**Chip Select Input (Host Mode)** Active "Low" signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial microprocessor is disabled when the chip select signal returns "High". ***NOTES:*** *1. The serial microprocessor interface does **not** support burst mode. Chip Select must be de-asserted after each operation cycle.* *2. Chip Select is only active in Host Mode.* This pin is provided with an internal pull-up.
SCLK	LVTTL, LVCMOS	I	37	**Serial Clock Input (Host Mode Only)** Once $\overline{CS}$ is pulled "Low", the serial microprocessor interface requires 16 clock cycles for a complete Read or Write operation. Serial Clock Input is only active in Host Mode. This pin is provided with an internal pull-down.
DLOSDIS /SDI	LVTTL, LVCMOS	I	39	**Serial Data Input (Host Mode Only)** When $\overline{CS}$ is pulled "Low", the serial data input is sampled on the rising edge of SCLK. Serial Data Input is only active in Host Mode. This pin is provided with an internal pull-down. **Hardware Mode** This pin is functions as the DLOSDIS control pin.
SDO	LVCMOS	O	40	**Serial Data Output (Host Mode Only)** If a Read function is initiated, the serial data output is updated on the falling edge of SCLK8 through SCLK15, with the LSB (D0) updated first. This enables the data to be sampled on the rising edge of SCLK9 through SCLK16. Serial Data Output is only active in Host Mode.
$\overline{INT}$	LVCMOS	O	41	**Interrupt Output (Host Mode Only)** Active "Low" signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". Interrupt Output is only active in Host Mode. ***NOTE:*** *This open-drain output pin requires an external pull-up resistor.*

1.0 FUNCTIONAL DESCRIPTION

The XRT91L34 Quad Channel CDR is designed to operate with a multichannel SONET Framer/ASIC device and provide a high-speed serial clock and data recovery interface to optical networks. The CDR receives differential NRZ serial bit stream running at STS-12/STM-4 or STS-3/STM-1 or STS-1/STM-0, and outputs recovered serial clock and data via differential LVDS/LVPECL drivers. It implements four independently configurable receive clock and data recovery (CDR) units and a LOL and LOS detection circuit (Host Mode Only) for each channel. The CDR is used to provide the front end component of SONET equipment.

1.1 Hardware Mode vs. Host Mode

Functional control of the receiver can be configured by using either Host mode or Hardware mode. Hardware mode is selected by pulling HOST/$\overline{HW}$ "Low" or leaving this pin unconnected. The receiver functionality is then controlled by the hardware pins described in the Hardware Pin Descriptions. Host mode is selected by pulling HOST/$\overline{HW}$ "High". In Host mode the functionality is controlled by programming internal R/W registers using the Serial Microprocessor interface. Host mode offers functions not available in Hardware mode, such as Loss of Signal Monitoring, Interrupt Generation and Disabling of the recovered clock output.

1.2 STS-12/STM-4 and STS-3/STM-1 and STS-1/STM-0 Mode of Operation

The data rate of each receiver channel can be configured by using the appropriate signal level on the DATAnRATE1:0] pins (where n = channel 0, 1, 2, or 3) as shown in **Table 1**.

TABLE 1: CHANNEL DATA RATE SELECTION

DATANRATE[1:0]		DATA RATE SELECTED FOR CHANNEL N
0	**0**	STS-1/STM-0 51.84 Mbps
0	**1**	STS-3/STM-1 155.52 Mbps
1	**0**	STS-12/STM-4 622.08 Mbps
1	**1**	STS-12/STM-4 622.08 Mbps

NOTE: *n denotes channel number.*

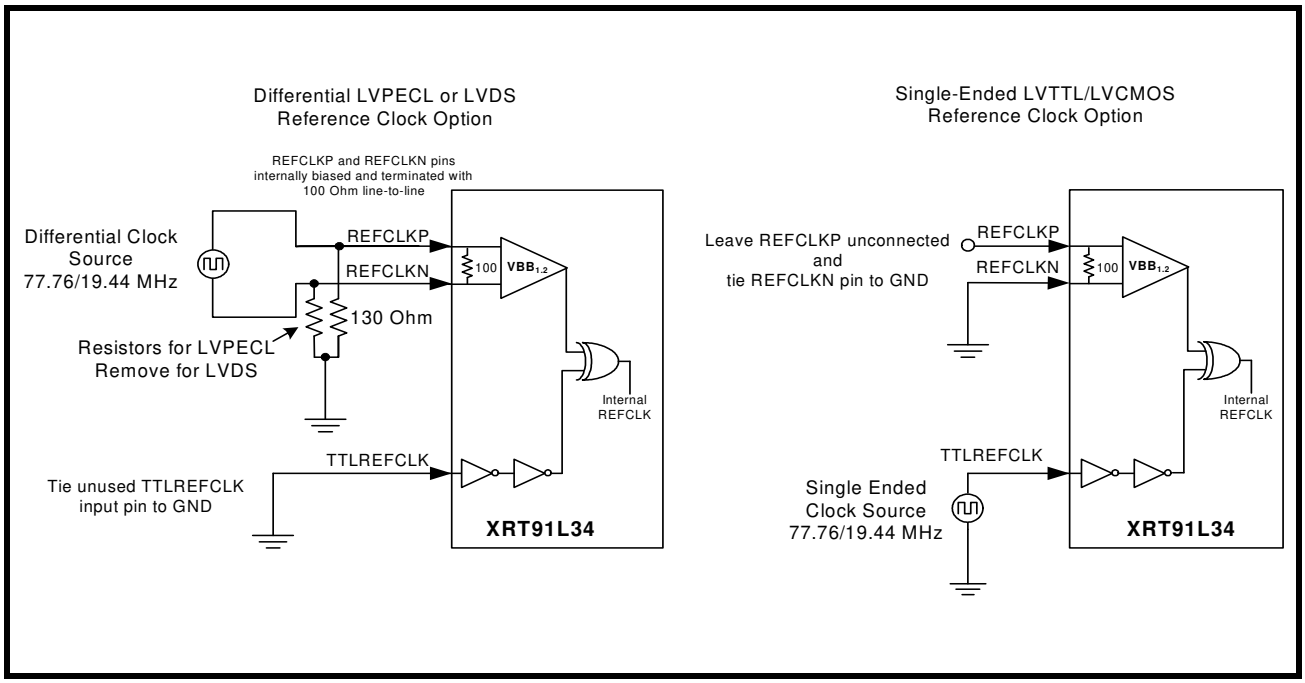
1.3 Reference Clock Input

The XRT91L34 can accept either a 19.44 MHz or 77.76 MHz Differential clock input at REFCLKP/N or a Single-Ended LVTTL clock input at TTLREFCLK. The REFCLKP/N or TTLREFCLK should be generated from a source which has a frequency accuracy better than ±100ppm in order for the CDR Loss of Lock detector to have the necessary accuracy required for SONET systems. The reference clock can be provided with one of two frequencies chosen by CDRREFSEL. The reference frequency options for the XRT91L34 are listed in Table 2. Figure 3 illustrate the reference clock design options.

TABLE 2: CDR REFERENCE FREQUENCY OPTIONS (LVDS/ DIFF LVPECL OR SINGLE-ENDED LVTTL/LVCMOS)

CDRREFSEL	REFCLKP/N OR TTLREFCLK FREQUENCY	CHANNEL 0 - 3 AVAILABLE DATA RATES
0	77.76 MHz	STS-1/STM-0 51.84 Mbps STS-3/STM-1 155.52 Mbps STS-12/STM-4 622.08 Mbps
1	19.44 MHz	

FIGURE 3. REFERENCE CLOCK DESIGN OPTIONS



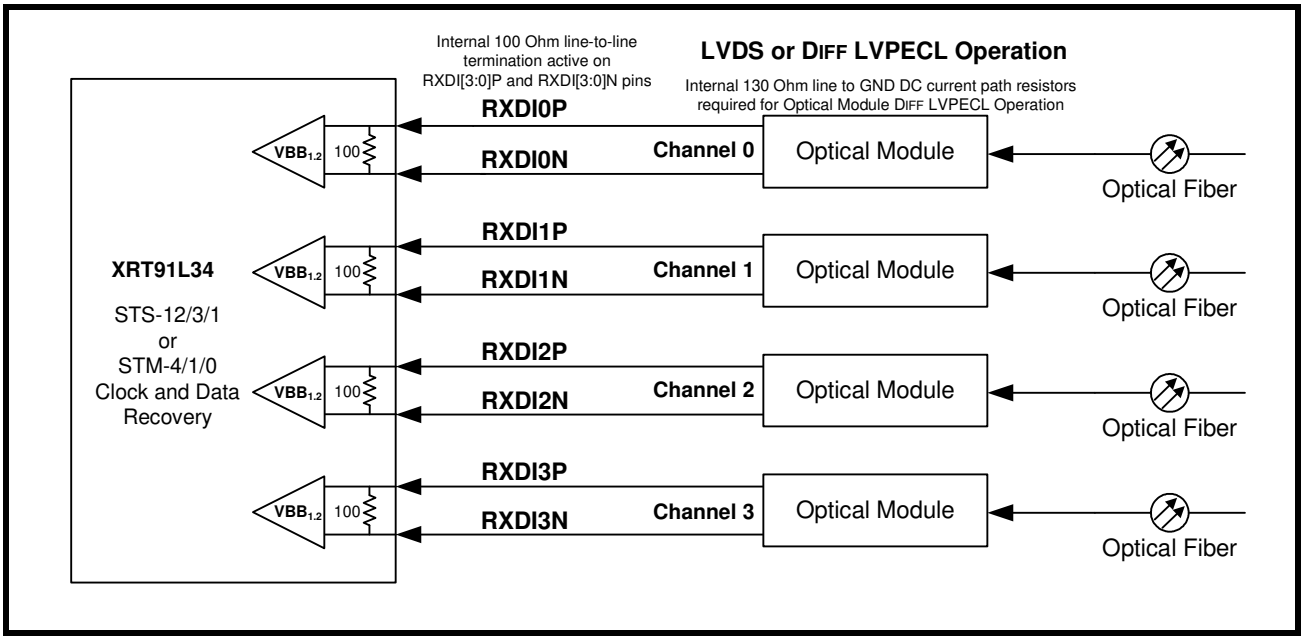
2.0 RECEIVE SECTION

The receive section of XRT91L34 includes four differential input buffers RXDI[3:0]P/N, followed by clock and data recovery units (CDR) and recovered serial data and clock differential output drivers. The receiver accepts the high speed Non-Return to Zero (NRZ) serial data at 622.08/155.52/51.84 Mbps through the input interfaces RXDI[3:0]P/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming data stream. The recovered serial data is presented to the RXDO[3:0]P/N differential output driver interface. The high-speed recovered clock RXCLKO[3:0]P/N, is used to synchronize the transfer of the RXDO[3:0]P/N data with the receive portion of a framer/mapper device. The recovered data RXDO[3:0]P/N and clock RXCLKO[3:0]P/N differential output driver interfaces are designed for ultimate flexibility by supporting either LVDS or Differential LVPECL protocol level. Upon initialization or loss of signal or loss of lock, the external reference clock signal of 19.44 MHz or 77.76 MHz is used to start-up the clock recovery phase-locked loop for proper operation. The included CDR blocks in the XRT91L34 can be individually disabled by asserting the CDRDIS[3:0] pins to permit the flexibility of powering down unused channels.

2.1 Receive Serial Input

The receive serial inputs are applied to RXDI[3:0]P/N. The XRT91L34 includes internal termination, this has the advantage of reducing the number of external board components. The XRT91L34 terminates the receive inputs using 100Ω line-to-line method of termination. Differential LVPECL operation of receive inputs can be supported, provided each optical module Differential LVPECL output pin must have a 130Ω DC current path resistor to GND whether internally or externally. A simplified LVDS/Differential LVPECL DC coupling block diagram is shown in **Figure 4**.

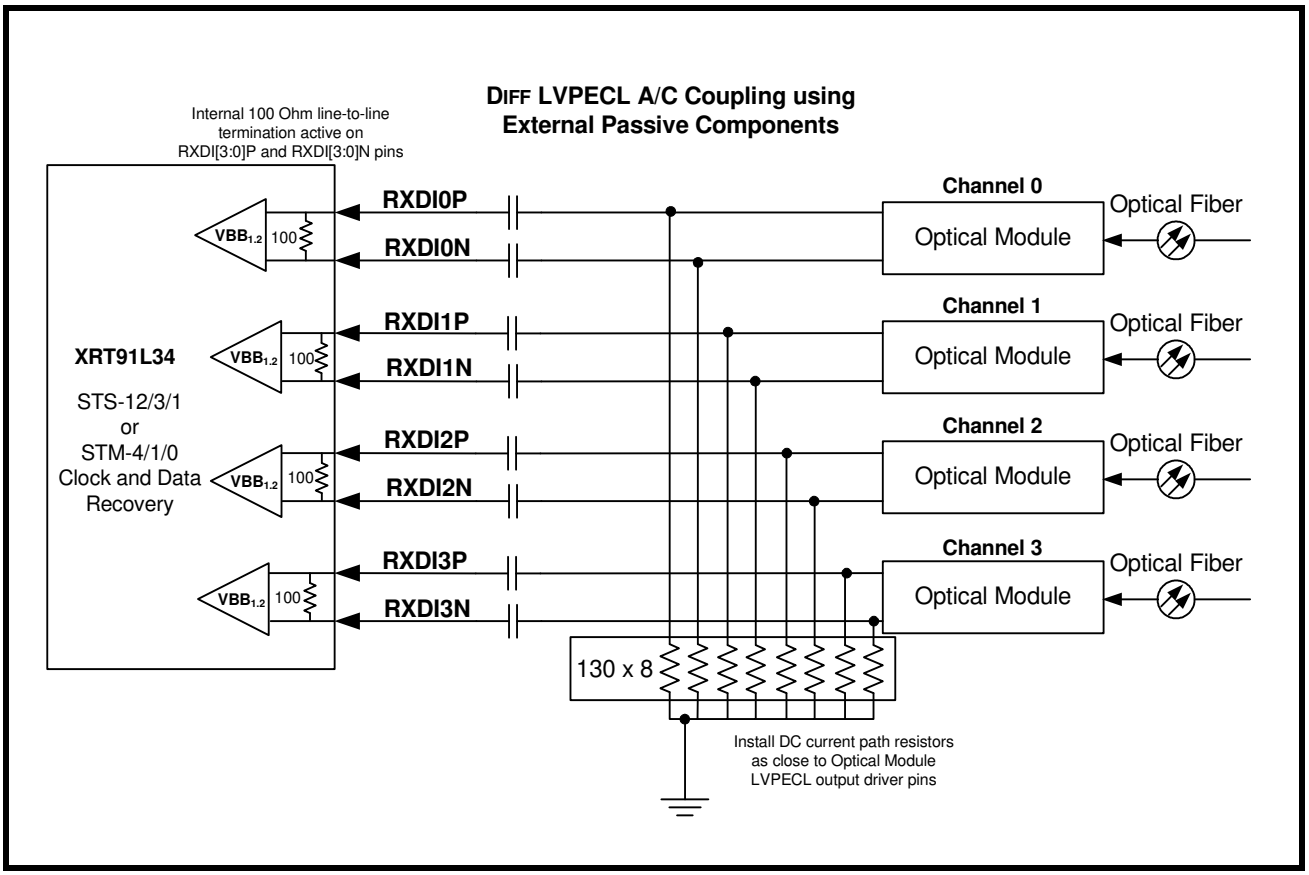
FIGURE 4. RECEIVE SERIAL INPUT INTERFACE USING LVDS/DIFF LVPECL DC COUPLING INTERNAL TERM



NOTE: Some optical modules integrate AC coupling capacitors and DC current path resistors internally within the module. AC or DC coupling is largely specific to system design and optical module of choice.

The receive serial inputs can also be AC coupled to an optical module or an electrical interface. A simplified Differential LVPECL AC coupling using external passive components block diagram is shown in Figure 5.

FIGURE 5. RECEIVE SERIAL INPUT INTERFACE USING DIFF LVPECL AC COUPLING INTERNAL TERMINATION



NOTE: *Some optical modules integrate AC coupling capacitors and DC current path resistors internally within the module.*

2.2 Receive Clock and Data Recovery

The clock and data recovery (CDR) unit accepts the high speed NRZ serial data from the Differential receiver and generates a clock that is the same frequency as the incoming data. The clock recovery block utilizes the reference clock from REFCLKP/N or TTLREFCLK to train and monitor its clock recovery PLL. Upon startup, the PLL locks to the local reference clock. Once this is achieved, the PLL then attempts to lock onto the incoming receive serial data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch to the local reference clock, declare a Loss of Lock and output a high level signal on the LOL output pin. Whenever a Loss of Lock (LOL) or a Loss of Signal (LOS) event occurs, the CDR will continue to supply a receive clock (based on the local reference). When the SDEXT becomes active and internal DLOS is cleared and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source, the clock recovery PLL will switch back to the incoming receive serial data stream. Table 3 specifies the Clock and Data Recovery Unit performance characteristics.

TABLE 3: CLOCK AND DATA RECOVERY UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	40		60	%
REF_{TOL}	Reference clock frequency tolerance[2]	-100		+100	ppm
TOL_{JIT}	Input jitter tolerance with 1 MHz < f < 20 MHz PRBS pattern	0.3	0.4		UI
$OCLK_{DUTY}$	Clock output duty cycle	45		55	%

Jitter specification is defined using a 12kHz to 0.4/1.3/5MHz LP-HP single-pole filter.

[1]These reference clock jitter limits are required for the outputs to meet SONET system level jitter requirements (<10 mUI_{rms}).

[2]Required to meet SONET output frequency stability requirements.

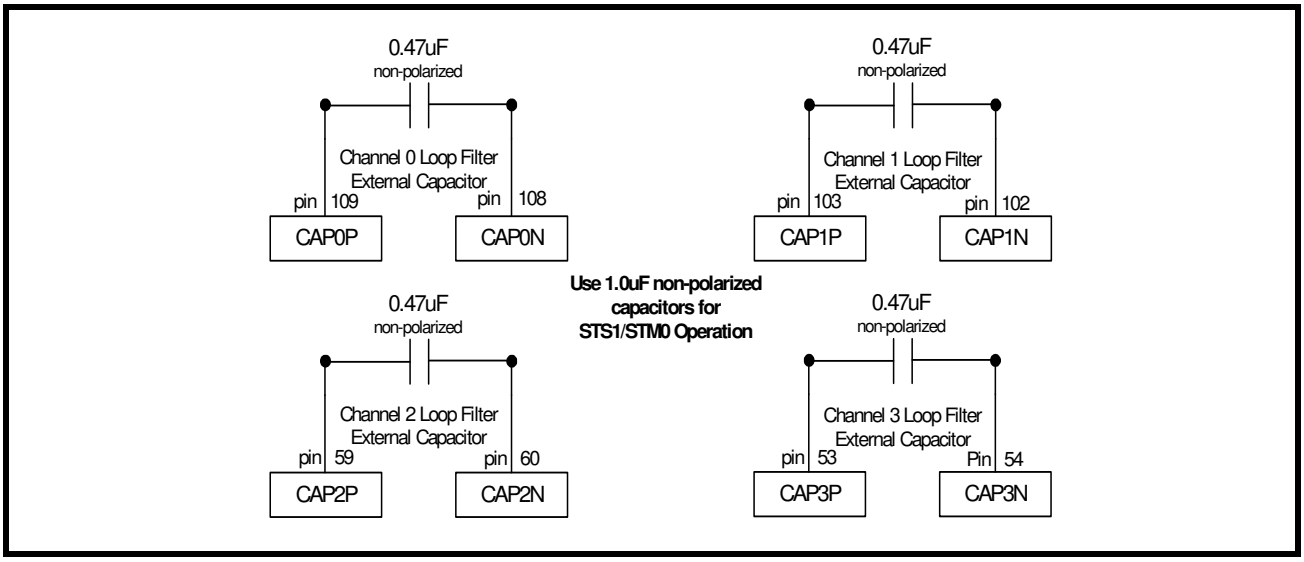
2.2.1 Internal Clock and Data Recovery Disable

Optionally, each of the four internal CDR unit can be disabled and powered down when the channel is not in use. Asserting the CDRDISn pin (where n = channel 0, 1, 2, or 3) "High" in Hardware Mode or setting CDRDISn bit (where n = channel 0, 1, 2, or 3) in Host Mode, disables the internal Clock and Data Recovery unit for that particular channel.

2.3 External Receive Loop Filter Capacitors

For STS12/STM4 and STS3/STM1 operation, use 0.47µF (or greater) non-polarized external loop filter capacitors to achieve the required receiver jitter performance for each of the channels. For STS1/STM0 operation, use a minimum of 1.0µF non-polarized capacitors. If all 3 data rates STS12/STS3/STS1 are required in an application, then use 1uF loop filter capacitors. They must be well isolated to prohibit noise entering the CDR block and should be placed as close to the pins as possible. **Figure 6** shows the pin connections and external loop filter components. These four non-polarized capacitors should be of +/- 10% tolerance. Use type X7R or X5R capacitors for improved stability over temperature.

FIGURE 6. EXTERNAL LOOP FILTERS



2.4 Internal Digital Loss of Signal and External Signal Detection

XRT91L34 has an integrated Digital Loss of Signal (DLOS) circuit and supports external Signal Detection (SDEXT) for detecting and determining received signal integrity. The internal DLOS circuit monitors the incoming data stream. If the incoming data stream has no transition for more than 2.5µs, Loss of Signal is declared. This LOS condition will be cleared when the circuit detects transitions in a 128µs interval sliding window. Pulling the DLOSDIS pin signal to a high level in hardware mode or setting DLOSDIS bit in host mode will disable the internal DLOS detection circuit to permit the framer/mapper interface to determine the Loss of Signal declaration and clearance criteria for specific applications. The external Signal Detect function is supported by the SDEXT input. An LVCMOS/LVTTL signal comes from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices, the polarity of this signal can be either active "Low" or active "High." The SDEXT and POL inputs are Exclusive OR’ed to determine external Loss of Signal (LOS) condition. In the event that internal DLOS is detected or an external SDEXT input indicates signal absence, the recovered serial data output will be forced to a logic state "0," and the LOS status register is set whenever the host mode serial microprocessor interface is active. This acts as a receive data mute upon LOS function to prevent data chattering and to prevent random noise from being misinterpreted as valid incoming data. **Figure 7** shows the Loss of Signal Detection logic circuit. **Table 4** specifies LOS declaration polarity settings.

FIGURE 7. LOSS OF SIGNAL DECLARATION CIRCUIT

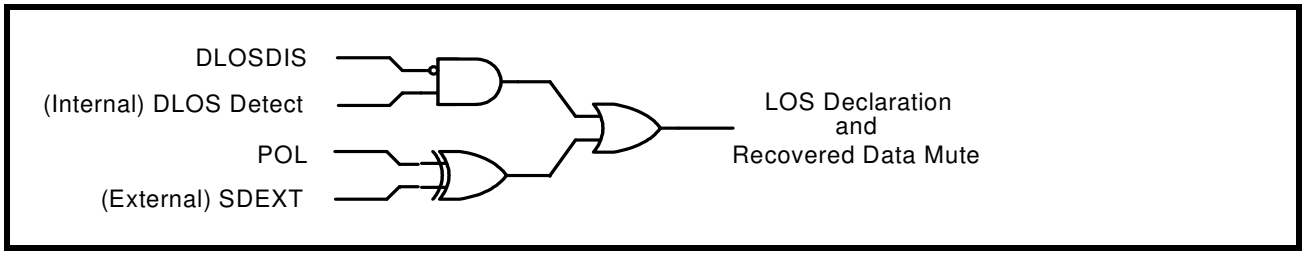


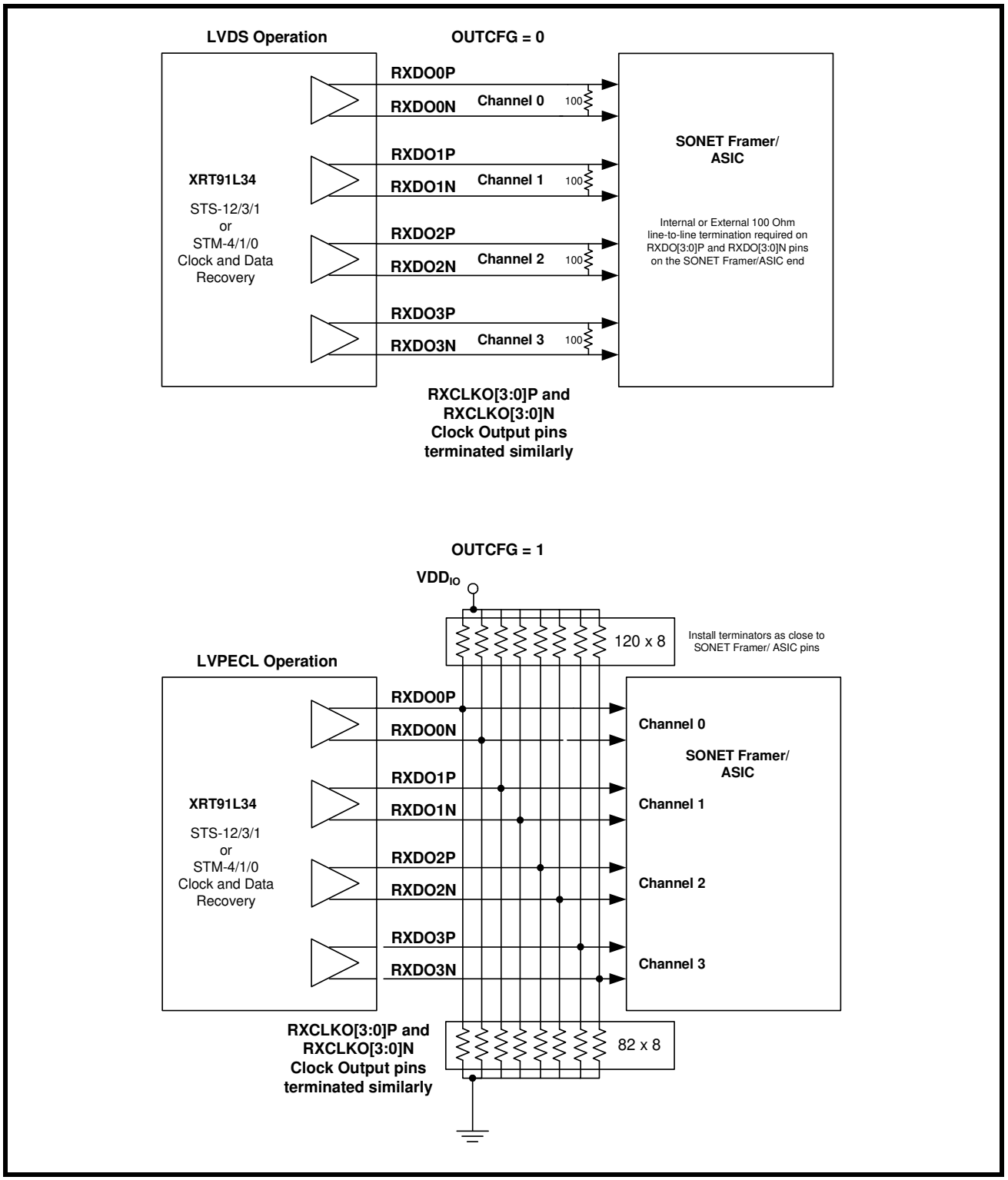
TABLE 4: EXTERNAL LOS DECLARATION POLARITY SETTING

SDEXT	POL	INTERNAL SIGNAL DETECT	LOS BIT STATE (HOST MODE ONLY)	RXDO[3:0]P/N
0	**0**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module.	Low	Normal Operation
0	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module.	High **LOS declared**	Muted
1	**0**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module.	High **LOS declared**	Muted
1	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module.	Low	Normal Operation

2.5 Multichannel Recovered Output Interface

The recovered data RXDO[3:0]P/N differential output drivers along with the recovered clock RXCLKO[3:0]P/N differential output drivers can be configured for LVDS or Differential LVPECL standard operation. In addition, Host Mode operation permits each of the channelized recovered clock output to be independently disabled such as in repeater applications to save power.

FIGURE 8. MULTICHANNEL RECOVERED OUTPUT INTERFACE BLOCK



2.6 Differential Recovered Data Output Timing

The differential recovered data and clock outputs operating at the STS-12/STM-4 or STS-3/STM-1 or STS-1/STM-0 datarates will adhere to the data valid output timing shown in Figure 9 ,Table 5, Table 6, and Table 7.

FIGURE 9. DIFFERENTIAL RECOVERED OUTPUT TIMING

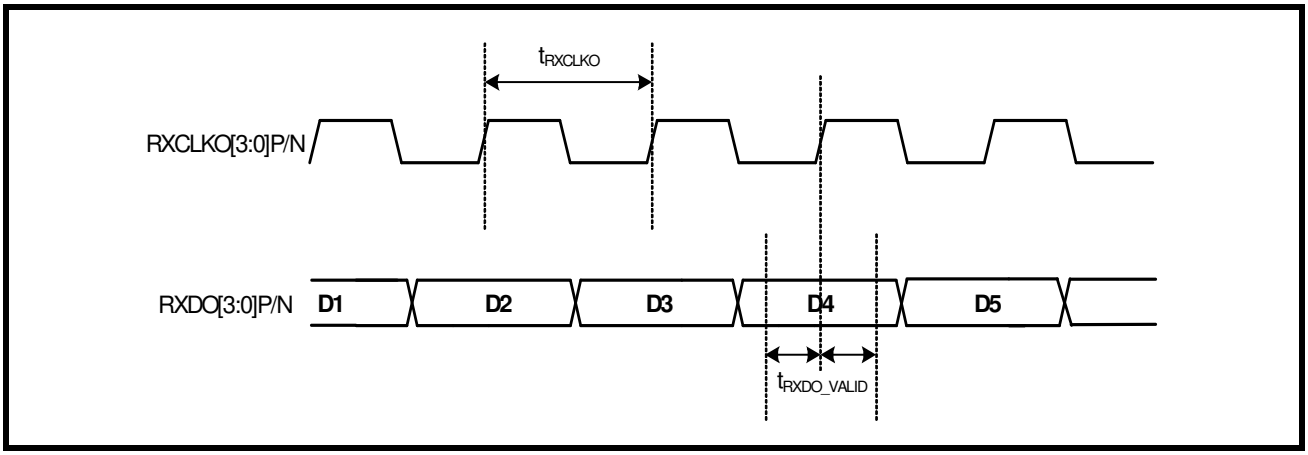


TABLE 5: RECOVERED DATA OUTPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLKO}	Recovered high-speed output clock period		1.608		ns
t_{RXDO_VALID}	Time the data is valid on RXDO[3:0]P/N before and after the rising edge of RXCLKO[3:0]P/N	0.5			ns

TABLE 6: RECOVERED DATA OUTPUT TIMING (STS-3/STM-1 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLKO}	Recovered high-speed output clock period		6.43		ns
t_{RXDO_VALID}	Time the data is valid on RXDO[3:0]P/N before and after the rising edge of RXCLKO[3:0]P/N	2.8			ns

TABLE 7: RECOVERED DATA OUTPUT TIMING (STS-1/STM-0 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLKO}	Recovered high-speed output clock period		19.29		ns
t_{RXDO_VALID}	Time the data is valid on RXDO[3:0]P/N before and after the rising edge of RXCLKO[3:0]P/N	8.3			ns

3.0 JITTER PERFORMANCE

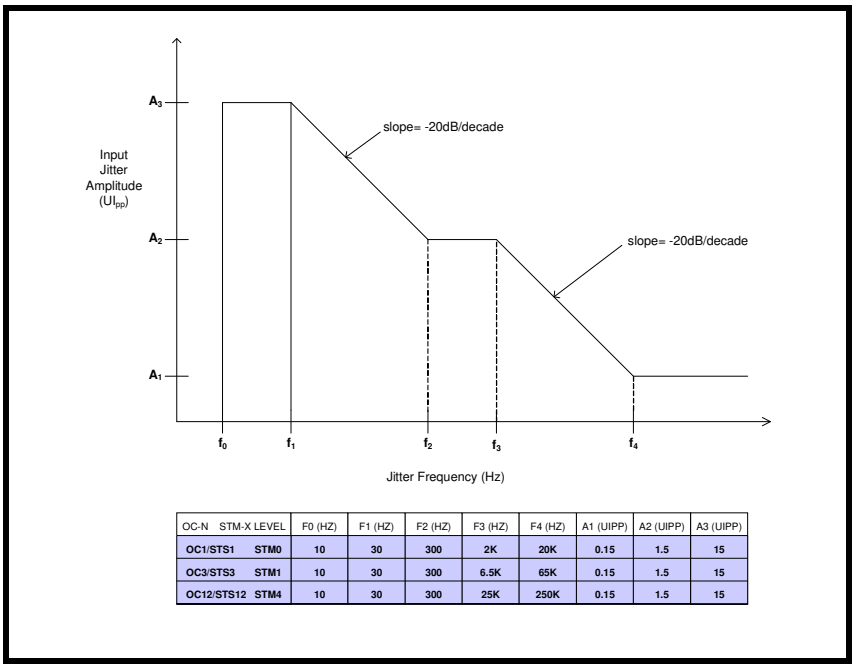
3.1 SONET Jitter Requirements

SONET receive equipment jitter requirements are specified jitter tolerance and jitter transfer. The definitions of each of these types of jitter are given below.

3.1.1 Rx Jitter Tolerance:

OC-1/STM-0, OC-3/STM-1, and OC-12/STM-4 category II SONET interfaces should tolerate, the input jitter applied according to the mask of **Figure 10**, with the corresponding parameters specified in the figure.

FIGURE 10. GR-253/G.783 JITTER TOLERANCE MASK



OC-N STM-X LEVEL	F0 (HZ)	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (HZ)	A1 (UIPP)	A2 (UIPP)	A3 (UIPP)
OC1/STS1 STM0	10	30	300	2K	20K	0.15	1.5	15
OC3/STS3 STM1	10	30	300	6.5K	65K	0.15	1.5	15
OC12/STS12 STM4	10	30	300	25K	250K	0.15	1.5	15

FIGURE 11. XRT91L34 MEASURED JITTER TOLERANCE AT 51.84 MBPS STS-1/STM-0

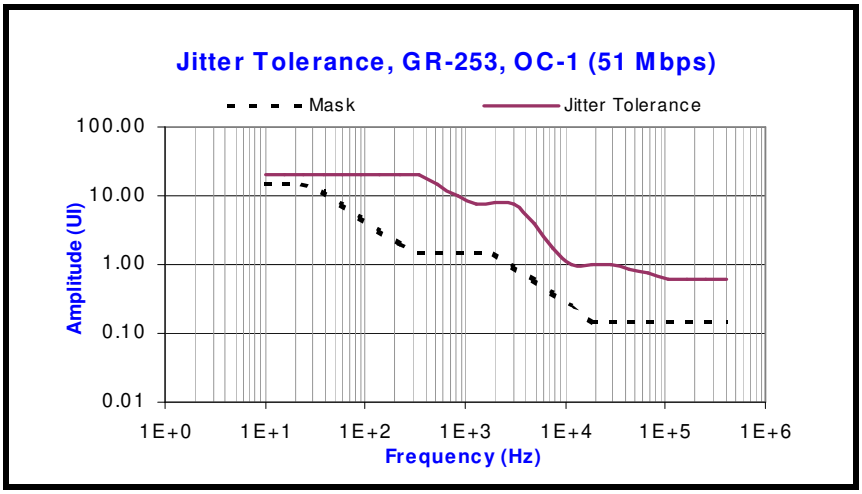


FIGURE 12. XRT91L34 MEASURED JITTER TOLERANCE AT 155.52 MBPS STS-3/STM-1

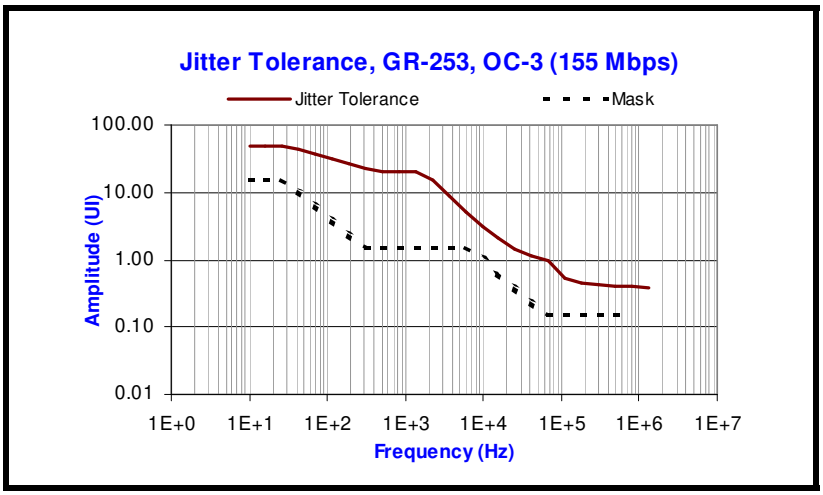
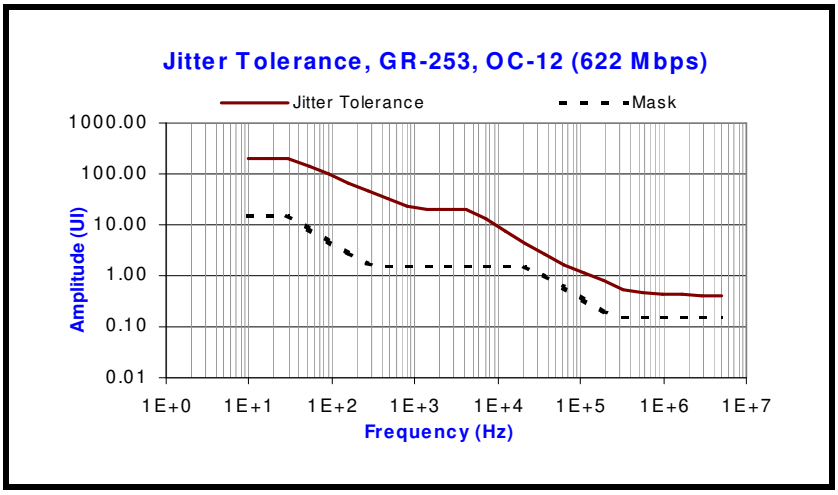


FIGURE 13. XRT91L34 MEASURED JITTER TOLERANCE AT 622.08 MBPS STS-12/STM-4



3.1.2 Rx Jitter Transfer

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency. It displays the ability of the component unit to attenuate jitter at the specified injected jitter frequencies. There are two distinct characteristics in jitter transfer, jitter gain (jitter peaking) defined as the highest ratio above 0dB and jitter transfer bandwidth. The overall jitter transfer bandwidth is controlled by a low bandwidth loop.

The XRT91L34 meets the latest jitter transfer characteristics as shown in the Figure 14, Figure 15, and Figure 16. The XRT91L34 complies with STS-12/3/1 and STM-4/1/0 jitter transfer masks set forth by Bellcore GR-253 Core section 5.6.2.1 and ITUT G.783 section 15.1.3 as defined in G.825.

FIGURE 14. XRT91L34 MEASURED JITTER TRANSFER AT 51.84 MBPS STS-1/STM-0

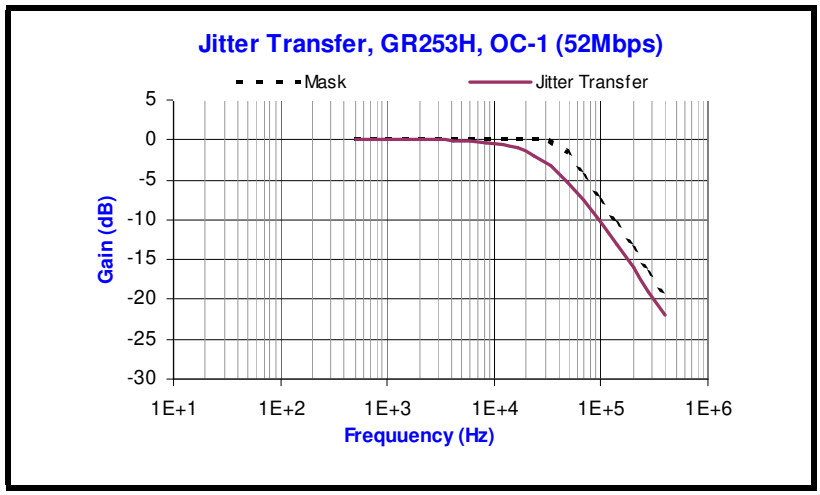


FIGURE 15. XRT91L34 MEASURED JITTER TRANSFER AT 155.52 MBPS STS-3/STM-1

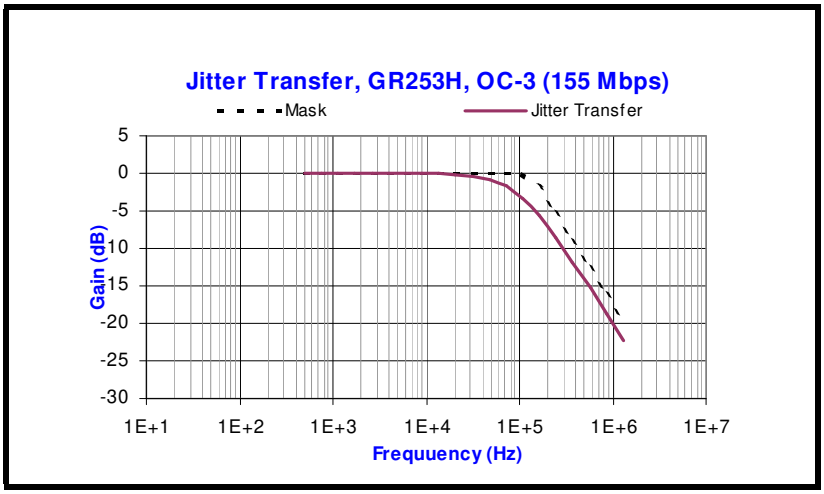
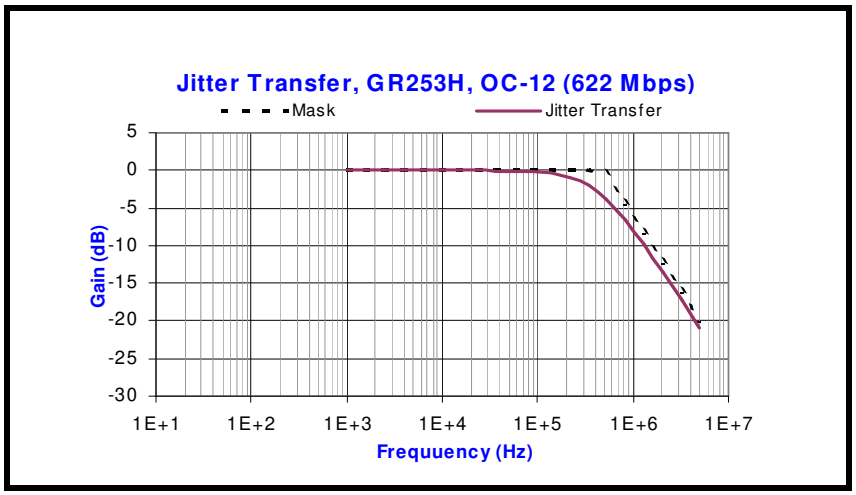


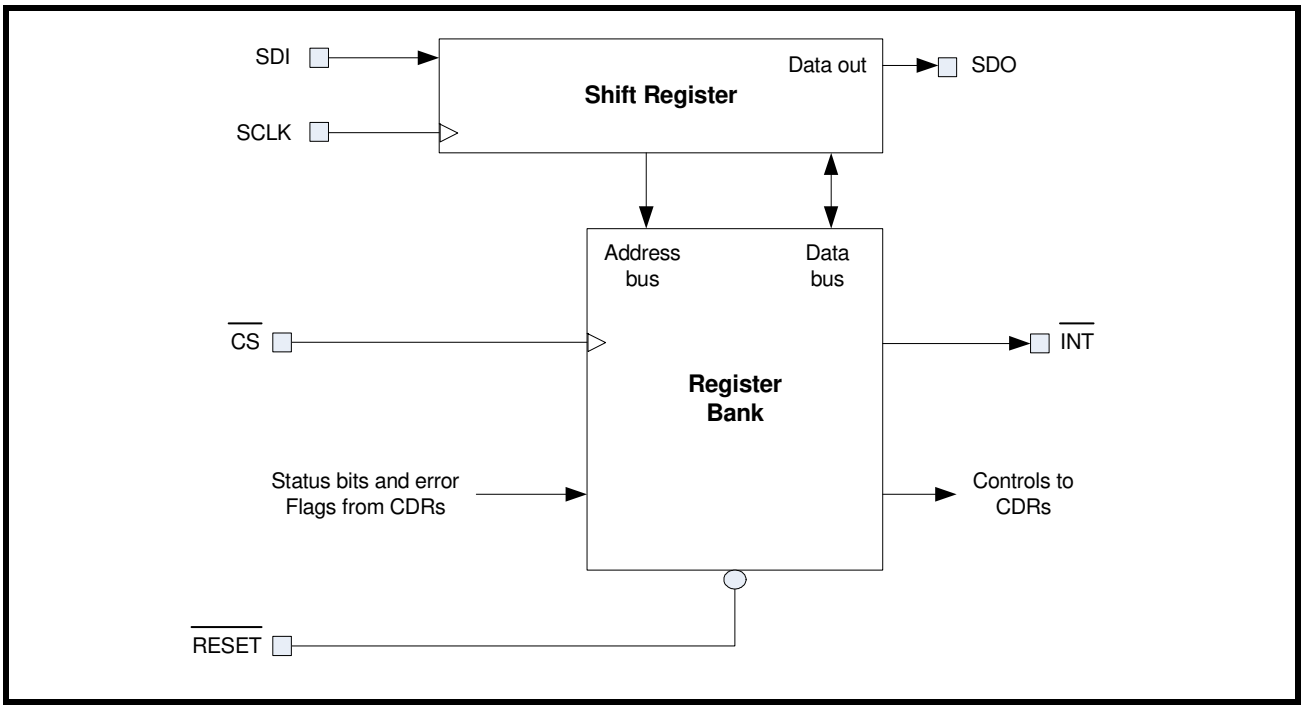
FIGURE 16. XRT91L34 MEASURED JITTER TRANSFER AT 622.08 MBPS STS-12/STM-4



4.0 SERIAL MICROPROCESSOR INTERFACE BLOCK

The Serial Microprocessor Interface uses a standard 3-pin serial port with $\overline{CS}$, SCLK, and SDI for programming the device. Optional pins such as SDO, $\overline{INT}$, and $\overline{RESET}$ allow the ability to read back contents of the registers, monitor the device via an interrupt pin, and reset the device to its default configuration by pulling reset "Low" for more than 10ns. A simplified block diagram of the Serial Microprocessor Interface is shown in Figure 17.

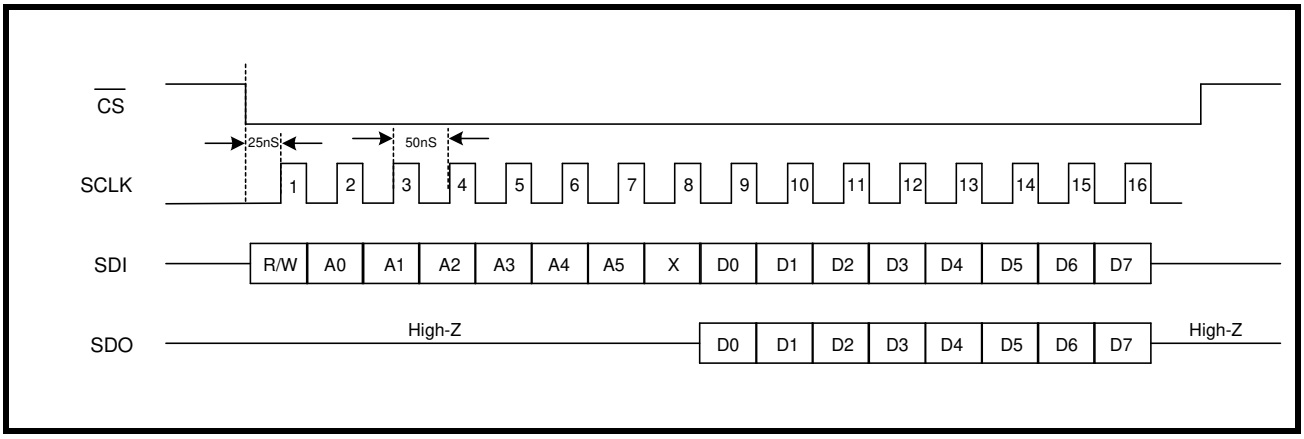
FIGURE 17. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



4.1 SERIAL TIMING INFORMATION

The serial port requires 16 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor Interface samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 16 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor Interface is shown in Figure 18.

FIGURE 18. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



*NOTE: The serial microprocessor interface does **NOT** support "burst write" or "burst read" operations. Chip Select (active "Low") **must be de-asserted** at the end of each write or read operation.*

4.2 16-BIT SERIAL DATA INPUT DESCRITPTION

The serial data input is sampled on the rising edge of SCLK. For read operations, the SDO signal is updated on the falling edge of SCLK. The serial data must be applied to the serial port LSB first. The 16 bits of serial data are described below.

4.2.1 R/W (SCLK1)

The first serial bit applied to the device SDI pin determines whether a Read or Write operation is desired. If the R/W bit is set to "0", the serial port is configured for a Write operation. If the R/W bit is set to "1", the serial port is configured for a Read operation.

4.2.2 A[5:0] (SCLK2 - SCLK7)

The next 6 SCLK cycles are used to provide the address to which a Read or Write operation will occur. A0 (LSB) must be sent to the SDI pin first followed by A1 and so forth until all 6 address bits have been sampled by SCLK.

4.2.3 X (Dummy Bit SCLK8)

The dummy bit sampled by SCLK8 is used to allow sufficient time for the serial data output pin to update data if the readback mode is selected by setting R/W = "1". Therefore, the state of this bit is ignored and can hold either "0" or "1" during both Read and Write operations.

4.2.4 D[7:0] (SCLK9 - SCLK16)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. D0 (LSB) must be sent to the SDI pin first followed by D1 and so forth until all 8 data bits have been sampled by SCLK. Once 16 SCLK cycles have been complete, the data is held until $\overline{CS}$ is pulled "High" whereby, the serial port latches the data into the selected internal register.

4.3 8-BIT SERIAL DATA OUTPUT DESCRIPTION

When R/W is set to "1" (Read operation) the serial data output is updated on the falling edge of SCLK8 - SCLK16, D0 (LSB) is provided at the SDO pin on the falling edge of SCLK8, followed by D1 and so forth until all 8 data bits have been updated after which the SDO output pin returns to a high impedance state until the next read operation.