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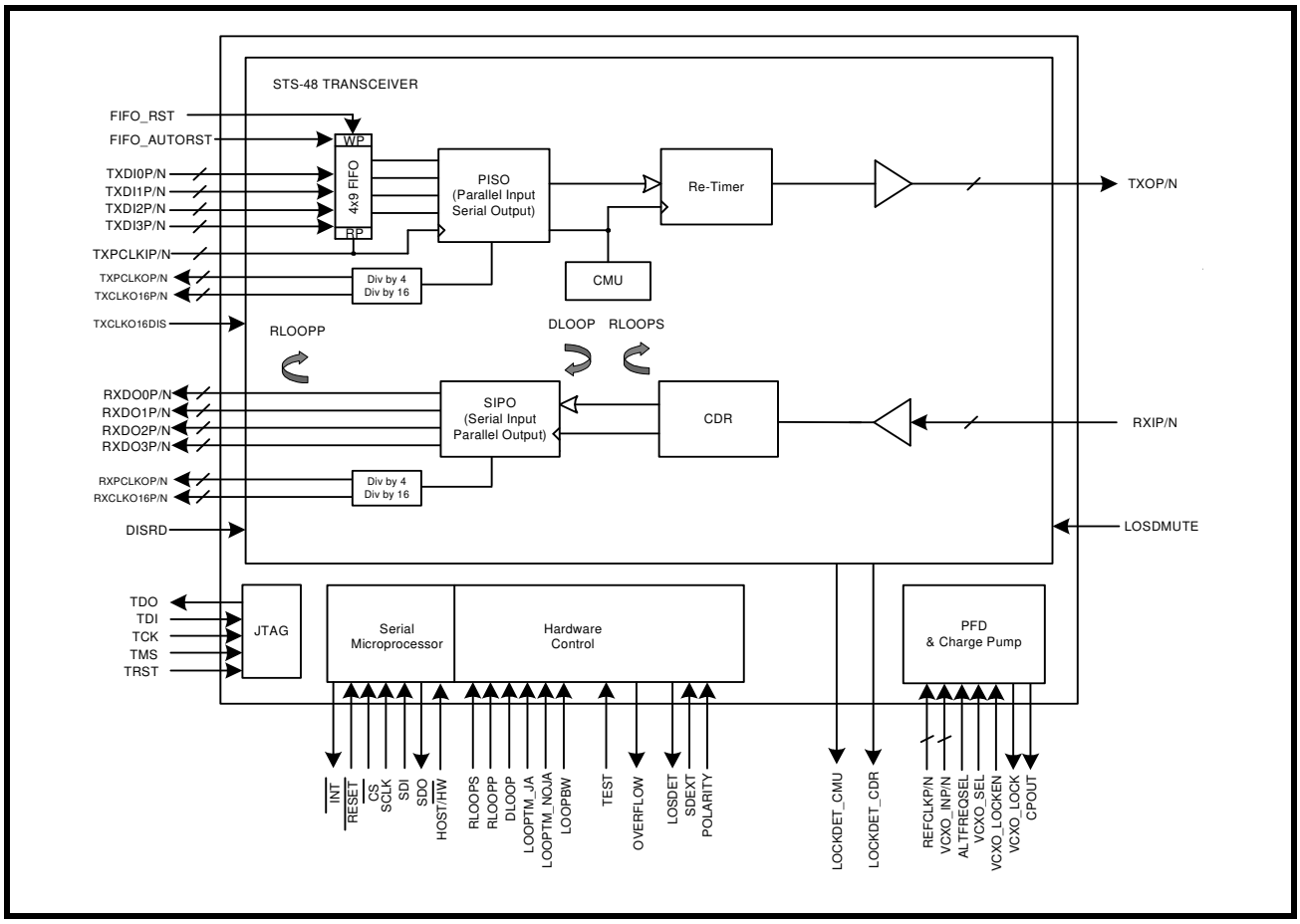
## GENERAL DESCRIPTION

The XRT91L80 is a fully integrated SONET/SDH transceiver for SONET OC-48/STM-16 applications supporting the use of Forward Error Correction (FEC) capability. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from a slower external clock reference. It also provides Clock and Data Recovery (CDR) functions by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The chip provides serial-to-parallel and parallel-to-serial converters and 4-bit LVDS system interfaces in both receive and transmit directions. The transmit section includes a 4x9 Elastic Buffer (FIFO) to absorb any phase differences between the transmitter clock input and the internally generated transmitter reference clock. In the event of an overflow, an internal FIFO control circuit outputs an OVERFLOW indication. The FIFO under the control of the FIFO_AUTORST pin can automatically recover from an overflow condition. The operation of the device can be monitored by checking the status of the LOCKDET_CMU, LOCKDET_CDR, and LOSDET output signals. An on-chip phase/frequency detector and charge-pump offers the ability to form a de-jittering PLL with an external VCXO that can be used in loop timing mode to clean up the recovered clock in the receive section.

### *APPLICATIONS*

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches and Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

**FIGURE 1. BLOCK DIAGRAM OF XRT91L80**



### *FEATURES*

- 2.488 / 2.666 Gbps Transceiver
- Targeted for SONET OC-48/SDH STM-16 Applications
- Selectable full duplex operation between standard rate of 2.488 Gbps or Forward Error Correction rate of 2.666 Gbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, and clock data recovery (CDR) functions
- 4-bit LVDS signaling data paths running at 622.08/666.51 Mbps compliant with OIF SFI-4 Implimentation Agreement
- Non-FEC and FEC rate REFCLKP/N single reference input port
- Supports 77.76/83.31 MHz or 155.52/166.63 MHz transmit and receive external reference input port
- Optional VCXO input port support multiple de-jittering modes
- On-chip phase detector and charge pump for external VCXO based de-jittering PLL
- Internal FIFO decouples transmit parallel clock input and transmit parallel clock output
- Provides Local, Remote Serial, Remote Parallel and Split Loopback modes as well as Loop Timing mode
- Diagnostics features include various lock detect functions and transmit CMU and receive CDR Lock Detect
- Host mode serial microprocessor interface simplifies monitor and control
- Meets Telcordia, ANSI and ITU-T jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, GR-253 CORE, GR-253 ILR SONET Jitter specifications.
- Operates at 1.8V CMOS and CML with 3.3V I/O
- 490mW Typical Power Dissipation
- Package: 12 x 12 mm 196-pin STBGA
- IEEE 1149.1 Compatable JTAG port

## PRODUCT ORDERING INFORMATION

| PRODUCT NUMBER | PACKAGE TYPE | OPERATING TEMPERATURE RANGE |
|---|---|---|
| XRT91L80IB | 196 STBGA | -40℃ to +85℃ |

**FIGURE 2. 196 BGA PINOUT OF THE XRT91L80 (TOP VIEW)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | AGND_RX | TRST | LOSDMUTE | NC | DGND | RXCLKO16P | RXCLKO16N | VDD3.3 | SDI | $\overline{CS}$ | RLOOPP | DGND | VDD1.8 | RXDO3P |
| B | AGND_RX | AGND_RX | DGND | NC | SDEXT | DLOOP | VDD1.8 | DGND | SCLK | $\overline{RESET}$ | TDO | DGND | VDD1.8 | RXDO3N |
| C | RXIP | AGND_RX | AGND_RX | POLARITY | LOSDET | LOOPTM_JA | LOCKDET_CDR | SDO | HOST/$\overline{HW}$ | RLOOPS | $\overline{INT}$ | DISRD | RXDO2P | RXDO1P |
| D | RXIN | AGND_RX | AVDD3.3_RX | AVDD1.8_RX | AVDD1.8_RX | AVDD1.8_RX | AGND_RX | AVDD1.8_RX | VDD3.3 | VDD3.3 | VDD3.3 | VDD1.8 | RXDO2N | RXDO1N |
| E | AGND_RX | AGND_RX | AVDD3.3_RX | AGND_RX | TGND | TGND | TGND | TGND | TGND | TGND | VDD3.3 | VDD1.8 | RXDO0P | RXPCLKOP |
| F | XRES1N | AGND_RX | AVDD1.8_RX | AGND_RX | TGND | TGND | TGND | TGND | TGND | TGND | DGND | DGND | RXDO0N | RXPCLKON |
| G | XRES1P | AGND_RX | AVDD1.8_RX | AGND_RX | TGND | TGND | TGND | TGND | TGND | TGND | DGND | DGND | DGND | DGND |
| H | AGND_RX | AGND_RX | AGND_RX | AGND_RX | TGND | TGND | TGND | TGND | TGND | TGND | DGND | DGND | TXDI0P | TXPCLKIP |
| J | AVDD1.8_TX | AGND_TX | AGND_TX | AVDD1.8_TX | TGND | TGND | TGND | TGND | TGND | TGND | DGND | DGND | TXDI0N | TXPCLKIN |
| K | TXOP | AGND_TX | AGND_TX | AGND_TX | TGND | TGND | TGND | TGND | TGND | TGND | VDD1.8 | DGND | TXDI2P | TXDI1P |
| L | TXON | AGND_TX | DGND | AGND_TX | AGND_TX | AVDD1.8_TX | AVDD1.8_TX | AVDD1.8_TX | VDD1.8 | VDD1.8 | DGND | DGND | TXDI2N | TXDI1N |
| M | AGND_TX | AVDD1.8_TX | AVDD1.8_TX | AGND_TX | AGND_TX | VCXO_SEL | LOOPBW | TDI | VDD1.8 | VDD1.8 | VDD1.8 | TXCLKO16DIS | OVERFLOW | TXDI3P |
| N | TMS | LOCKDET_CMU | TCK | VCXO_INN | AGND_TX | REFCLKN | AGND_TX | VCXO_LOCK | AVDD1.8_TX | TXCLKO16P | TXCLKO16N | FIFO_AUTORST | FIFO_RST | TXDI3N |
| P | ALTFREQSEL | LOOPTM_NOJA | VCXO_LOCKEN | VCXO_INP | AVDD3.3_TX | REFCLKP | AGND_TX | CPOUT | AVDD3.3_TX | TXPCLKOP | TXPCLKON | DGND | VDD3.3 | VDD3.3 |

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# PIN DESCRIPTIONS

### *SERIAL MICROPROCESSOR INTERFACE*

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| HOST/$\overline{HW}$ | LVTTL, LVCMOS | I | C9 | **Host or Hardware Mode Select Input**<br>The XRT91L80 offers two modes of operation for interfacing to the device. The Host mode uses a serial microprocessor interface for programming individual registers. The Hardware mode is controlled by the state of the hardware pins set by the user. When left unconnected, by default, the device is configured in the Hardware mode.<br>"Low" = Hardware Mode<br>"High" = Host Mode<br>This pin is provided with an internal pull-down. |
| $\overline{CS}$ | LVTTL, LVCMOS | I | A10 | **Chip Select Input (Host Mode Only)**<br>Active "Low" signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial microprocessor is disabled when the chip select signal returns "High".<br>***NOTE:*** *The serial microprocessor interface does **not** support burst mode. Chip Select must be de-asserted after each operation cycle.*<br>This pin is provided with an internal pull-up. |
| SCLK | LVTTL, LVCMOS | I | B9 | **Serial Clock Input (Host Mode Only)**<br>Once $\overline{CS}$ is pulled "Low", the serial microprocessor interface requires 16 clock cycles for a complete Read or Write operation.<br>This pin is provided with an internal pull-down. |
| SDI | LVTTL, LVCMOS | I | A9 | **Serial Data Input (Host Mode Only)**<br>When $\overline{CS}$ is pulled "Low", the serial data input is sampled on the rising edge of SCLK.<br>This pin is provided with an internal pull-down. |
| SDO | LVCMOS | O | C8 | **Serial Data Output (Host Mode Only)**<br>If a Read function is initiated, the serial data output is updated on the falling edge of SCLK8 through SCLK15, with the LSB (D0) updated first. This enables the data to be sampled on the rising edge of SCLK9 through SCLK16. |
| $\overline{INT}$ | LVCMOS | O | C11 | **Interrupt Output (Host Mode Only)**<br>Active "Low" signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High".<br>***NOTE:*** *This pin requires an external pull-up resistor.* |
| $\overline{RESET}$ | LVTTL, LVCMOS | I | B10 | **Master Reset Input**<br>Active "Low" signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values.<br>This pin is provided with an internal pull-up. |

### HARDWARE COMMON CONTROL

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| RLOOPS | LVTTL, LVCMOS | I | C10 | **Serial Remote Loopback**<br>The serial remote loopback mode interconnects the receive serial data input to the transmit serial data output. If serial remote loopback is enabled, the 4-bit parallel transmit data input is ignored while the 4-bit parallel receive data output is maintained.<br>"Low" = Disabled<br>"High" = Serial Remote Loopback Mode Enabled<br>***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*<br>This pin is provided with an internal pull-down. |
| RLOOPP | LVTTL, LVCMOS | I | A11 | **Parallel Remote Loopback**<br>The parallel remote loopback mode allows the serial data input stream to pass through the clock and data recovery circuit and looped-back at the parallel interface to the serial output port. The 4-bit parallel transmit data input is ignored while the 4-bit parallel receive data output is maintained.<br>"Low" = Disabled<br>"High" = Parallel Remote Loopback Mode Enabled<br>***NOTE:*** *DLOOP and RLOOPS should be* ***disabled*** *when RLOOPP is enabled. The internal FIFO should also be flushed using FIFO_RST pin or register bit when parallel remote loopback is enabled/disabled.*<br>This pin is provided with an internal pull-down. |
| DLOOP | LVTTL, LVCMOS | I | B6 | **Digital Local Loopback**<br>The digital local loopback mode interconnects the 4-bit parallel transmit data and parallel transmit clock input to the 4-bit parallel receive data and parallel receive clock output respectively while maintaining the transmit serial data output. If digital local loopback is enabled, the receive serial data input is ignored.<br>"Low" = Disabled<br>"High" = Digital Local Loopback Mode Enabled<br>***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*<br>This pin is provided with an internal pull-down. |

### *HARDWARE COMMON CONTROL*

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| LOOPTM_JA | LVTTL, LVCMOS | I | C6 | **Loop Timing Mode With Jitter Attenuation**<br>The LOOPTM_JA pin must be set "High" in order to select the recovered receive clock as the reference source for the de-jitter PLL.<br>"Low" = Disabled<br>"High" = Loop timing with de-jitter PLL Activated<br>This pin is provided with an internal pull-down. |
| LOOPTM_NOJA | LVTTL, LVCMOS | I | P2 | **Loop Timing Mode With No Jitter Attenuation**<br>When the loop timing mode is activated, the external local reference clock input to the CMU is replaced with the 1/16th or 1/32nd of the high-speed recovered receive clock coming from the CDR.<br>"Low" = Disabled<br>"High" = Loop timing Activated<br>This pin is provided with an internal pull-down. |

### *TRANSMITTER SECTION*

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| TXDI0P<br>TXDI0N<br>TXDI1P<br>TXDI1N<br>TXDI2P<br>TXDI2N<br>TXDI3P<br>TXDI3N | LVDS | I | H13<br>J13<br>K14<br>L14<br>K13<br>L13<br>M14<br>N14 | **Transmit Parallel Data Input**<br>The 622.08 Mbps 4-bit parallel transmit data input should be applied to the transmit parallel bus simultaneously to be sampled at the rising edge of the TXPCLKIP/N input. The 4-bit parallel interface is multiplexed into the transmit serial output interface MSB first (TXDI3P/N).<br>***NOTE:*** *The XRT91L80 can accept 666.51 Mbps 4-bit parallel transmit data input for Forward Error Correction (FEC) Applications.* |
| TXPCLKIP<br>TXPCLKIN | LVDS | I | H14<br>J14 | **Transmit Parallel Clock Input**<br>622.08 MHz clock input used to sample the 4-bit parallel transmit data input TXDI[3:0]P/N.<br>***NOTE:*** *The XRT91L80 can accept a 666.51 MHz transmit clock input for Forward Error Correction (FEC) Applications.* |
| TXOP<br>TXON | CMLDIFF | O | K1<br>L1 | **Transmit Serial Data Output**<br>The transmit serial data output stream is generated by multiplexing the 4-bit parallel transmit data input into a 2.488 Gbps serial data output stream. In Forward Error Correction, the transmit serial data output stream is 2.666 Gbps. |
| REFCLKP<br>REFCLKN | LVPECL | I | P6<br>N6 | **Reference Clock Input**<br>This differential clock input reference is used for the transmit clock multiplier unit (CMU) to provide the necessary high-speed clock reference for this device. Pin ALTFREQSEL determines the value used as the reference. See Pin ALTFREQSEL for more details. |
| VCXO_INP<br>VCXO_INN | LVPECL | I | P4<br>N4 | **Voltage Controled Oscillator Input**<br>This differential clock input is used for the transmit PLL jitter attenuation. Pin ALTFREQSEL determines the value used as the reference. See Pin ALTFREQSEL for more details. |

### *TRANSMITTER SECTION*

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| ALTFREQSEL | LVTTL, LVCMOS | I | P1 | **Reference Clock Frequency Select**<br>This pin is used to select the frequency of the REFCLKP/N clock input to the CMU.<br>"Low" = 77.76 MHz (83.31 MHz for FEC)<br>"High" = 155.52 MHz (166.63 MHz for FEC)<br>This pin is provided with an internal pull-up. |
| VCXO_SEL | LVTTL, LVCMOS | I | M6 | **De-Jitter VCXO Select Option**<br>This pin selects either the normal REFCLKP/N or the de-jitter VCXO_INP/N pin as a reference clock to the CMU.<br>"Low" = Normal REFCLKP/N reference clock<br>"High" = De-Jitter VCXO_INP/N reference clock<br>This pin is provided with an internal pull-down. |
| VCXO_LOCK | LVCMOS | O | N8 | **De-Jitter PLL Lock Detect**<br>If the de-jitter PLL lock detect is enabled with pin P3 and the de-jitter VCXO mode is selected by pin M6, this pin will assert "High" when the PLL is locked.<br>"Low" = VCXO Out of Lock<br>"High" = VCXO Locked |
| VCXO_LOCKEN | LVTTL, LVCMOS | I | P3 | **De-Jitter PLL Lock Detect Enable**<br>This pin enables the VCXO_INP/N lock detect circuit and VCXO_LOCK pin N8 to be active.<br>"Low" = VCXO Lock Detect Disabled<br>"High" = VCXO Lock Detect Enabled<br>This pin is provided with an internal pull-down. |
| CPOUT | - | O | P8 | **Charge Pump Output (for external VCXO)**<br>The nominal output of the charge pump current is 250µA |
| LOOPBW | LVTTL, LVCMOS | I | M7 | **CMU Loop Bandwidth Select**<br>This pin is used to select the bandwidth of the clock multiplier unit of the transmit path to a narrow or wide band. Use Wide Band for clean reference signals and Narrow Band for noisy references.<br>"Low" = Wide Band (4x)<br>"High" = Narrow Band (1x)<br>This pin is provided with an internal pull-down. |
| TXPCLKOP<br>TXPCLKON | LVDS | O | P10<br>P11 | **Transmit Parallel Clock Output**<br>This 622.08 MHz clock can be used for the downstream device to generate the TXDI[3:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48/STM-16 transceiver to be in synchronization.<br>***NOTE:*** *The XRT91L80 can output a 666.51 MHz transmit clock output for Forward Error Correction (FEC).* |

### *TRANSMITTER SECTION*

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| TXCLKO16P<br>TXCLKO16N | LVDS | O | N10<br>N11 | **Auxiliary Clock Output (155.52/166.63 MHz)**<br>155.52/166.63 MHz auxiliary clock derived from CMU output. This clock can also be used for the downstream device as a reference for generating the TXDI[3:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48/STM-16 transceiver to be in synchronization. The output of this pin is controlled by TXCLKO16DIS. |
| TXCLKO16DIS | LVTTL, LVCMOS | I | M12 | **Auxiliary Clock Disable**<br>This pin is used to control the activity of the auxiliary clock.<br>"Low" = TXCLKO16P/N Enabled<br>"High" = TXCLKO16P/N Disabled<br>This pin is provided with an internal pull-down. |
| LOCKDET_CMU | LVCMOS | O | N2 | **CMU Lock Detect**<br>This pin is used to monitor the lock condition of the clock multiplier unit.<br>"Low" = CMU Out of Lock<br>"High" = CMU Locked |
| OVERFLOW | LVCMOS | O | M13 | **Transmit FIFO Overflow**<br>This pin is used to monitor the transmit FIFO status.<br>"Low" = Normal Status<br>"High" = Overflow Condition |
| FIFO_RST | LVTTL, LVCMOS | I | N13 | **FIFO Control Reset**<br>FIFO_RST should be held "High" for a minimum of 2 TXPCLKOP/N cycles after powering up and during manual FIFO reset. After the FIFO_RST pin is returned "Low," it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Upon an interrupt indication that the FIFO has an overflow condition, this pin is used to reset or flush out the FIFO.<br>"Low" = Normal Operation<br>"High" = Manual FIFO Reset<br>***NOTE:*** *To automatically reset the FIFO, see FIFO_AUTORST pin.*<br>This pin is provided with an internal pull-down. |
| FIFO_AUTORST | LVTTL, LVCMOS | I | N12 | **Automatic FIFO Overflow Reset**<br>If this pin is set "High", the STS-48/STM-16 transceiver will automatically flush the FIFO upon an overflow condition. Upon power-up, the FIFO should be manually reset by setting FIFO_RST "High" for a minimum of 2 TXPCLKOP/N cycles.<br>"Low" = Manual FIFO reset required for Overflow Conditions<br>"High" = Automatically resets FIFO upon Overflow Detection<br>This pin is provided with an internal pull-down. |

### *RECEIVER SECTION*

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| RXDO0P<br>RXDO0N<br>RXDO1P<br>RXDO1N<br>RXDO2P<br>RXDO2N<br>RXDO3P<br>RXDO3N | LVDS | O | E13<br>F13<br>C14<br>D14<br>C13<br>D13<br>A14<br>B14 | **Receive Parallel Data Output**<br>622Mbps 4-bit parallel receive data output is updated simultaneously on the rising edge of the RXPCLKOP/N output. The 4-bit parallel interface is de-multiplexed from the receive serial data input MSB first (RXDO3P/N).<br>***NOTE:*** *The XRT91L80 can output 666.51 Mbps 4-bit parallel receive data output for Forward Error Correction (FEC) Applications.* |
| RXPCLKOP<br>RXPCLKON | LVDS | O | E14<br>F14 | **Receive Parallel Clock Output**<br>622.08 MHz parallel clock output used to update the 4-bit parallel receive data output RXDO[3:0]P/N at the rising edge of this clock..<br>***NOTE:*** *The XRT91L80 can output a 666.51 MHz receive clock output for Forward Error Correction (FEC).* |
| DISRD | LVTTL<br>LVCMOS | I | C12 | **Parallel Receive Data Output Disable**<br>This pin is used to disable the RXDO[3:0]P/N parallel receive data output bus asynchronously.<br>"Low" = Normal Mode<br>"High" = Forces RXDO[3:0]P/N to a logic state "0"<br>This pin is provided with an internal pull-down. |
| RXIP<br>RXIN | CMLDIFF | I | C1<br>D1 | **Receive Serial Data Input**<br>The receive serial data stream of 2.488 Gbps is applied to these input pins. In Forward Error Correction, the receive serial data stream is 2.666 Gbps. |
| XRES1P<br>XRES1N | - | I | G1<br>F1 | **External LVDS Biasing Resistors**<br>A 402Ω resistor with +/-1% tolerance should be placed across these 2 pins for proper biasing. |
| RXCLKO16P<br>RXCLKO16N | LVDS | O | A6<br>A7 | **Auxiliary Clock Output (155.52/166.63 MHz)**<br>155.52/166.63 MHz auxiliary clock derived from divide-by-16 CDR recovered clock. |
| LOCKDET_CDR | LVCMOS | O | C7 | **CDR Lock Detect**<br>This pin is used to monitor the lock condition of the clock and data recovery unit.<br>"Low" = CDR Out of Lock<br>"High" = CDR Locked |
| SDEXT | LVTTL,<br>LVCMOS | I | B5 | **Signal Detect Input from Optical Module**<br>**Hardware Mode** When inactive, it will immediately declare a Loss of Signal Detect (LOSD) condition and assert LOSDET output pin and control the activity of the RXDO[3:0]P/N parallel data output based on LOSDMUTE pin setting.<br>**Host Mode** In addition to asserting LOSDET output pin, it will update the LOSD condition on the registers and control the activity of the RXDO[3:0]P/N parallel data output based on LOSDMUTE register bit setting.<br>"Active" = Normal Operation<br>"Inactive" = LOSD Condition (SDEXT detects signal absence)<br>This pin is provided with an internal pull-down. |

### *RECEIVER SECTION*

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| POLARITY | LVTTL, LVCMOS | I | C4 | **Polarity for SDEXT Input**<br>Controls the Signal Detect polarity convention of SDEXT.<br>"Low" = SDEXT is active "Low."<br>"High" = SDEXT is active "High."<br>This pin is provided with an internal pull-down. |
| LOSDET | LVCMOS | O | C5 | **LOS Detect Condition**<br>Flags LOSD condition based on SDEXT signal coming from the optical module.<br>"Low" = No Alarm<br>"High" = A LOS condition is present |
| LOSDMUTE | LVTTL, LVCMOS | I | A3 | **Parallel Receive Data Output Mute Upon LOSD**<br>If this pin is asserted "High", the receive data output will automatically be forced to a logic state of "0" when an LOSD condition occurs.<br>"Low" = Disabled<br>"High" = Mute RXDO[3:0]P/N Data Upon LOSD Condition<br>This pin is provided with an internal pull-down. |

### *POWER AND GROUND*

| NAME | TYPE | PIN | DESCRIPTION |
|---|---|---|---|
| VDD3.3 | PWR | A8, D9, D10, D11, E11, P13, P14 | **CMOS Digital 3.3V I/O Power Supply**<br>VDD3.3 should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDD3.3 power supply pins should have bypass capacitors to the nearest ground. |
| AVDD3.3_RX | PWR | D3, E3 | **Analog 3.3V I/O Receiver Power Supply**<br>AVDD3.3_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_RX power supply pins should have bypass capacitors to the nearest ground. |
| AVDD3.3_TX | PWR | P5, P9 | **Analog 3.3V I/O Transmitter Power Supply**<br>AVDD3.3_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_TX power supply pins should have bypass capacitors to the nearest ground. |
| VDD1.8 | PWR | A13, B7, B13, D12, E12, K11, L9, L10, M9, M10, M11 | **CMOS Digital 1.8V Core Power Supply**<br>VDD1.8 should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDD1.8 power supply pins should have bypass capacitors to the nearest ground. |
| AVDD1.8_RX | PWR | D4, D5, D6, D8, F3, G3 | **Analog 1.8V Core Receiver Power Supply**<br>AVDD1.8_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD1.8_RX power supply pins should have bypass capacitors to the nearest ground. |

### POWER AND GROUND

| NAME | TYPE | PIN | DESCRIPTION |
|---|---|---|---|
| AVDD1.8_TX | PWR | J1, J4, L6, L7, L8, M3, N9, M2 | **Analog 1.8V Core Transmitter Power Supply**<br>AVDD1.8_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD1.8_TX power supply pins should have bypass capacitors to the nearest ground. |
| DGND | GND | A5, A12, B3, B8, B12, F11, F12, G11, G12, G13, G14, H11, H12, J11, J12, K12, L3, L11, L12, P12 | **Digital Ground for 3.3V I/O and 1.8V Core Digital Power Supplies**<br>It is recommended that all ground pins of this device be tied together. |
| AGND_RX | GND | A1, B1, B2, C2, C3, D2, D7, E1, E2, E4, F2, F4, G2, G4, H1, H2, H3, H4 | **Receiver Analog Ground for 3.3V I/O and 1.8V Core Analog Power Supplies**<br>It is recommended that all ground pins of this device be tied together. |
| AGND_TX | GND | J2, J3, K2, K3, K4, L2, L4, L5, M1, M4, M5, N5, N7, P7 | **Transmitter Analog Ground for 3.3V I/O and 1.8V Core Analog Power Supplies**<br>It is recommended that all ground pins of this device be tied together. |
| TGND | GND | E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10 | **Thermal Ground**<br>It is recommended that all ground pins of this device be tied together. |

### NO CONNECTS

| NAME | LEVEL | TYPE | PIN | DESCRIPTION |
|---|---|---|---|---|
| NC | | NC | A4<br>B4 | **No Connect**<br>This pin can be left floating or tied to ground. |

***JTAG***

| SIGNAL NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| TCK | N3 | I | **Test clock:** Boundary Scan Clock Input. |
| TMS | N1 | I | **Test Mode Select:** Boundary Scan Mode Select Input.<br>JTAG is disabled by default.<br>***Note****: This input pin should be pulled "Low" for JTAG operation*<br>This pin is provided with an internal pull-up. |
| TDI | M8 | I | **Test Data In:** Boundary Scan Test Data Input<br>This pin is provided with an internal pull-up. |
| TDO | B11 | O | **Test Data Out:** Boundary Scan Test Data Output |
| TRST | A2 | I | **JTAG Test Reset Input**<br>***Note****: This input pin should be pulled "Low" to reset JTAG*<br>This pin is provided with an internal pull-up. |

## 1.0 FUNCTIONAL DESCRIPTION

The XRT91L80 transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The transceiver converts 4-bit parallel data at 622.08/666.51 Mbps to a serial CML bit stream at 2.488/2.666 Gbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), and receive clock and data recovery (CDR) unit. The transceiver is divided into transmit and receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

### 1.1 Hardware Mode vs. Host Mode

Functionality of the STS-48/STM-16 transceiver can be configured by using either Host mode or Hardware mode. If Hardware mode is selected by pulling HOST/$\overline{HW}$ "Low" or leaving this pin unconnected, the functionality is controlled by the hardware pins described in the Hardware Pin Descriptions. However, if Host mode is selected by pulling HOST/$\overline{HW}$ "High", the functionality is controlled by programming internal R/W registers using the Serial Microprocessor interface. Whether using Host or Hardware mode, the functionality remains the same. Therefore, the following sections describe the functionality rather than how each function is controlled. The Hardware Pin Descriptions and the Register Bit Descriptions concentrate on configuring the device.

### 1.2 Clock Input Reference

The XRT91L80 can accept either a 77.76/83.3 MHz or 155.52/166.63 MHz clock input at REFCLKP/N as its internal timing reference for generating higher speed clocks. The reference clock can be provided with one of two frequencies chosen by ALTFREQSEL. The reference frequency options for the XRT91L80 are listed in Table 1.

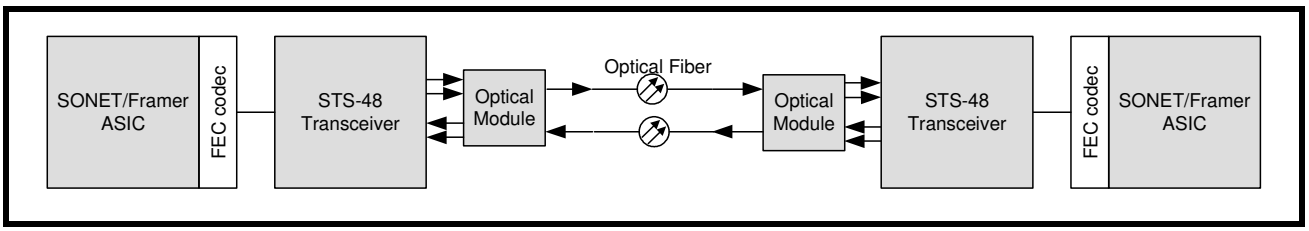
**TABLE 1: REFERENCE FREQUENCY OPTIONS (NON-FEC AND FEC MODE)**

| ALTFREQSEL | REFERENCE CLOCK FREQUENCY | TRANSMIT/RECEIVE DATA RATE | OPERATING MODE |
|---|---|---|---|
| 0 | 77.76/83.3 MHz | 2.488/2.666 Gbps | STS-48/STM-16 |
| 1 | 155.52/166.63 MHz | 2.488/2.666 Gbps | STS-48/STM-16 |

### 1.3 Forward Error Correction (FEC)

Forward Error Correction is used to control errors along a one-way path of communication. FEC sends extra information along with data which can be used by a receiver to check and correct the data without requesting re-transmission of the original information. It does so by introducing a known structure into a data sequence prior to transmission. The most common methods are to replace a 14-bit data packet with a 15-bit codeword structure, or to replace a 17-bit data packet with an 18-bit codeword structure. To maintain original bandwidth, a higher speed clock reference, derived by the ratio of 15/14 or 18/17 referenced to 77.76MHz or 155.52MHz is applied to the STS-48/STM-16 transceiver using an external crystal. The XRT91L80 supports FEC by accepting a clock input reference frequency of 83.31 MHz or 166.63 MHz. This allows the transmit 4-bit parallel data input to be applied to the STS-48/STM-16 transceiver at 666.51 Mbps which is converted to a 2.666 Gbps serial output stream to an optical module. A simplified block diagram of FEC is shown in Figure 3.

**FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF FORWARD ERROR CORRECTION**



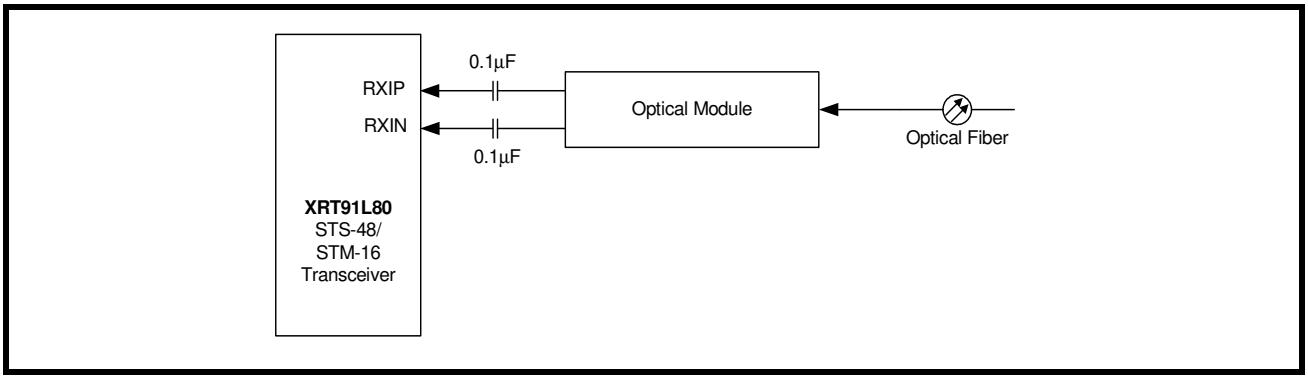
## 2.0 RECEIVE SECTION

The receive section of XRT91L80 includes the differential inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter (SIPO). The receiver accepts the high speed Non-Return to Zero (NRZ) serial data at 2.488/2.666 Gbps through the differential input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into 4-bit-wide 622.08/666.51 Mbps parallel data and presented to the RXD[3:0]P/N LVDS parallel interface. A divide-by-4 version of the high-speed recovered clock, RXPCLKOP/N, is used to synchronize the transfer of the 4-bit RXDO[3:0]P/N data with the receive portion of the upstream device. Upon initialization or loss of signal or loss of lock the 77.76/155.52 MHz (83.31/166.63 MHz) external local reference clock is used to start-up the clock recovery phase-locked loop for proper operation. A special loop-back feature can be configured when parallel remote loopback (RLOOPP) is used in conjunction with de-jittered loop-time mode that allows the re-transmitted data to comply with ITU and Bellcore jitter generation specifications.

### 2.1 Receive Serial Input

The receive serial CML inputs are applied to RXIP/N. The receive serial inputs can be AC or DC coupled to an optical module or an electrical interface. A simplified AC coupled block diagram is shown in Figure 4.

**FIGURE 4. RECEIVE SERIAL INPUT INTERFACE BLOCK**




***NOTE:*** *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

The 2.488/2.666 Gbps high-speed differential CML RXIP/N input swing characteristics is shown in Table 2.

**TABLE 2: DIFFERENTIAL CML INPUT SWING PARAMETERS**

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $\Delta V_{INDIFF}$ | Differential Input Voltage Swing | 200 | | 1000 | mV |
| $\Delta V_{INSE}$ | Single-Ended Input Voltage Swing | 100 | | 500 | mV |
| $\Delta V_{INBIAS}$ | Input Bias Range (AC Coupled) | 1.0 | | 1.4 | V |
| $R_{DIFF}$ | Differential Input Resistance | 75 | | 125 | Ω |

## 2.2 Receive Clock and Data Recovery

The clock and data recovery unit accepts the high speed NRZ serial data from the differential CML receiver and generates a clock that is the same frequency as the incoming data. The clock recovery utilizes the REFCLKP/N to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the local reference clock within ±500 ppm. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock. When this condition occurs the PLL will declare Loss of Lock and the LOCKDET_CDR signal will be pulled "Low." Whenever a Loss of Lock/Loss of Signal Detection (LOSD) event occurs, the CDR will continue to supply a receive clock (based on the local reference clock) to the upstream framer device. A Loss of Lock condition will also be declared when the external SDEXT becomes inactive. When the SDEXT is de-asserted by the optical module and LOSDMUTE is enabled, receive parallel data output will be forced to a logic zero state for the entire duration that a LOSD condition is detected. This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. When SDEXT becomes active and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source, the clock recovery PLL will switch and lock back onto the incoming receive data stream and the lock detect output (LOCKDET_CDR) will go active. Table 3 specifies the Clock and Data Recovery Unit performance characteristics.

**TABLE 3: CLOCK AND DATA RECOVERY UNIT PERFORMANCE**

| NAME | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $REF_{DUTY}$ | Reference clock duty cycle | 45 | | 55 | % |
| $REF_{TOL}$ | Reference clock frequency tolerance[1] | -20 | | +20 | ppm |
| $OCLK_{JIT}$ | Clock output jitter generation with 77.76 MHz reference clock | | 3.5 | 5.0 | $mUI_{rms}$ |
| $OCLK_{JIT}$ | Clock output jitter generation with 155.52 MHz reference clock | | 3.7 | 5.0 | $mUI_{rms}$ |
| $TOL_{JIT}$ | Input jitter tolerance with 1 MHz < f < 20 MHz PRBS pattern | 0..35 | 0.5 | | UI |
| $OCLK_{FREQ}$ | Frequency output | 2.488 | | 2.667 | GHz |
| $OCLK_{DUTY}$ | Clock output duty cycle | 45 | | 55 | % |

Jitter specification is defined using a 12kHz to 20MHz appropriate SONET/SDH filter.

[1]Required to meet SONET output frequency stability requirements.

## 2.3 External Signal Detection

XRT91L80 supports external Signal Detection (SDEXT). The external Signal Detect function is supported by the SDEXT input. This input is coming from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices, the polarity of this signal can be either active "Low" or active "High." The SDEXT and POLARITY inputs are Exclusive OR’ed to generate the external LOSDET signal, internal Loss of Signal Detect (LOSD) declaration and Mute upon LOSD control signal. Whenever an external SD is absent, the XRT91L80 will automatically output a high level signal on the LOSDET output pin as well as update the control registers whenever the host mode serial microprocessor interface feature is active. If LOSDMUTE is enabled, it will force the receive parallel data output to a logic state "0" for the entire duration that a LOSD condition is declared. This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. Table 4 specifies SDEXT declaration polarity settings.

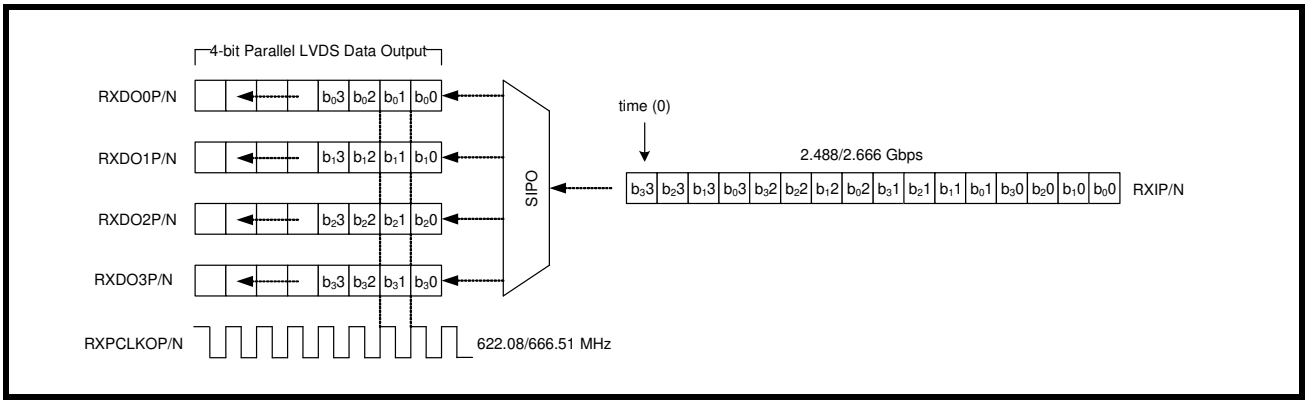
**TABLE 4: LOSD DECLARATION POLARITY SETTING**

| SDEXT | POLARITY | LOSDMUTE | INTERNAL SIGNAL DETECT | LOSDET OUTPUT | RXDO[3:0]P/N | CDR PLL REFERENCE LOCK |
|---|---|---|---|---|---|---|
| **0** | **0** | **1** | Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module. | Low | Normal Operation | Hi-Spd Received Data |
| **0** | **1** | **1** | Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module. | High **LOSD declared** | Muted | Local Reference Clock |
| **1** | **0** | **1** | Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module. | High **LOSD declared** | Muted | Local Reference Clock |
| **1** | **1** | **1** | Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module. | Low | Normal Operation | Hi-Spd Received Data |

## 2.4 Receive Serial Input to Parallel Output (SIPO)

The SIPO is used to convert the 2.488/2.666 Gbps serial data input to 622.08/666.51 Mbps parallel data output which can interface to a SONET Framer/ASIC. The SIPO bit de-interleaves the serial data input into a 4-bit parallel output to RXDO[3:0]P/N. A simplified block diagram is shown in Figure 5.

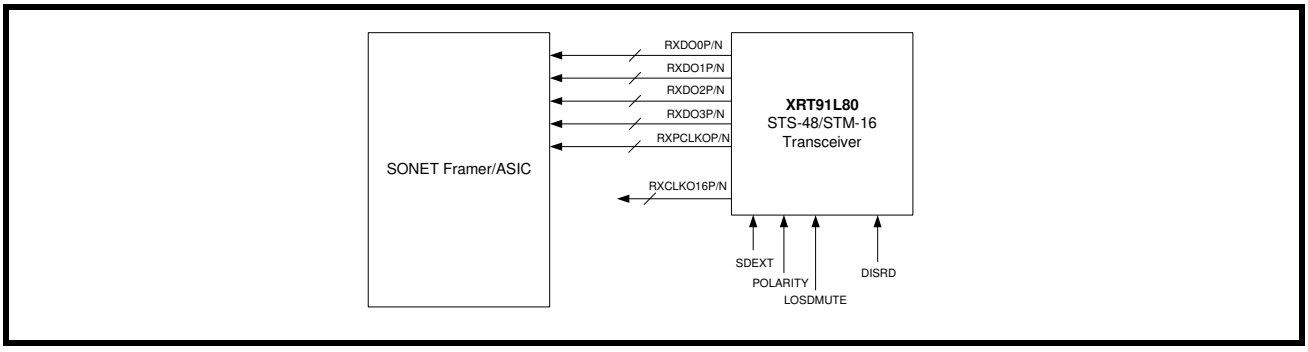
**FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF SIPO**




## 2.5 Receive Parallel Output Interface

The 4-bit LVDS 622.08/666.51 Mbps parallel data output of the receive path is used to interface to a SONET Framer/ASIC synchronized to the recovered clock. A simplified block diagram is shown in Figure 6.

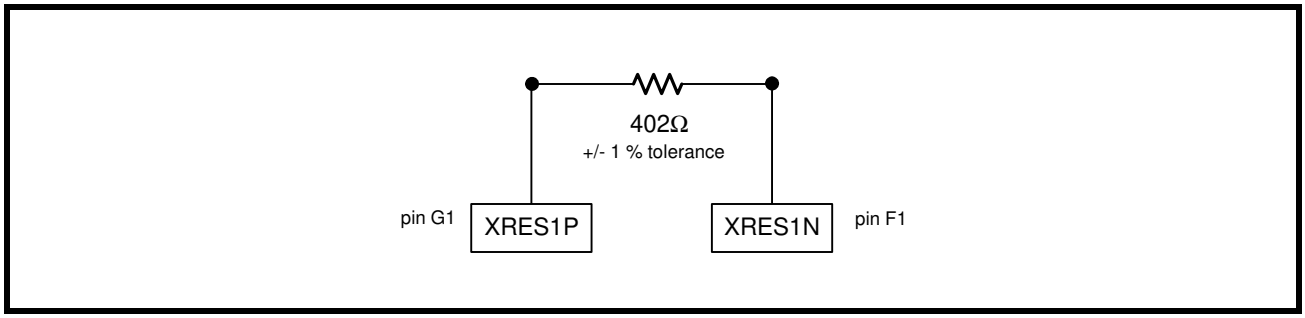
**FIGURE 6. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK**



### 2.6 Receive Parallel Interface LVDS Operation

When operating the 4-bit Differential bus in LVDS mode, a 402Ω external resistor is needed across XRES1P and XRES1N to properly bias the RXDO[3:0]P/N and RXPCLKOP/N pins. Figure 7 shows the proper biasing resistor installed.

**FIGURE 7. LVDS EXTERNAL BIASING RESISTORS**




### 2.7 Parallel Receive Data Output Mute Upon LOSD

The parallel receiver data outputs can be automatically forced "Low" during an LOSD condition to prevent data chattering. However, the user must select the proper SDEXT polarity for the optical module used. By asserting LOSDMUTE "High", the parallel receiver data outputs will be forced "Low" any time an LOSD condition occurs.

### 2.8 Parallel Receive Data Output Disable

Unlike LOSDMUTE, DISRD is used to asynchronously force the parallel receiver data outputs to zero, regardless of the data input stream. By asserting DISRD "High", the parallel receiver data outputs will immediately mute.

### 2.9 Receive Parallel Data Output Timing

The receive parallel data output from the STS-48/STM-16 receiver will adhere to the setup and hold times shown in Figure 8 and Table 5.

**FIGURE 8. RECEIVE PARALLEL OUTPUT TIMING**

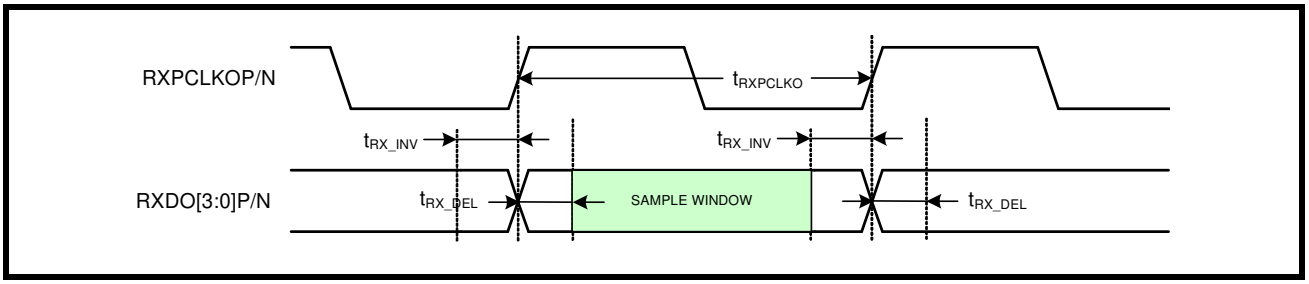



**TABLE 5: RECEIVE PARALLEL DATA AND CLOCK OUTPUT TIMING SPECIFICATIONS**

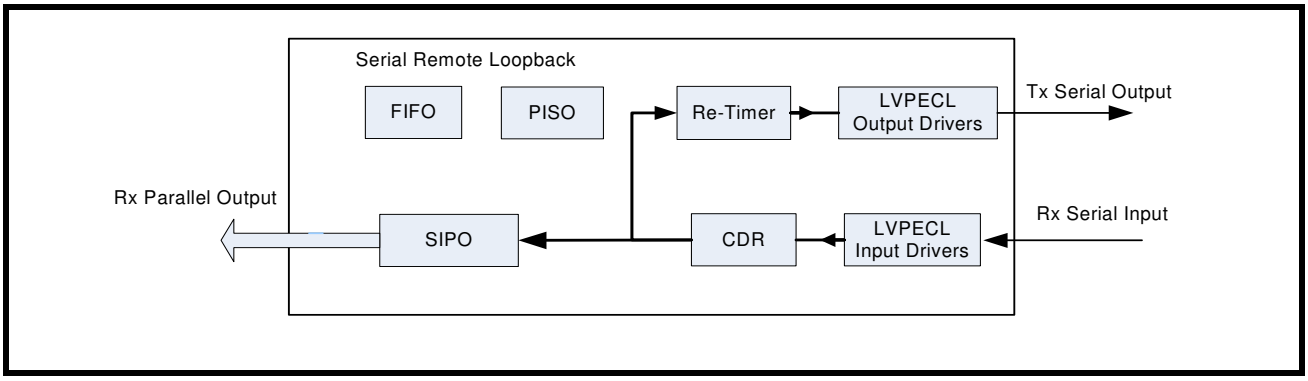
| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{RXPCLKO}$ | Receive parallel clock output period (622.08 MHz non-FEC rate) | | 1608 | | ps |
| $t_{RXPCLKO}$ | Receive parallel clock output period (666.51 MHz FEC rate) | | 1500 | | ps |
| $t_{RX\_INV}$ | RXPCLKOP/N "High" to data invalid window | | 50 | 300 | ps |
| $t_{RX\_DEL}$ | RXPCLKOP/N "High" to data delay | | 50 | 300 | ps |
| $RX_{DUTY}$ | RXPCLKOP/N Duty Cycle | 45 | 50 | 55 | % |

## 4.0 DIAGNOSTIC FEATURES

### 4.1 Serial Remote Loopback

The serial remote loopback function is activated by setting RLOOPS "High". When serial remote loopback is activated, the high-speed serial receive data from RXIP/N is presented at the high-speed transmit output TXOP/N, and the high-speed recovered clock is selected and presented to the high-speed transmit clock input of the Retimer. During serial remote loopback, the high-speed receive data (RXIP/N) is also converted to parallel data and presented at the low-speed receive parallel interface RXDO[3:0]P/N. The recovered receive clock is also divided by 4 and presented at the low-speed clock output RXPCLKOP/N to synchronize the transfer of the 4-bit received parallel data. A simplified block diagram of serial remote loopback is shown in Figure 16.

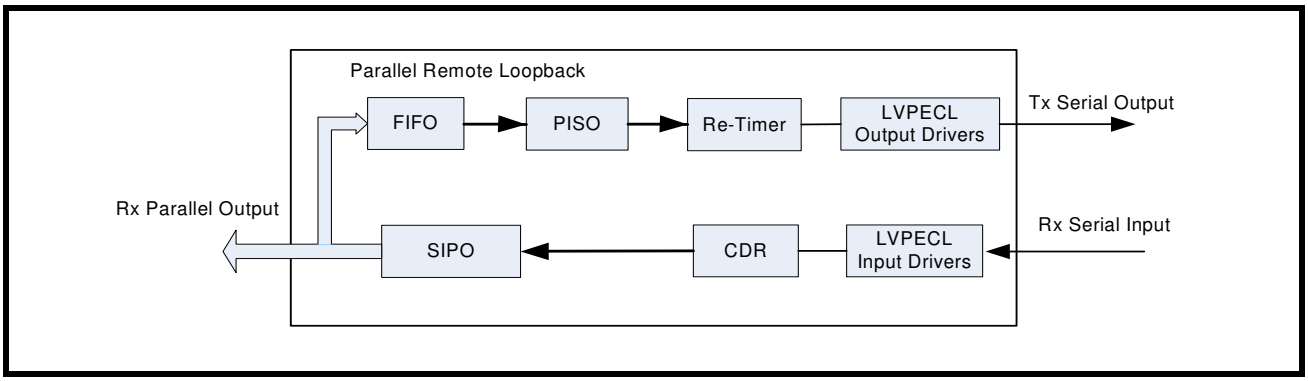
**FIGURE 16. SERIAL REMOTE LOOPBACK**




### 4.2 Parallel Remote Loopback

RLOOPP controls a more comprehensive version of remote loop-back that can also be used in conjunction with the de-jitter PLL that is phase locked to the recovered receive clock. In this mode, the received signal is processed by the CDR, and is sent through the serial to parallel converter. At this point, the 4-bit parallel data and clock are looped back to the transmit FIFO. Concurrently, if receive clock jitter attenuation is also employed, the received clock is divided down in frequency and presented to the input of the integrated phase/ frequency detector and is compared to the frequency of a VCXO that is connected to the VCXO_INP/N inputs. With the LOOPTM_JA configured to use the recovered receive clock as the reference and VCXO_SEL asserted, the VCXO is phase locked to the recovered receive clock. The de-jittered clock is then used to retime the transmitter, resulting in the re-transmission of the de-jittered received data out of TXOP/N. A FIFO reset using FIFO_RST should follow immediately after enabling/disabling parallel remote loopback. A simplified block diagram of parallel remote loopback is shown in Figure 17.

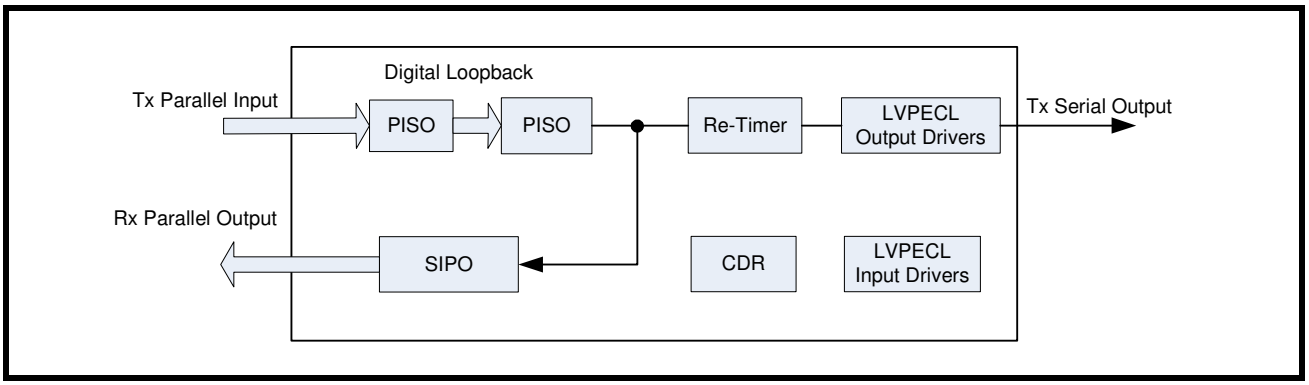
**FIGURE 17. PARALLEL REMOTE LOOPBACK**



### 4.3 Digital Local Loopback

The digital local loopback is activated when the DLOOP signal is set "High." When digital local loopback is activated, the high-speed data from the output of the parallel to serial converter is looped back and presented to the high-speed input of the receiver serial to parallel converter. The CMU output is also looped back to the receive section and is used to synchronize the transfer of the data through the receiver. In Digital loopback mode, the transmit data from the transmit parallel interface TXDI[3:0]P/N is serialized and presented to the high-speed transmit output TXOP/N using the high-speed 2.488/2.666 GHz transmit clock which is generated from the clock multiplier unit and presented to the input of the Retimer and SIPO. A simplified block diagram of digital loopback is shown in Figure 18.

**FIGURE 18. DIGITAL LOOPBACK**



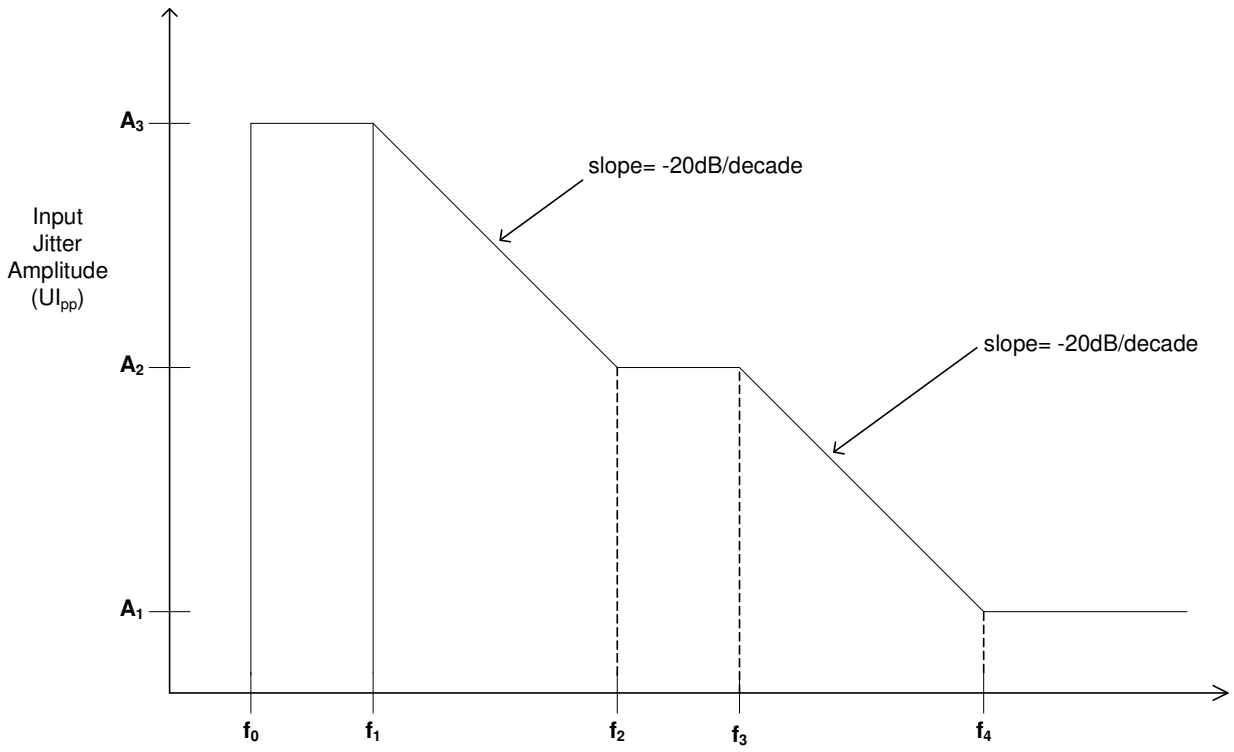
### 4.4 SONET Jitter Requirements

SONET equipment jitter requirements are specified for the following three types of jitter. The definitions of each of these types of jitter are given below. SONET equipment jitter requirements are specified for the following three types of jitter.

#### 4.4.1 Jitter Tolerance:

Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input OC-N equipment interface that causes an equivalent 1dB optical power penalty. OC-1/STS-1, OC-3/STS-3, OC-12/ STS-12 and OC-48/STS-48 category II SONET interfaces should tolerate, the input jitter applied according to the mask of Figure 19, with the corresponding parameters specified in the figure.

**FIGURE 19. JITTER TOLERANCE MASK**




| OC-N/STS-N LEVEL | F0 (HZ) | F1 (HZ) | F2 (HZ) | F3 (HZ) | F4 (HZ) | A1 (UIPP) | A2 (UIPP) | A3 (UIPP) |
|---|---|---|---|---|---|---|---|---|
| 1 | 10 | 30 | 300 | 2K | 20K | 0.15 | 1.5 | 15 |
| 3 | 10 | 30 | 300 | 6.5K | 65K | 0.15 | 1.5 | 15 |
| 12 | 10 | 30 | 300 | 25K | 250K | 0.15 | 1.5 | 15 |
| 48 | 10 | 600 | 6000 | 100K | 1000K | 0.15 | 1.5 | 15 |

FIGURE 20. 91L80 MEASURED JITTER TOLERANCE WITH EXTERNAL JITTER ATTENUATION ENABLED IN LOOPTIMING AT 2.488 GBPS IN STS-48.

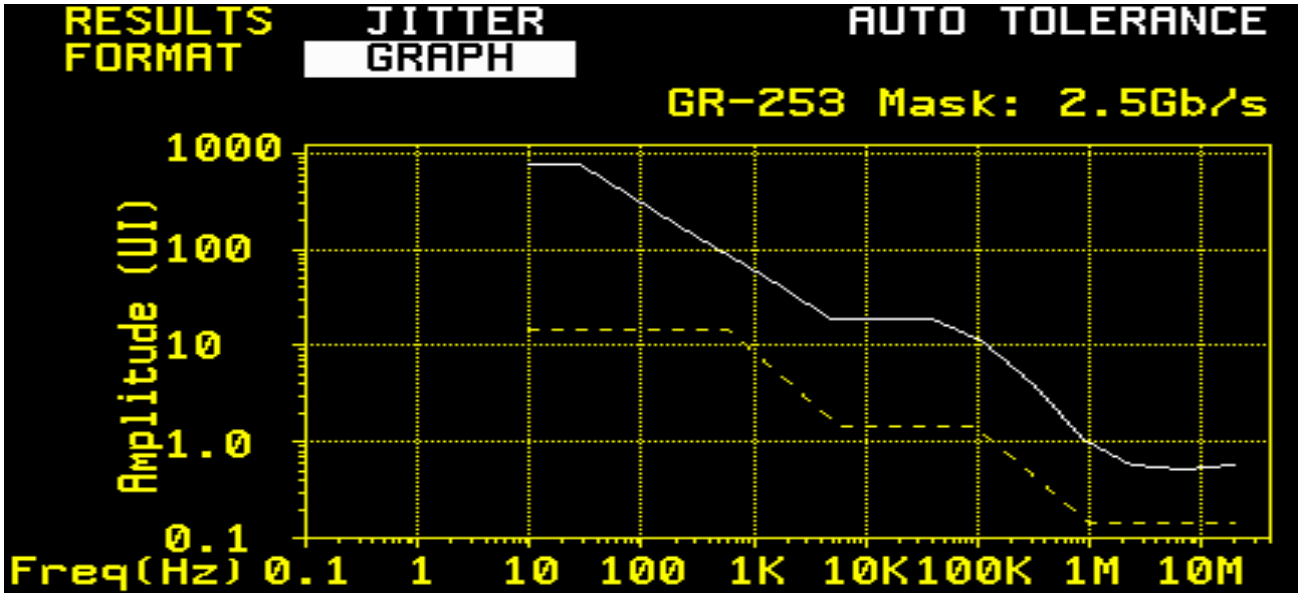
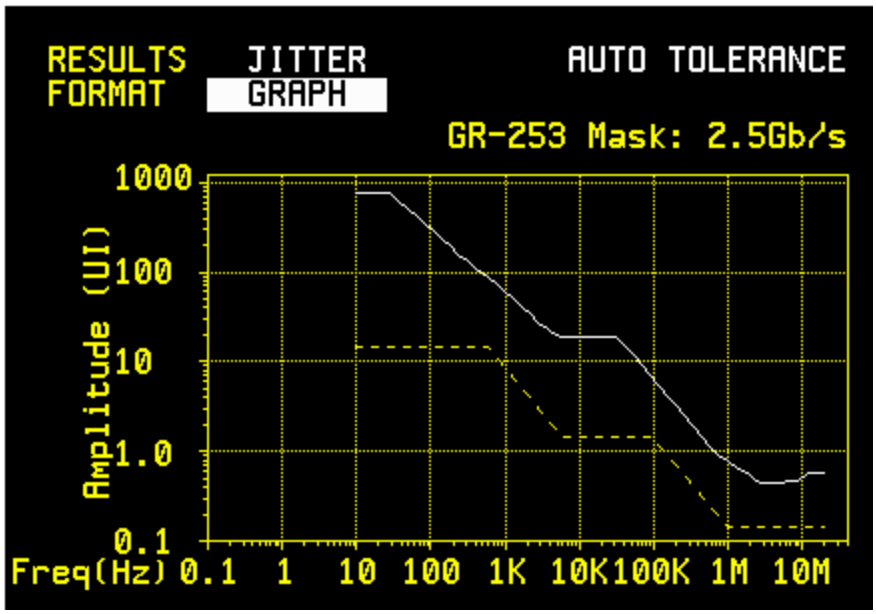



FIGURE 21. 91L80 MEASURED JITTER TOLERANCE WITHOUT JITTER ATTENUATION IN REMOTE SERIAL LOOP BACK




### 4.4.2 Jitter Transfer

Jitter transfer is defined as the ratio of the jitter on the output of STS-N to the jitter applied on the input of STS-N versus frequency. Jitter transfer is important in applications where the system is utilized in the loop-timed mode, where the recovered clock is used as the source of the transmit clock.

FIGURE 22. 91L80 MEASURED JITTER TRANSFER WITH EXTERNAL JITTER ATTENUATION ENABLED IN LOOPTIMING AT 2.488 GBPS IN STS-48.

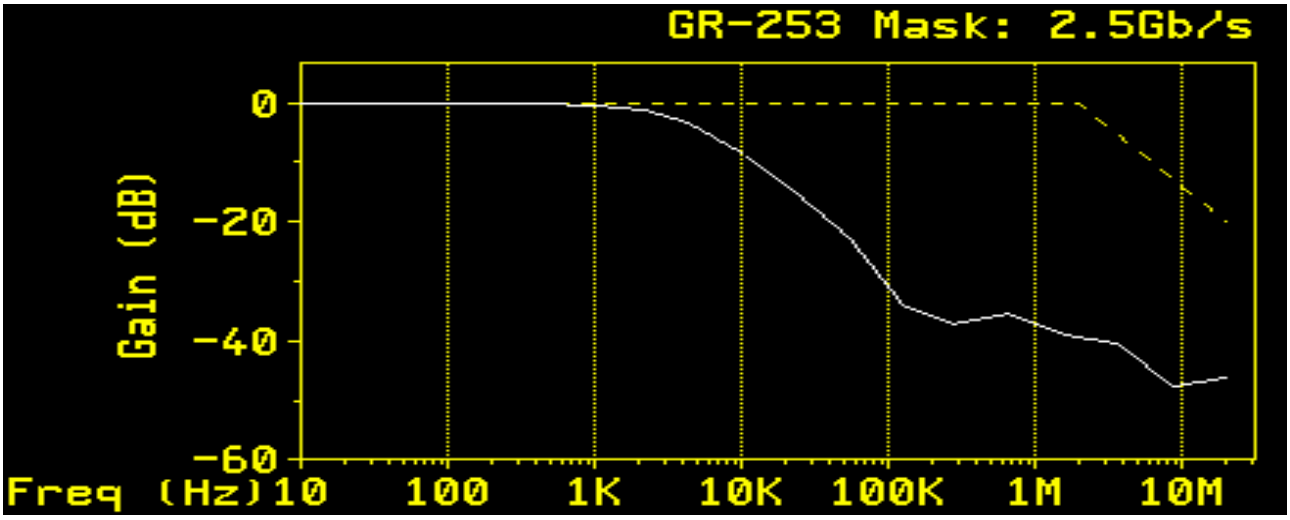



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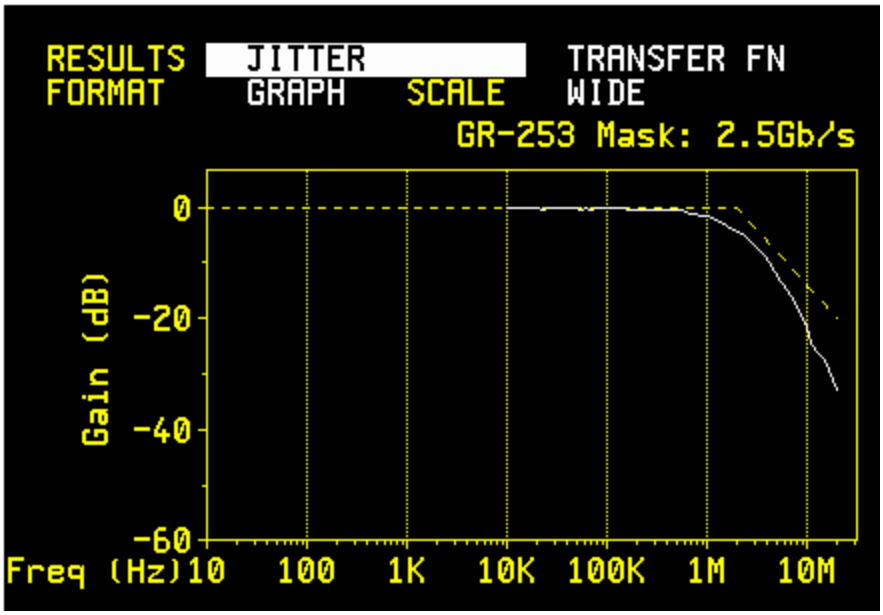
FIGURE 23. MEASURED JITTER TRANSFER WITHOUT JITTER ATTENUATION IN REMOTE SERIAL LOOP BACK



### 4.4.3 Jitter Generation

Jitter generation is defined as the amount of jitter at the STS-N output in the absence of applied input jitter. The Bellcore and ITU requirement for this type jitter is 0.01UI rms measured with a specific band-pass filter.

**FIGURE 24. 91L80 MEASURED ELECTRICAL PHASE NOISE TRANSMIT JITTER GENERATION AT 2.488 GBPS**

Wide-band filter used in this test case.

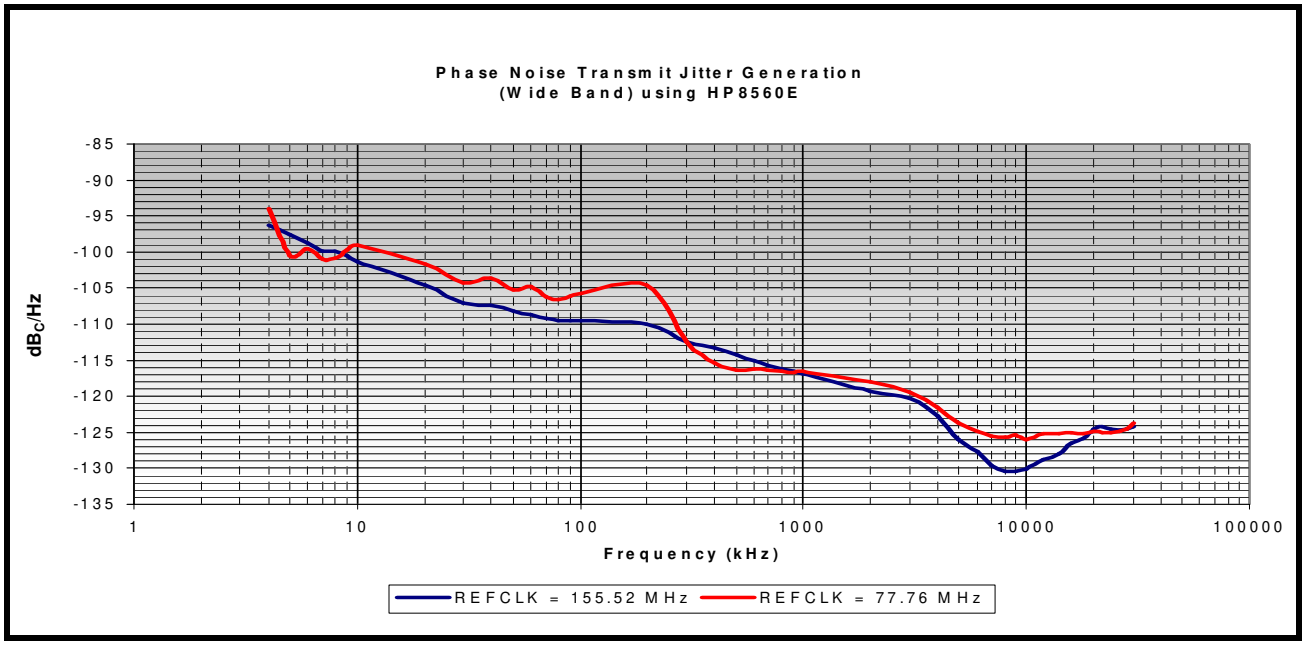
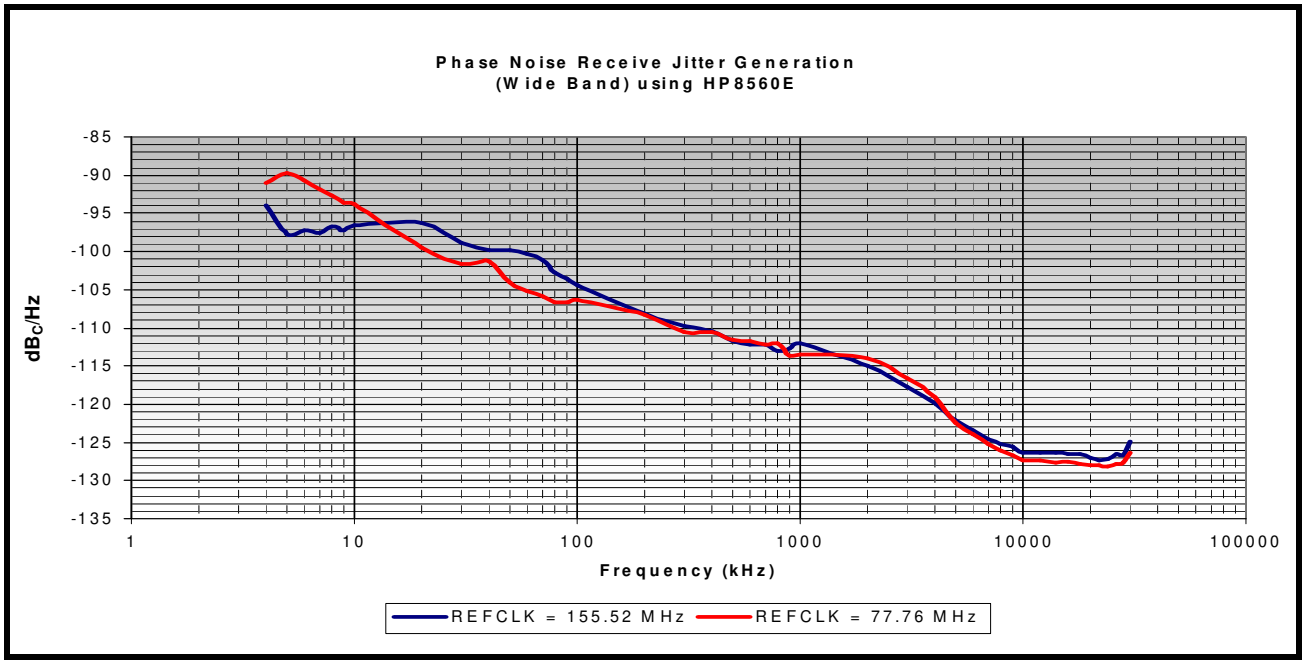



**FIGURE 25. 91L80 MEASURED ELECTRICAL PHASE NOISE RECEIVE JITTER GENERATION AT 2.488 GBPS**

Wide-band filter used in this test case.




For more information on these specifications refer to Bellcore TR-NWT-000253 sections 5.6.2-5 and GR-253-CORE section 5.6.