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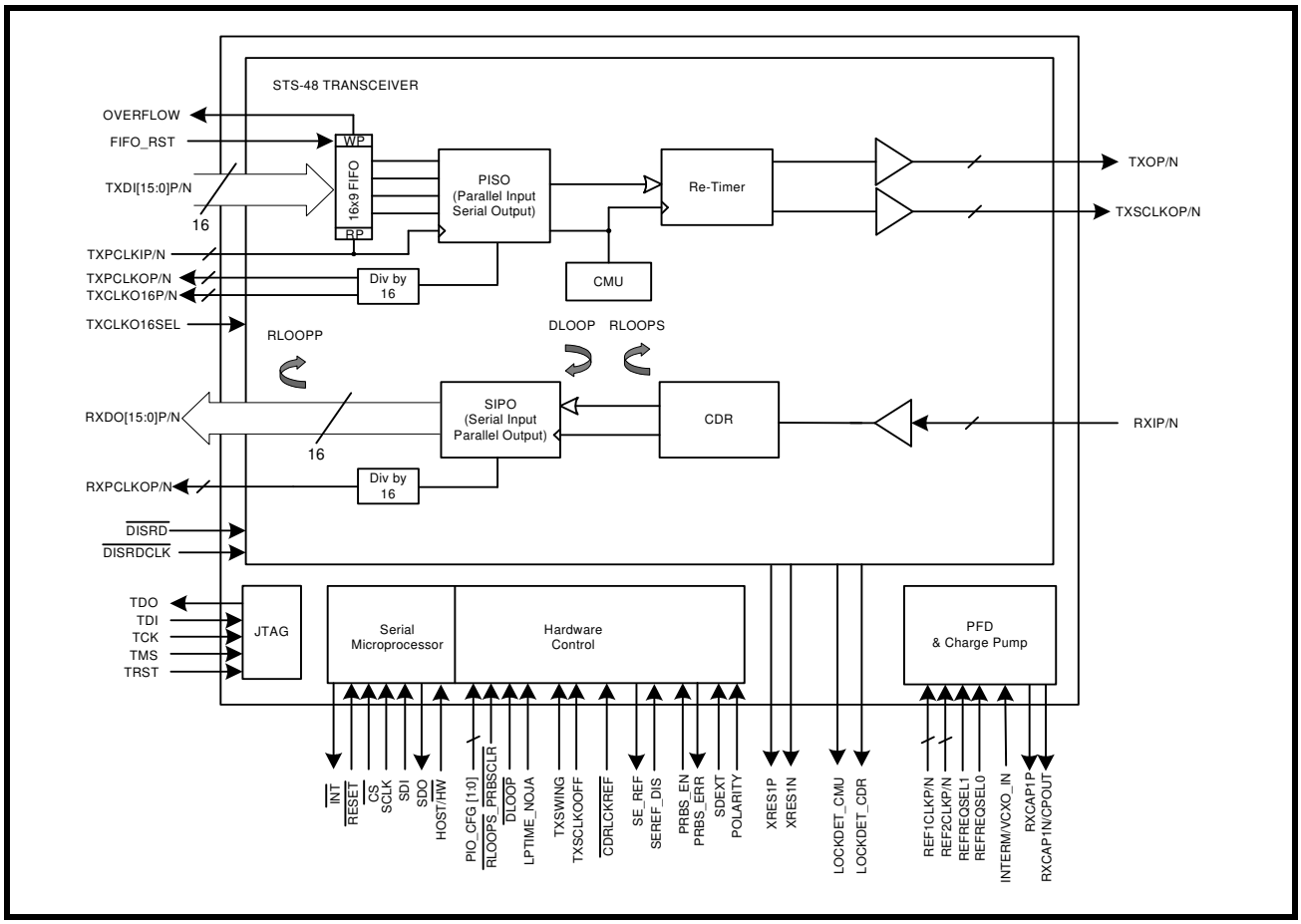
GENERAL DESCRIPTION

The XRT91L82 is a fully integrated SONET/SDH transceiver for OC-48/STM16 applications supporting the use of Forward Error Correction (FEC) capability. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from slower external clock references. It also provides Clock and Data Recovery (CDR) functions by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The chip provides serial-to-parallel and parallel-to-serial converters and 16-bit Differential LVDS/LVPECL, or Single-Ended LVPECL system interfaces in both receive and transmit directions. The transmit section includes a 16x9 Elastic Buffer (FIFO) to absorb any phase differences between the transmitter clock input and the internally generated transmitter reference clock. In the event of an overflow, an internal FIFO control circuit outputs an OVERFLOW indication. The FIFO under the control of the FIFO_AUTORST register bit can automatically recover from an overflow condition. The operation of the device can be monitored by checking the status of the LOCKDET_CMU and LOCKDET_CDR output signals. An on-chip phase/frequency detector and charge-pump offers the ability to form a de-jittering PLL with an external VCXO that can be used in loop timing mode to clean up the recovered clock in the receive section.

APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

FIGURE 1. BLOCK DIAGRAM OF XRT91L82



FEATURES

- 2.488 / 2.666 Gbps Transceiver
- Targeted for SONET OC-48/SDH STM-16 Applications
- Selectable full duplex operation between standard rate of 2.488 Gbps or Forward Error Correction rate of 2.666 Gbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, and clock data recovery (CDR) functions
- 16-bit Differential LVDS/LVPECL, or Single-Ended LVPECL signaling data paths running at 155.52/166.63 Mbps using internal input termination for reduced passive components on board
- Non-FEC and FEC rate REF1CLKP/N and REF2CLKP/N dual reference input ports
- Supports 155.52/166.63MHz or 77.76/83.31MHz transmit and receive external reference input ports
- Optional VCXO input port support multiple de-jittering modes in Host mode
- On-chip phase detector and charge pump for external VCXO based de-jittering PLL
- Internal FIFO decouples transmit parallel clock input and transmit parallel clock output
- Provides Local, Remote Serial and Remote Parallel Loopback modes as well as Loop Timing mode
- Diagnostics features include various lock detect functions and transmit CMU and receive CDR Lock Detect
- Host mode serial microprocessor interface simplifies monitor and control
- Meets Telcordia, ANSI and ITU-T jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, GR-253 CORE, GR-253-ILR- SONET Jitter specifications.
- Operates at 1.8V CMOS and CML Power with 3.3V I/O
- 500mW Typical Power Dissipation using LVDS Interface
- Package: 15 x 15 mm 196-pin STBGA
- IEEE 1149.1 Compatable JTAG port

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT91L82IB	196 STBGA	-40℃ to +85℃

FIGURE 2. 196 BGA PINOUT OF THE XRT91L82 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	GND	RXIP	RXIN	VDD_CML	TXON	TXOP	VDD_CML	TXSCLKON	TXSCLKOP	VDD_CML	REF2CLKP	VDD_CML	REF1CLKP	GND
B	GND	GND	VDD_CML	GND	VDD_CML	GND	VDD_CML	GND	VDD_CML	GND	REF2CLKN	GND	REF1CLKN	GND
C	AVDD_RX	SDEXT	SEREFDIS	TXCLKO16SEL	LOCKDET_CDR	LOCKDET_CMU	TCK	TDI	TXSCLKOOFF / $\overline{CS}$	LOOPTM_NOJA / SDI	VDD_CML	$\overline{CDRLCKREF}$	VDD_CML	AVDD_TX
D	GND	AVDD_RX	PIO_CFG1	$\overline{DISRD}$ /PRBS_LOCK	FIFO_RST	OVERFLOW	TDO	TMS	PRBS_EN	TXSWING / $\overline{INT}$	DISRDCLK (I^2C - SDA)	REFREQSEL1 / SCLK	AVDD_TX	GND
E	RXCAP1P	GND	PIO_CFG0	INTERM / VCXO_IN	$\overline{RESET}$	VDD_CMOS	GND	VDD_CMOS	PRBS_ERR / SDO	POLARITY	$\overline{DLOOP}$ (I^2C - SCL)	REFREQSEL0	GND	XRES1P
F	RXCAP1N / CP_OUT	GND	VDD_CMOS	GND	VDD_CMOS	GND	VDD_CMOS	GND	VDD_CMOS	GND	$\overline{RLOOPS}$ - PRBSCLR	TXDI14P	GND	XRES1N
G	GND	AVDD_RX	VDD_IO	RXDO0N	RXDO0P	GND	TXDI15N	TXDI15P	VDD_IO	TXDI13N	TXDI13P	TXDI14N	AVDD_TX	GND
H	AVDD_RX	GND	RXDO1N	RXDO1P	GND	RXDO2N	RXDO2P	RXDO3P	TXDI11P	GND	TXDI12N	TXDI12P	GND	AVDD_TX
J	VDD_IO	RXDO4N	RXDO4P	VDD_CMOS	RXDO5N	RXDO5P	VDD_CMOS	RXDO3N	TXDI11N	TXDI9P	VDD_IO	TXDI10N	TXDI10P	TXDI8P
K	RXDO6N	RXDO6P	VDD_IO	RXDO7N	RXDO7P	VDD_IO	RXDO8N	RXDO8P	VDD_IO	TXDI9N	TXDI7N	TXDI7P	VDD_IO	TXDI8N
L	GND	RXDO9N	RXDO9P	GND	RXDO10N	RXDO10P	SE_REF	RXDO11P	TXDI5N	TXDI5P	GND	TXDI6N	TXDI6P	GND
M	RXDO12N	RXDO12P	VDD_IO	RXDO13N	RXDO13P	VDD_CMOS	RXDO14P	RXDO11N	VDD_CMOS	TXDI3N	TXDI3P	VDD_CMOS	TXDI4N	TXDI4P
N	VDD_IO	HOST/$\overline{HW}$	TRST	VDD_IO	RXDO15N	RXDO15P	RXDO14N	GND	TXDI1N	TXDI1P	VDD_IO	TXDI2N	TXDI2P	VDD_IO
P	TXCLKO16N	TXCLKO16P	GND	RXPCLKON	RXPCLKOP	GND	TXPCLKON	TXPCLKOP	GND	TXPCLKIN	TXPCLKIP	GND	TXDI0N	TXDI0P

TABLE OF CONTENTS

PIN DESCRIPTIONS

COMMON CONTROL

<table>
<tr><th>NAME</th><th>LEVEL</th><th>TYPE</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>LVTTL,
LVCMOS</td><td>I</td><td>E5</td><td>Master Reset Input
Active low signal. When this pin is pulled "Low" for more than 30ns, the internal registers are set to their default state. See the register description for the default values.
This pin is provided with an internal pull-up.</td></tr>
<tr><td>PIO_CFG1
PIO_CFG0</td><td>LVTTL,
LVCMOS</td><td>I</td><td>D3
E3</td><td>Parallel I/O Configuration
Selects parallel I/O to be differential LVDS, differential LVPECL, or Single-Ended LVPECL based on table below.
<table>
<tr><th>PIO_CFG [1:0]</th><th>VDD_I/O</th><th>Input Configuration</th><th>Output Configuration</th></tr>
<tr><td>00</td><td>3.3V</td><td>3.3V Differential LVPECL</td><td>3.3V Differential LVPECL</td></tr>
<tr><td>01</td><td>3.3V</td><td>3.3V Single-Ended LVPECL</td><td>3.3V Single-Ended LVPECL</td></tr>
<tr><td>10</td><td>3.3V</td><td>3.3V Differential LVDS</td><td>3.3V Differential LVDS</td></tr>
<tr><td>11</td><td colspan="3">Reserved</td></tr>
</table>
This pin is provided with an internal pull-down.</td></tr>
<tr><td>XRES1P
XRES1N</td><td>-</td><td>I</td><td>E14
F14</td><td>External LVDS Biasing Resistors
A 402Ω resistor with +/-1% tolerance should be placed across these 2 pins for proper biasing. Although unecessary in LVPECL operation, this resistor is required in LVDS operation. See Figure 8 on page 22.</td></tr>
<tr><td>SE_REF</td><td>Analog</td><td>O</td><td>L7</td><td>Single-Ended LVPECL Biasing Output Reference
VBB 100K output bias reference.
Maximum load capacitance is 30pF. Maximum sourcing/sinking capability is 750µA and 1000µA respectively.</td></tr>
<tr><td>SEREFDIS</td><td>LVTTL,
LVCMOS</td><td>I</td><td>C3</td><td>SE_REF Power down Control
Powers down SE_REF and reduces power consumption.
"Low" = SE_REF Enabled
"High" = SE_REF Disabled
This pin is provided with an internal pull-up.</td></tr>
<tr><td>REF1CLKP
REF1CLKN</td><td>LVPECL Diff</td><td>I</td><td>A13
B13</td><td>Reference Clock Input 1
This differential clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high-speed clock reference for this device. Pin REFREQSEL[1:0] determines the value used as the reference. See Pin REFREQSEL[1:0] for more details. Internally terminated and biased.</td></tr>
</table>

COMMON CONTROL

<table>
<tr><th>NAME</th><th>LEVEL</th><th>TYPE</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>REF2CLKP
REF2CLKN</td><td>LVPECL Diff</td><td>I</td><td>A11
B11</td><td>Reference Clock Input 2
This differential clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high-speed clock reference for this device. Pin REFREQSEL[1:0] determines the value used as the reference. See Pin REFREQSEL[1:0] for more details. Internally terminated and biased.</td></tr>
<tr><td>REFREQSEL1
/ SCLK</td><td>LVTTL,
LVCMOS</td><td>I</td><td>D12</td><td>Reference Clock Frequency Select
Hardware Mode REFREQSEL1 pin is used to select the frequency of the REF1CLK and/or REF2CLK input to the CMU and CDR.
<table><tr><th>REFREQSEL [1:0]</th><th>CMU REFERENCE FREQUENCY</th><th>CDR REFERENCE FREQUENCY</th></tr><tr><td>00</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td></tr><tr><td>01</td><td>155.52 MHz present on REF1CLK</td><td>166.63 MHz present on REF2CLK</td></tr><tr><td>10</td><td>166.63 MHz present on REF2CLK</td><td>155.52 MHz present on REF1CLK</td></tr><tr><td>11</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td></tr></table>
NOTE: Non-FEC rates require 155.52 MHz clock reference. FEC rates require 166.63 MHz clock reference
This pin is provided with an internal pull-down.

Host Mode This pin is functions as the microprocessor Serial Clock Input.</td></tr>
<tr><td>REFREQSEL0</td><td>LVTTL,
LVCMOS</td><td>I</td><td>E12</td><td>Reference Clock Frequency Select
REFREQSEL0 pin is used to select the frequency of the REF1CLK and/or REF2CLK input to the CMU and CDR.
<table><tr><th>REFREQSEL [1:0]</th><th>CMU REFERENCE FREQUENCY</th><th>CDR REFERENCE FREQUENCY</th></tr><tr><td>00</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td></tr><tr><td>01</td><td>155.52 MHz present on REF1CLK</td><td>166.63 MHz present on REF2CLK</td></tr><tr><td>10</td><td>166.63 MHz present on REF2CLK</td><td>155.52 MHz present on REF1CLK</td></tr><tr><td>11</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td></tr></table>
NOTE: Non-FEC rates require 155.52 MHz clock reference. FEC rates require 166.63 MHz clock reference
This pin is provided with an internal pull-down.</td></tr>
</table>

COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
PRBS_EN	LVTTL, LVCMOS	I	D9	**2^{23}-1 PRBS TEST Pattern Enable** Generates 2^{23}-1 Pseudo Random Binary Sequence test patterns and analyzes in the receiving block for proper reception. "Low" = Normal Mode "High" = PRBS pattern generator and analyzer Enabled. ***NOTE:*** *A Local Loopback of some type such as Digital Local Loopback or an optical cable loopback is expected to be used in conjunction with PRBS_EN in order for the PRBS analyzer to receive the PRBS pattern.* This pin is provided with an internal pull-down.
PRBS_ERR /SDO	LVCMOS	O	E9	**2^{23}-1 PRBS Pattern Validation Error** **Hardware Mode** Indicates an error condition has occurred/is occuring in the validation of generated PRBS pattern. "Low" = Un-erred transmission and reception of PRBS pattern. "High" = Error Condition occurrence. **Host Mode** This pin is functions as the microprocessor Serial Data Output.
$\overline{\text{RLOOPS\_}}$ - $\overline{\text{PRBSCLR}}$	LVTTL, LVCMOS	I	F11	**Serial Remote Loopback** **Normal Mode** The serial remote loopback mode interconnects the receive serial data input to the transmit serial data output. If serial remote loopback is enabled, the 16-bit parallel transmit data input is ignored while the 16-bit parallel receive data output and parallel receive clock output is maintained. "Low" = Serial Remote Loopback Mode Enabled "High" = Disabled **PRBSTest Mode** When PRBS_EN is asserted, this bit is used to clear or reset PRBS_ERR error condition. Serial Remote Loopback is not available in PRBS Test Mode. "Low" = Clears PRBS_ERR condition "High" = Normal Mode This pin is provided with an internal pull-up.

COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
$\overline{\text{DLOOP}}$	LVTTL, LVCMOS	I	E11	**Digital Local Loopback** The digital local loopback mode interconnects the 16-bit parallel transmit data and parallel transmit clock input to the 16-bit parallel receive data and parallel receive clock output respectively while maintaining the transmit serial data output. If digital local loopback is enabled, the receive serial data input is ignored. "Low" = Digital Local Loopback Mode Enabled "High" = Disabled This pin is provided with an internal pull-up.
LOOPTM_NOJA / SDI	LVTTL, LVCMOS	I	C10	**Loop Timing Mode With No Jitter Attenuation** **Hardware Mode** When the loop timing mode is activated, the external local reference clock input to the CMU is replaced with the 1/16th of the high-speed recovered receive clock coming from the CDR. "Low" = Disabled "High" = Loop timing Activated This pin is provided with an internal pull-down. **Host Mode** This pin is functions as the microprocessor Serial Data Input.

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXDI0P TXDI0N TXDI1P TXDI1N TXDI2P TXDI2N TXDI3P TXDI3N TXDI4P TXDI4N TXDI5P TXDI5N TXDI6P TXDI6N TXDI7P TXDI7N TXDI8P TXDI8N TXDI9P TXDI9N TXDI10P TXDI10N TXDI11P TXDI11N TXDI12P TXDI12N TXDI13P TXDI13N TXDI14P TXDI14N TXDI15P TXDI15N	LVDS, LVPECL Diff and SE	I	P14 P13 N10 N9 N13 N12 M11 M10 M14 M13 L10 L9 L13 L12 K12 K11 J14 K14 J10 K10 J13 J12 H9 J9 H12 H11 G11 G10 F12 G12 G8 G7	**Transmit Parallel Data Input** The 155.52 Mbps 16-bit parallel transmit data input should be applied to the transmit parallel bus simultaneously to be sampled at the rising edge of the TXPCLKIP/N input. The 16-bit parallel interface is multiplexed into the transmit serial output interface, MSB first (TXDI15P/N). TXDI[15:0]P/N 100 Ω internal termination is controlled by INTERM pin or register bit. Inputs are internally biased to VDD_IO - 1V for AC coupled applications. For LVPECL Single-Ended applications, either a 100K VBB bias reference must be provided or the SE_REF pin can also be used to bias and connected all the negative polarity "N" pins. ***NOTE:*** *The XRT91L82 can accept 166.63 Mbps 16-bit parallel transmit data input for Forward Error Correction (FEC) Applications.*
TXOP TXON	CMLDIFF	O	A6 A5	**Transmit Serial Data Output** The transmit serial data output stream is generated by multiplexing the 16-bit parallel transmit data input into a 2.488 Gbps serial data output stream. In Forward Error Correction, the transmit serial data output stream is 2.666 Gbps.
TXSWING / $\overline{\text{INT}}$	LVTTL, LVCMOS	I/O	D10	**Transmit Serial CML Output Swing Mode** **Hardware Mode** Selects the generated transmit serial CML Output swing to the optical module. "Low" = Low Swing CML Mode "High" = High Swing CML Mode This pin is provided with an internal pull-up. **Host Mode** This pin is functions as the microprocessor Interrupt Output. ***NOTE:*** *This pin becomes an open drain output in Host Mode and requires an external pull-up resistor.*

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXSCLKOP TXSCLKON	CMLDIFF	O	A9 A8	**2.488/2.666 GHz Transmit Serial Clock Output** A high-speed 2.488/2.666 GHz Transmit serial clock output that can be used to retime TXOP/N.
TXSCLKOOFF / $\overline{CS}$	LVTTL, LVCMOS	I	C9	**2.488/2.666 GHz Hi-speed Serial Clock Output Tristate** **Hardware Mode** Tristates TXSCLKOP/N output and reduces power consumption. "Low" = TXSCLKOP/N output Enabled "High" = Tristates TXSCLKOP/N output This pin is provided with an internal pull-up. **Host Mode** This pin is functions as the microprocessor Chip Select Input.
INTERM / VCXO_IN	LVTTL, LVCMOS / SE- LVCMOS	I	E4	**Transmit Parallel Bus Input Internal Termination** **Hardware Mode** Provides 100Ω line-to-line internal termination to TXDI[15:0]P/N and TXPCLKIP/N. "Low" = Disabled "High" = TXDI[15:0]P/N and TXPCLKIP/N internally terminated. This pin is provided with an internal pull-down. **Host Mode - Voltage Controled 77.76/83.31 MHz or 155.52/166.63 MHz External Oscillator Input** This 77.76/83.31 MHz or 155.52/166.63 MHz Single-Ended LVCMOS clock input is used for the transmit PLL jitter attenuation. ALTFREQSEL register bit determines the value used as the reference. Software register bit VCXOSEL allows the selection of the De-Jitter VCXO Mode. See ALTFREQSEL and VCXO_SEL software register bit description for more details.
TXPCLKIP TXPCLKIN	LVDS, LVPECL Diff and SE	I	P11 P10	**Transmit Parallel Clock Input** 155.52 MHz clock input used to sample the 16-bit parallel transmit data input TXDI[15:0]P/N. TXPCLKIP/N 100 Ω internal termination is controlled by INTERM pin or register bit. TXPCLKIP/N inputs are internally biased to VDD_IO - 1V for AC coupled application. ***NOTE:*** *The XRT91L82 can accept a 166.63 MHz transmit clock input for Forward Error Correction (FEC) Applications.*
TXPCLKOP TXPCLKON	LVDS, LVPECL Diff and SE	O	P8 P7	**Transmit Parallel Clock Output** This 155.52 MHz clock can be used for the downstream device to generate the TXDI[15:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48 transceiver to be in synchronization. ***NOTE:*** *The XRT91L82 can output a 166.63 MHz transmit clock output for Forward Error Correction (FEC).*

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXCLKO16P TXCLKO16N	LVDS, LVPECL Diff and SE	O	P2 P1	**Auxiliary Clock Output (155.52/19.44 MHz)** 155.52 or 19.44 MHz auxiliary clock derived from CMU output. This clock can also be used for the downstream device as a reference for generating the TXDI[15:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48 transceiver to be in synchronization. The frequency output of this pin is controlled by TXCLKO16SEL. ***NOTE:*** *This pin can output a 166.63/20.83 MHz transmit clock output for Forward Error Correction (FEC).*
TXCLKO16SEL	LVTTL, LVCMOS	I	C4	**Auxiliary Clock Output Select** This pin is used to select the auxiliary clock output. "Low" = TXCLKO16P/N outputs 155.52/ 166.63 MHz "High" = TXCLKO16P/N outputs 19.44/ 20.83 MHz This pin is provided with an internal pull-down.
LOCKDET_CMU	LVCMOS	O	C6	**CMU Lock Detect** This pin is used to monitor the lock condition of the clock multiplier unit. "Low" = CMU Out of Lock "High" = CMU Locked
OVERFLOW	LVCMOS	O	D6	**Transmit FIFO Overflow** This pin is used to monitor the transmit FIFO status. "Low" = Normal Status "High" = Overflow Condition
FIFO_RST	LVTTL, LVCMOS	I	D5	**FIFO Control Reset** FIFO_RST should be held "High" for a minimum of 2 TXPCLKOP/N cycles after powering up and during manual FIFO reset. After the FIFO_RST pin is returned "Low," it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Upon an interrupt indication that the FIFO has an overflow condition, this pin is used to reset or flush out the FIFO. "Low" = Normal Operation "High" = Manual FIFO Reset This pin is provided with an internal pull-down. ***NOTES:*** **1.** ***In Hardware Mode****, to automatically reset the FIFO, tie the OVERFLOW output pin to the FIFO_RST input pin or if desired, an asynchronous FIFO reset pin and the OVERFLOW output pin can be logically 'OR'ed and the output tied to the FIFO_RST input pin.* **2.** ***In Host Mode****, this pin is disabled and not used. FIFO_RST is asserted through Microprocessor Control Register 0x03H Bit-D0. A FIFO_AUTORST bit is also available on Microprocessor Control Register 0x03H Bit-D1.*

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXDO0P RXDO0N RXDO1P RXDO1N RXDO2P RXDO2N RXDO3P RXDO3N RXDO4P RXDO4N RXDO5P RXDO5N RXDO6P RXDO6N RXDO7P RXDO7N RXDO8P RXDO8N RXDO9P RXDO9N RXDO10P RXDO10N RXDO11P RXDO11N RXDO12P RXDO12N RXDO13P RXDO13N RXDO14P RXDO14N RXDO15P RXDO15N	LVDS, LVPECL Diff and SE	O	G5 G4 H4 H3 H7 H6 H8 J8 J3 J2 J6 J5 K2 K1 K5 K4 K8 K7 L3 L2 L6 L5 L8 M8 M2 M1 M5 M4 M7 N7 N6 N5	**Receive Parallel Data Output** 155.52 Mbps 16-bit parallel receive data output is updated simultaneously on the falling edge of the RXPCLKOP/N output. The 16-bit parallel interface is de-multiplexed from the receive serial data input, MSB first (RXDO15P/N). For LVPECL Single-Ended applications, all the negative polarity "N" pins should not be connected. ***NOTE:*** *The XRT91L82 can output 166.63 Mbps 16-bit parallel receive data output for Forward Error Correction (FEC) Applications.*
RXIP RXIN	CMLDIFF	I	A2 A3	**Receive Serial Data Input** The receive serial data stream of 2.488 Gbps is applied to these input pins. In Forward Error Correction, the receive serial data stream is 2.666 Gbps. This pin is internally biased and terminated.
RXPCLKOP RXPCLKON	LVDS, LVPECL Diff and SE	O	P5 P4	**Receive Parallel Clock Output** 155.52 MHz parallel clock output used to update the 16-bit parallel receive data output RXDO[15:0]P/N at the falling edge of this clock. ***NOTE:*** *The XRT91L82 can output a 166.63 MHz receive clock output for Forward Error Correction (FEC).*

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
$\overline{\text{CDRLCKREF}}$	LVTTL, LVCMOS	I	C12	**CDR's Recovered High-speed Serial Clock Reference** Controls CDR's operation. "Low" = Forced to lock to CDR PLL reference training clock "High" = Normal Operation (Locked to incoming serial data) This pin is provided with an internal pull-up.
$\overline{\text{DISRD}}$ /PRBS_LOCK	LVTTL, LVCMOS	I/O	D4	**Receive Parallel Data Output Disable** **Hardware Mode** If this pin is set to "0", the 16-bit parallel receive data output will asynchronously mute. "Low" = Forces RXDO[15:0]P/N to a logic state of "0" "High" = Normal Mode This pin is provided with an internal pull-up. **Host Mode 2^{23}-1 PRBS Pattern Lock Output Indicator** This pin indicates the current state condition of the PRBS pattern analyzer when the PRBS pattern generator is enabled. "Low" = PRBS pattern analyzer currently Out of Lock "High" = PRBS pattern analyzer currently Locked
$\overline{\text{DISRDCLK}}$	LVTTL, LVCMOS	I	D11	**Receive Parallel Clock Output Disable** This pin is used to asynchronously control the activity of the parallel receive clock output. "Low" = Forces RXPCLKOP/N to a logic state of "0" "High" = Normal Mode This pin is provided with an internal pull-up.
LOCKDET_CDR	LVCMOS	O	C5	**CDR Lock Detect** This pin is used to monitor the lock condition of the clock and data recovery unit. "Low" = CDR Out of Lock "High" = CDR Locked
SDEXT	LVTTL, LVCMOS	I	C2	**Signal Detect Input from Optical Module** When inactive, it will automatically mute received data output bus RXDO[15:0]P/N upon Loss of Signal Detection (LOSD) condition. "Active" = Normal Operation (SDEXT detects signal presence) "Inactive" =Mutes upon LOSD (SDEXT detects signal absence) This pin is provided with an internal pull-up.
POLARITY	LVTTL, LVCMOS	I	E10	**Polarity for SDEXT Input** Controls the Signal Detect polarity convention of SDEXT. "Low" = SDEXT is active "Low" "High" = SDEXT is active "High" This pin is provided with an internal pull-up.

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXCAP1P	Analog	I	E1	**External Receive Loop Filter** **Hardware Mode** This pin is required for the external loop filter capacitor and resistors. See Figure 5 on page 19. **Host Mode - No Connect** This pin is not connected in Host Mode.
RXCAP1N / CP_OUT	Analog	I/O	F1	**External Receive Loop Filter** **Hardware Mode** This pin is required for the external loop filter capacitor and resistors. See Figure 5 on page 19. **Host Mode - Charge Pump Output (for external VCXO)** The nominal output of the charge pump current is 250µA.

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
AVDD_RX	PWR	C1, D2, G2, H1	**Analog 1.8V Receiver Power Supply** AVDD_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD_RX power supply pins should have bypass capacitors to the nearest ground.
AVDD_TX	PWR	C14, D13, G13, H14	**Analog 1.8V Transmitter Power Supply** AVDD_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD_TX power supply pins should have bypass capacitors to the nearest ground.
VDD_CML	PWR	A4, A7, A10, A12, B3, B5, B7, B9, C11, C13	**CML 1.8V Power Supply** These pins require a 1.8V potential.
VDD_CMOS	PWR	E6, E8, F3, F5, F7, F9, J4, J7, M6, M9, M12	**Digital 1.8V Power Supply** VDD_CMOS should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDD_CMOS power supply pins should have bypass capacitors to the nearest ground.
VDD_IO	PWR	G3, G9, J1, J11, K3, K6, K9, K13, M3, N1, N4, N11, N14	**3.3V LVPECL/ 3.3V LVDS Input /Output Bus Power Supply and 3.3V Digital I/O Power Supply** These pins require a 3.3V potential in LVPECL or LVDS operation. These pins also power the 3.3V Digital I/O Power Supply.
GND	GND	A1, A14, B1, B2, B4, B6, B8, B10, B12, B14, D1, D14, E2, E7, E13, F2, F4, F6, F8, F10, F13, G1, G6, G14, H2, H5, H10, H13, L1, L4, L11, L14, N8, P3, P6, P9, P12	**Ground for 3.3V / 1.8V Digital Power Supplies** It is recommended that all ground pins of this device be tied together.

NOTE: *For VDD_{IO}=3.3V, all input control pins are LVCMOS and LVTTL compatible. All output control pins are LVCMOS compatible only.*

SERIAL MICROPROCESSOR INTERFACE

NAME	LEVEL	TYPE	PIN	DESCRIPTION
HOST/$\overline{HW}$	LVTTL, LVCMOS	I	N2	**Host or Hardware Mode Select Input** The XRT91L82 offers two modes of operation for interfacing to the device. The Host mode uses a serial microprocessor interface for programming individual registers. The Hardware mode is controlled by the state of the hardware pins set by the user. When left unconnected, by default, the device is configured in the Hardware mode. "Low" = Hardware Mode "High" = Host Mode This pin is provided with an internal pull-down.
TXSCLKOOFF / $\overline{CS}$	LVTTL, LVCMOS	I	C9	**Chip Select Input (Host Mode Only)** Active "Low" signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial microprocessor is disabled when the chip select signal returns "High". ***NOTES:*** **1.** *The serial microprocessor interface does **not** support burst mode. Chip Select must be de-asserted after each operation cycle.* **2.** *Chip Select is only active in Host Mode.* This pin is provided with an internal pull-up.
REFREQSEL1 / SCLK	LVTTL, LVCMOS	I	D12	**Serial Clock Input (Host Mode Only)** Once $\overline{CS}$ is pulled "Low", the serial microprocessor interface requires 16 clock cycles for a complete Read or Write operation. Serial Clock Input is only active in Host Mode. This pin is provided with an internal pull-down.
LOOPTM_NOJA / SDI	LVTTL, LVCMOS	I	C10	**Serial Data Input (Host Mode Only)** When $\overline{CS}$ is pulled "Low", the serial data input is sampled on the rising edge of SCLK. Serial Data Input is only active in Host Mode. This pin is provided with an internal pull-down.
PRBS_ERR / SDO	LVCMOS	O	E9	**Serial Data Output (Host Mode Only)** If a Read function is initiated, the serial data output is updated on the falling edge of SCLK8 through SCLK15, with the LSB (D0) updated first. This enables the data to be sampled on the rising edge of SCLK9 through SCLK16. Serial Data Output is only active in Host Mode.
TXSWING / $\overline{INT}$	LVCMOS	O	D10	**Interrupt Output (Host Mode Only)** Active "Low" signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". Interrupt Output is only active in Host Mode. ***NOTE:*** *This pin is an open drain output and requires an external pull-up resistor.*

JTAG

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCK	C7	I	**Test clock:** Boundary Scan Clock Input. This pin is provided with an internal pull-down.
TMS	D8	I	**Test Mode Select:** Boundary Scan Mode Select Input. JTAG is disabled by default. ***Note**: This input pin should be pulled "Low" for JTAG operation* This pin is provided with an internal pull-up.
TDI	C8	I	**Test Data In:** Boundary Scan Test Data Input This pin is provided with an internal pull-up.
TDO	D7	O	**Test Data Out:** Boundary Scan Test Data Output
TRST	N3	I	**JTAG Test Reset Input** ***Note**: This input pin should be pulled "Low" to reset JTAG* This pin is provided with an internal pull-up.

NO CONNECTS

NAME	LEVEL	TYPE	PIN	DESCRIPTION
None	N/A	N/A	None	**No Connect** This pin can be left floating or tied to ground.

1.0 FUNCTIONAL DESCRIPTION

The XRT91L82 Transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The Transceiver converts 16-bit parallel data at 155.52/166.63 MHz to a serial CML bit stream at 2.488/2.666 Gbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), and receive clock and data recovery (CDR) unit. The Transceiver is divided into Transmit and Receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

1.1 Hardware Mode vs. Host Mode

Functionality of the STS-48/STM-16 Transceiver can be configured by using either Host mode or Hardware mode. Hardware mode is selected by pulling HOST/$\overline{HW}$ "Low" or leaving this pin unconnected. The transceiver functionality is then controlled by the hardware pins described in the Hardware Pin Descriptions. However, if Host mode is selected by pulling HOST/$\overline{HW}$ "High", the functionality is controlled by programming internal R/W registers using the Serial Microprocessor interface. Whether using Host or Hardware mode, the functionality remains the same. Therefore, the following sections describe the functionality rather than how each function is controlled. The Hardware Pin Descriptions and the Register Bit Descriptions concentrate on configuring the device.

1.2 Clock Input Reference

The XRT91L82 can accept both 155.52 MHz non-FEC or 166.63 MHz FEC clock input at REF1CLKP/N and/or REF2CLKP/N as its internal timing reference for generating higher speed clocks. The reference clock can be provided with one of two frequencies chosen by REFREQSEL[1:0]. The reference frequency options for the XRT91L82 are listed in Table 1.

TABLE 1: REFERENCE FREQUENCY OPTIONS (NORMAL MODE/ FEC RATE)

REFREQSEL [1:0]	CMU REFERENCE CLOCK FREQUENCY	CDR REFERENCE CLOCK FREQUENCY	REF1CLK CLOCK FREQUENCY	REF2CLK CLOCK FREQUENCY	TRANSMIT DATA RATE	RECEIVE DATA RATE
00	REF1CLK	REF1CLK	155.52 MHz non-FEC	not used	2.488 Gbps non-FEC	2.488 Gbps non-FEC
01	REF1CLK	REF2CLK	155.52 MHz non-FEC	166.63 MHz FEC	2.488 Gbps non-FEC	2.666 Gbps FEC
10	REF2CLK	REF1CLK	155.52 MHz non-FEC	166.63 MHz FEC	2.666 Gbps FEC	2.488 Gbps non-FEC
11	REF2CLK	REF2CLK	not used	166.63 MHz FEC	2.666 Gbps FEC	2.666 Gbps FEC

1.3 Alternate Clock Input Reference (Host Mode Only)

In Host mode, the XRT91L82 has the option to accept a lower reference frequency of 77.76 MHz non-FEC or 83.31 MHz FEC clock input at REF1CLKP/N and/or REF2CLKP/N. To use this feature, register bit ALTFREQSEL must be set "Low" on bit- D5 of ”Configuration Control Register (0x07h)”. The alternate reference frequency options are listed below in Table 2.

TABLE 2: ALTERNATE REFERENCE FREQUENCY OPTIONS (NORMAL MODE/ FEC RATE)

REFREQSEL [1:0]	CMU REFERENCE CLOCK FREQUENCY	CDR REFERENCE CLOCK FREQUENCY	REF1CLK CLOCK FREQUENCY	REF2CLK CLOCK FREQUENCY	TRANSMIT DATA RATE	RECEIVE DATA RATE
00	REF1CLK	REF1CLK	77.76 MHz non-FEC	not used	2.488 Gbps non-FEC	2.488 Gbps non-FEC
01	REF1CLK	REF2CLK	77.76 MHz non-FEC	83.31 MHz FEC	2.488 Gbps non-FEC	2.666 Gbps FEC
10	REF2CLK	REF1CLK	77.76 MHz non-FEC	83.31 MHz FEC	2.666 Gbps FEC	2.488 Gbps non-FEC
11	REF2CLK	REF2CLK	not used	83.31 MHz FEC	2.666 Gbps FEC	2.666 Gbps FEC

1.4 Data Latency

Due to different operating modes and data logic paths through the device, there is an associated latency from data ingress to data egress. Table 3 specifies the data latency for a typical path.

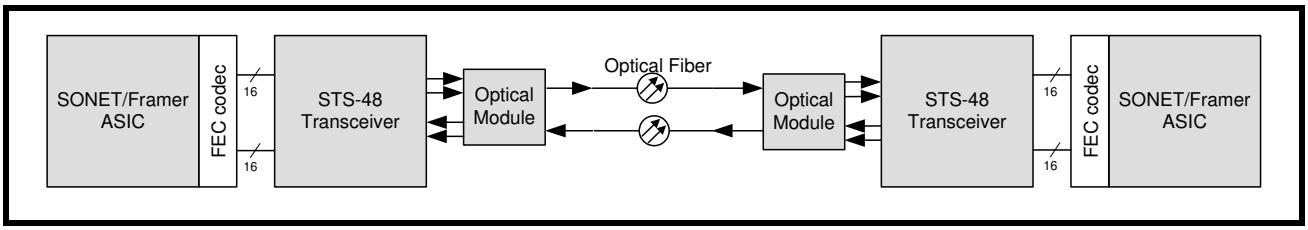
TABLE 3: DATA INGRESS TO DATA EGRESS LATENCY

MODE OF OPERATION	DATA PATH	CLOCK REFERENCE	MAXIMUM REFNCLK CLOCK CYCLES
Thru-mode	Data on TXDI[15:0]P/N to data on TXOP/N	REF1CLKP/N or REF2CLKP/N Clock	18 to 20

1.5 Forward Error Correction (FEC)

Forward Error Correction is used to control errors along a one-way path of communication. FEC sends extra information along with data which can be used by a receiver to check and correct the data without requesting re-transmission of the original information. It does so by introducing a known structure into a data sequence prior to transmission. The most common methods are to replace a 14-bit data packet with a 15-bit codeword structure, or to replace a 17-bit data packet with an 18-bit codeword structure. The XRT91L82 supports FEC by accepting a clock input reference frequency of 83.31 or 166.63 MHz. Both reference frequencies allows the transmit 16-bit parallel data input to be applied to the STS-48 transceiver at 166.63 Mbps which is converted to a 2.666 Gbps serial output stream to an optical module. A simplified block diagram of FEC is shown in Figure 3.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF FORWARD ERROR CORRECTION



1.6 PRBS Pattern Generator and Analyzer

The XRT91L82 contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. With the PRBS_EN asserted, the transmitter will send out PRBS pattern of 2^{23}-1 in STS-48/48c or STM-16 rate. At the same time, the receiver PRBS detector is also enabled. Whenever the PRBS detector is not in sync, the PRBS_ERR bit will be set to “1”. To clear the erred condition, $\overline{\text{PRBSCLR}}$ must be toggled "Low." If the correct PRBS pattern is detected by the receiver, then PRBS_ERR pin will go “Low” to indicate PRBS synchronization has been achieved, otherwise PRBS_ERR will remain "1." $\overline{\text{PRBSCLR}}$ shares pin F11 with $\overline{\text{RLOOPS}}$. Serial Remote Line Loopback ($\overline{\text{RLOOPS}}$) is disabled when PRBS_EN is enabled.

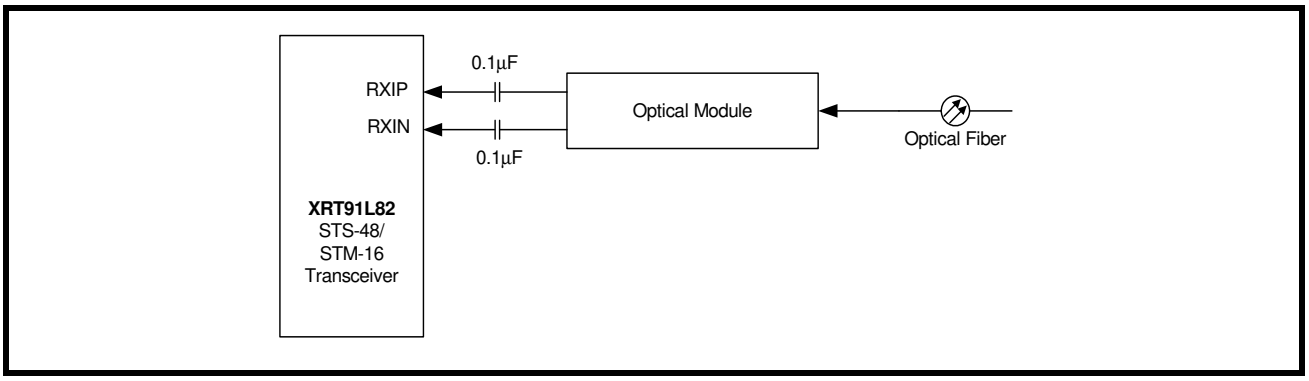
2.0 RECEIVE SECTION

The receive section of XRT91L82 includes the differential inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter. The receiver accepts the high-speed Non-Return to Zero (NRZ) serial data at 2.488/2.666 Gbps through the differential input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into 16-bit-wide 155.52/166.63 Mbps parallel data and presented to the RXDO[15:0]P/N parallel interface. This parallel interface can be configured for Differential LVPECL/LVDS, or Single-Ended LVPECL operation. A divide-by-16 version of the high-speed recovered clock, RXPCLKOP/N is used to synchronize the transfer of the 16-bit RXDO[15:0]P/N data with the receive portion of the upstream device. Upon initialization or loss of signal or loss of lock the 155.52 MHz or 166.63 MHz external local reference clock is used to start-up the clock recovery phase-locked loop for proper operation. In Host Mode, a special loopback feature can be configured when parallel remote loopback ($\overline{\text{RLOOPP}}$) is used in conjunction with de-jittered loop-time mode that allows the re-transmitted data to comply with ITU and Bellcore jitter generation specifications.

2.1 Receive Serial Input

The receive serial CML inputs are applied to RXIP/N. The receive serial inputs can be AC or DC coupled to an optical module or an electrical interface. A simplified AC coupled block diagram is shown in Figure 4.

FIGURE 4. RECEIVE SERIAL INPUT INTERFACE BLOCK



NOTE: *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

The 2.488/2.666 Gbps high-speed differential CML RXIP/N input swing characteristics is shown in Table 4. Figure 17, “CML Differential Voltage Swing,” on page 29 shows the CML differential voltage swing.

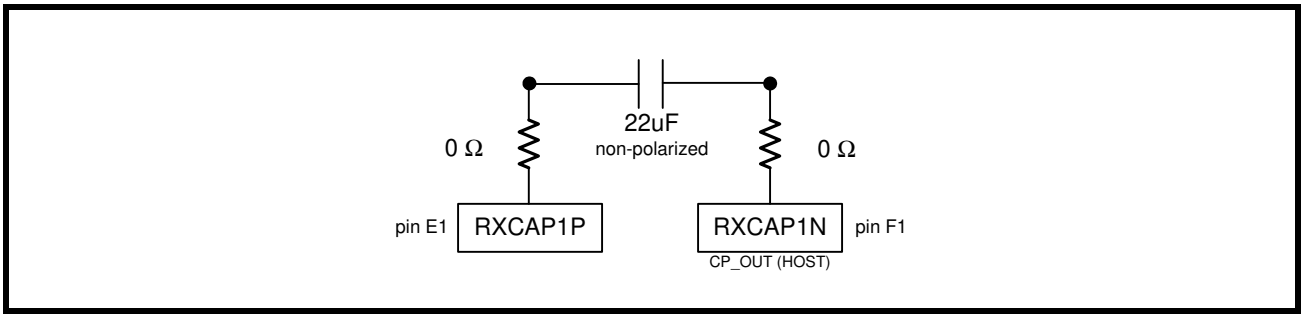
TABLE 4: DIFFERENTIAL CML INPUT SWING PARAMETERS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
ΔV_{INDIFF}	Differential Input Voltage Swing	100		2000	mV
ΔV_{INSE}	Single-Ended Input Voltage Swing	50		1000	mV
ΔV_{INBIAS}	Input Bias Range (AC Coupled)	VDD_CML - 0.4		VDD_CML - 0.2	V
R_{DIFF}	Differential Input Resistance	80	100	120	Ω

2.2 External Receive Loop Filter Capacitors

These external loop filter 0Ω resistors and 22µF non-polarized capacitor provide the necessary components to achieve the required receiver jitter performance. They must be well isolated to prohibit noise entering the CDR block. Figure 5 shows the pin connections and external loop filter components. The external loop filter is not needed while in host mode and RXCAP1N becomes the charge pump output for the external VCXO.

FIGURE 5. EXTERNAL LOOP FILTER



2.3 Receive Clock and Data Recovery

The clock and data recovery unit accepts the high-speed NRZ serial data from the differential CML receiver and generates a clock that is the same frequency as the incoming data. The clock recovery utilizes REF1CLKP/N and/or REF2CLKP/N to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the local reference clock within ±500 ppm. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock. When this condition occurs the PLL will declare Loss of Lock and the LOCKDET_CDR signal will be pulled "Low." Whenever a Loss of Lock/Loss of Signal Detection (LOSD) event occurs, the CDR will continue to supply a receive clock (based on the local reference clock) to the upstream framer device. A Loss of Lock condition will also be declared when the external SDEXT becomes inactive. When the SDEXT is de-asserted by the optical module or when $\overline{\text{DISRD}}$ is asynchronously asserted "Low," receive parallel data output will be forced to a logic zero state for the entire duration that a LOSD condition is detected or for as long as $\overline{\text{DISRD}}$ is asserted "Low." This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. When the SDEXT becomes active and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source, the clock recovery PLL will switch and lock back onto the incoming receive data stream and the lock detect output (LOCKDET_CDR) will go active. Table 5 specifies the Clock and Data Recovery Unit performance characteristics.

TABLE 5: CLOCK AND DATA RECOVERY UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	45		55	%
REF_{TOL}	Reference clock frequency tolerance[1]	-20		+20	ppm
$OCLK_{JIT}$	Clock output jitter generation with 155.52 MHz reference clock		5	7	mUI_{rms}
$OCLK_{JIT}$	Clock output jitter generation with 166.63 MHz reference clock		5	7	mUI_{rms}
TOL_{JIT}	Input jitter tolerance with 1 MHz < f < 20 MHz PRBS pattern	0.4		0.7	UI
$OCLK_{FREQ}$	Frequency output	2.488		2.667	GHz
$OCLK_{DUTY}$	Clock output duty cycle	45		55	%

Jitter specification is defined using a 12kHz to 20MHz appropriate SONET/SDH filter.

[1]Required to meet SONET output frequency stability requirements.

2.4 External Signal Detection

XRT91L82 supports external Signal Detection (SDEXT). The external Signal Detect function is supported by the SDEXT input. This input is coming from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices, the polarity of this signal can be either active "Low" or active "High." The SDEXT and POLARITY inputs are Exclusive OR’ed to generate the internal Loss of Signal Detect (LOSD) declaration and Mute upon LOSD control signal. Whenever an external SD is absent, the XRT91L82 will automatically force the receive parallel data output to a logic state "0" for the entire duration that a LOSD condition is declared as well as update the status registers whenever the host mode serial microprocessor interface feature is active. This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. Table 6 specifies SDEXT declaration polarity settings.

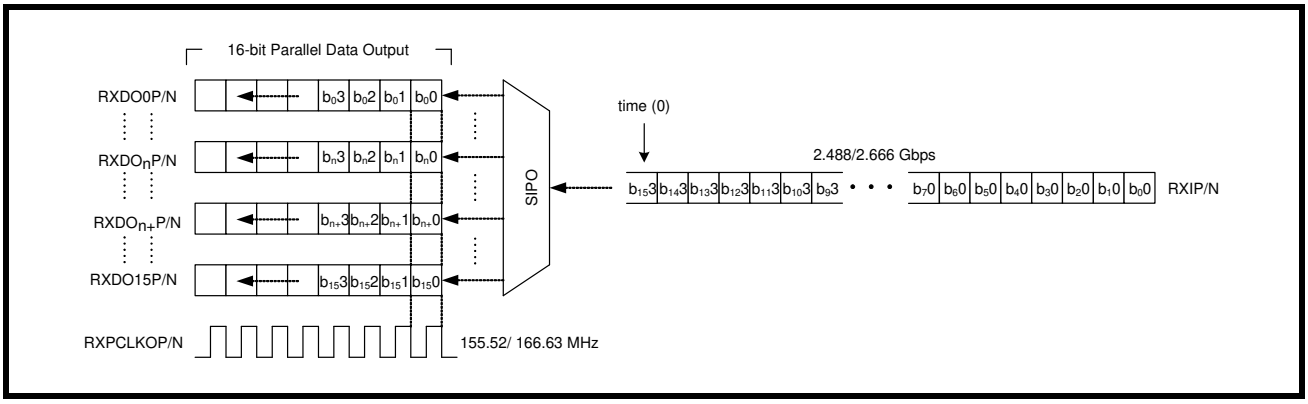
TABLE 6: LOSD DECLARATION POLARITY SETTING

SDEXT	POLARITY	INTERNAL SIGNAL DETECT	RECEIVE PARALLEL DATA OUTPUT RXDO[15:0]P/N	CLOCK AND DATA RECOVERY PLL REFERENCE LOCK
0	**0**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module. **LOSD not declared.**	Not Muted	Hi-Spd Received Data
0	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module. **LOSD declared.**	Muted	Local Reference Clock
1	**0**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module. **LOSD declared.**	Muted	Local Reference Clock
1	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module. **LOSD not declared.**	Not Muted	Hi-Spd Received Data

2.5 Receive Serial Input to Parallel Output (SIPO)

The SIPO is used to convert the 2.488/2.666 Gbps serial data input to 155.52/166.63 Mbps parallel data output which can interface to a SONET Framer/ASIC. The SIPO bit de-interleaves the serial data input into a 16-bit parallel output to RXDO[15:0]P/N. A simplified block diagram is shown in Figure 6.

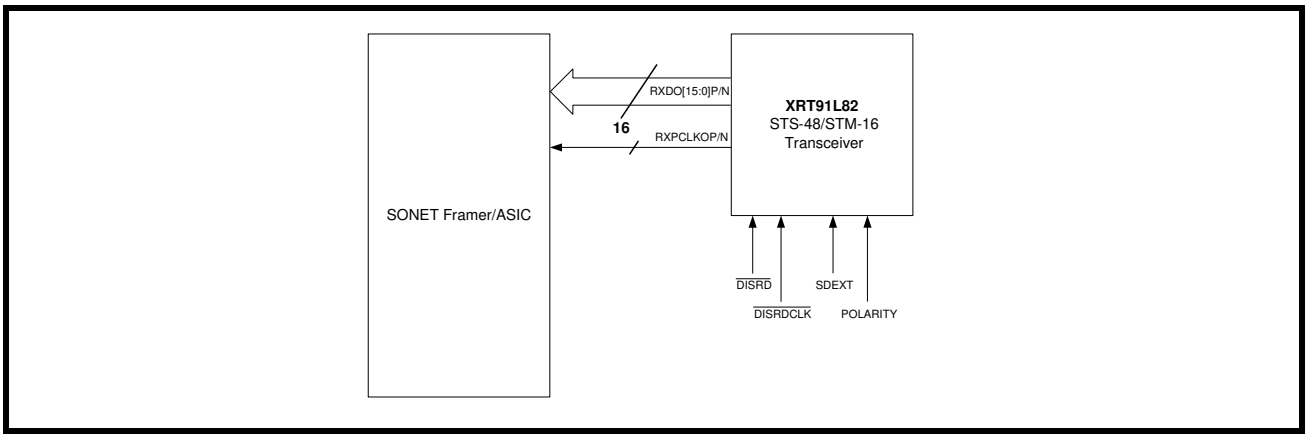
FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF SIPO



2.6 Receive Parallel Output Interface

The 16-bit LVDS, Differential LVPECL or Single-Ended LVPECL 155.52/166.63 Mbps parallel data output of the receive path is used to interface to a SONET Framer/ASIC synchronized to the recovered clock. A simplified block diagram is shown in Figure 7.

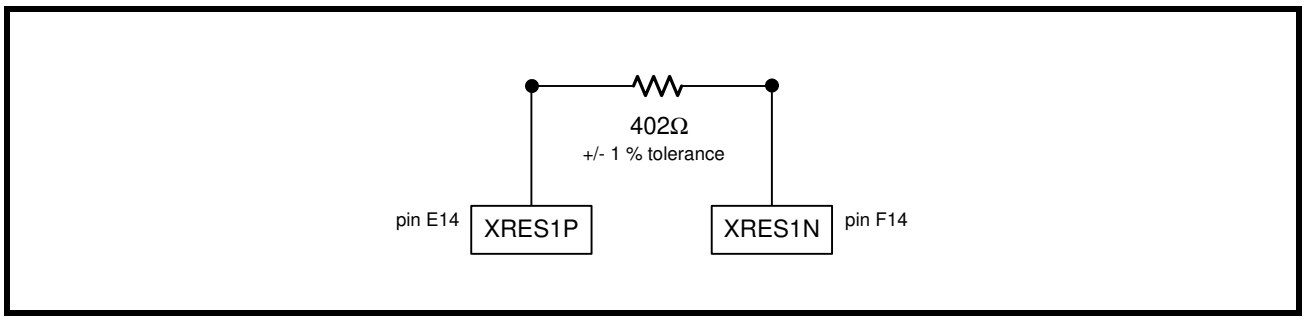
FIGURE 7. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK



2.7 Receive Parallel Interface LVDS Operation

When operating the 16-bit Differential bus in LVDS mode, a 402Ω external resistor is needed across XRES1P and XRES1N to properly bias the RXDO[15:0]P/N and RXPCLKOP/N pins. Figure 8 shows the proper biasing resistor installed.

FIGURE 8. LVDS EXTERNAL BIASING RESISTORS



2.8 Parallel Receive Data Output Disable/Mute Upon LOSD

The parallel receiver data outputs are automatically pulled "Low" during a LOSD condition to prevent data chattering. However, the user must select the proper SDEXT polarity for the optical module used. In addition, by pulling $\overline{\text{DISRD}}$ "Low", the receiver data outputs will be muted asynchronously or forced to a logic state of "0" regardless of the data input stream.

2.9 Parallel Receive Clock Output Disable

Like $\overline{\text{DISRD}}$, $\overline{\text{DISRDCLK}}$ is used to mute the parallel receiver clock output RXPCLKOP/N regardless of the data input stream. By pulling $\overline{\text{DISRDCLK}}$ "Low", the receiver clock output will be asynchronously muted whenever desired.

2.10 Receive Parallel Data Output Timing

The receive parallel data output from the STS-48/STM-16 receiver will adhere to the setup and hold times shown in Figure 9 and Table 7.

FIGURE 9. RECEIVE PARALLEL OUTPUT TIMING

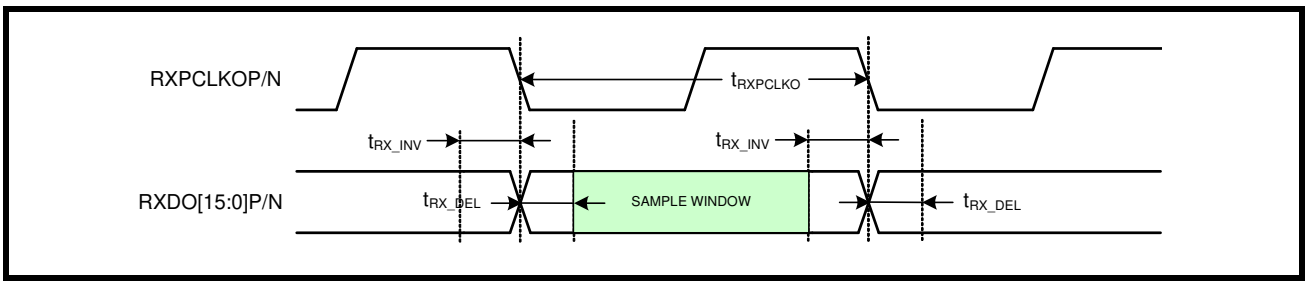


TABLE 7: RECEIVE PARALLEL DATA AND CLOCK OUTPUT TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{RXPCLKO}$	Receive parallel clock output period (155.52 MHz non-FEC rate)		6.43		ns
$t_{RXPCLKO}$	Receive parallel clock output period (166.63 MHz FEC rate)		6.00		ns
t_{RX_INV}	RXPCLKOP/N "Low" to data invalid window			1000	ps
t_{RX_DEL}	RXPCLKOP/N "Low" to data delay			900	ps
RX_{DUTY}	RXPCLKOP/N Duty Cycle	45		55	%