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GENERAL DESCRIPTION

The XRT94L31 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L31 interfaces directly to the optical transceiver.

The XRT94L31 processes the section, line and path overhead in the SONET/SDH data stream. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L31 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L31 memory map or from external interface. A1, A2 framing pattern, C1 byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L31 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L31 provides 3 mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

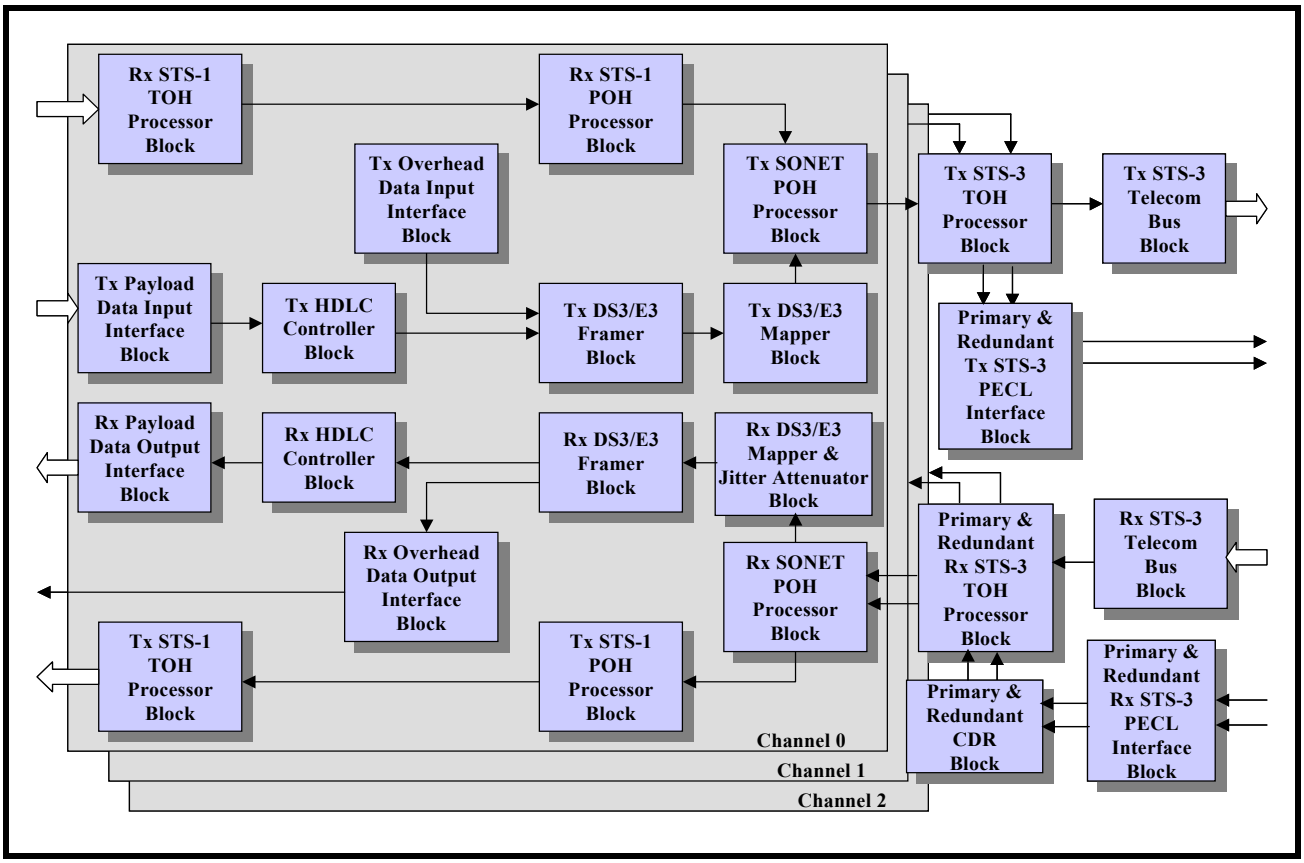
APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/ 19.44/77.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05UIpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Single PHY and Multi-PHY operations supported
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149·8-bit microprocessor interface·
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 504 Ball TBGA package

FIGURE 1. BLOCK DIAGRAM OF THE XRT94L31



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L31IB	27 x 27 504 Lead TBGA	-40°C to +85°C

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
				MICROPROCESSOR INTERFACE
Y22	PCLK	I	TTL	**Microprocessor Interface Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in one of the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in one of these modes, then it will use this clock signal to do the following.· • To sample the CS*, WR*/R/W*, A[14:0], D[7:0], RD*/DS* and DBEN input pins, and· To update the state of D[7:0] and the RDY/DTACK output signals. ***NOTES:*** *1. The Microprocessor Interface can work with mPCLK frequencies ranging up to 33MHz.* *2. This pin is inactive if the Microprocessor Interface has been configured to operate in either the Intel-Asynchronous or the Motorola-Asynchronousl Modes. In this case, tie this pin to GND.*
AD25 AD23 AC21	PTYPE_0PTYPE_1P TYPE_2	I	TTL	**Microprocessor Type Select input:** These three input pins are used to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. PTYPE[2:0] Microprocessor Interface Mode 000 Intel-Asynchronous Mode 001 Motorola - Asynchronous Mode 010 Intel X86 011 Intel I960 100 IDT3051/52 (MIPS) 101 Power PC 403 Mode 111 Motorola 860
AD27 AB25 W23 Y24 AD26 AC25 AA24 Y23 AE24 AB20 AD22 AC20 AD21 AE23 AF24	PADDR_0 PADDR_1 PADDR_2 PADDR_3 PADDR_4 PADDR_5 PADDR_6 PADDR_7 PADDR_8 PADDR_9 PADDR_10 PADDR_11 PADDR_12 PADDR_13 PADDR_14	I	TTL	**Address Bus Input pins (Microprocessor Interface):** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations (within the XRT94L31) whenever it performs READ and WRITE operations with the XRT94L31.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AD20 AC19 AE22 AG24 AE21 AD19 AF23 AE20	PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	I/O	TTL	**Bi-Directional Data Bus pins (Microprocessor Interface):** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ and WRITE operations with the Microprocessor Interface of the XRT94L31.
AF22	PWR_L/R/W*	I	TTL	**Write Strobe/Read-Write Operation Identifier:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - WR* - Write Strobe Input:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the WR* (Active-Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pins, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the target register or address location, within the XRT94L31) upon the rising of this input. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input Pin:** If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this pin is functionally equivalent to the R/W* input pin. In the Motorola Mode, a READ operation occurs if this pin is held at a logic 1, coincident to a falling edge of the RD/DS* (Data Strobe) input pin. **PowerPC 403 Mode - R/W* - Read/Write Operation Identification Input:** If the Microprocessor Interface is configured to operate in the PowerPC 403 Mode, then this input pin will function as the Read/Write Operation Identification input pin. Anytime the Microprocessor Interface samples this input signal at a logic "Low" (while also sampling the CS* input pin "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A]14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the DBEN*/OE* input pin, and the Microprocessor Interface will then place the contents of the target register (or address location within the XRT94L31) upon the Bi-Directional Dat Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic "High" (while also sampling the CS* input pin at a logic "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the RD*/DS*/WE* input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the target register or buffer location (within the XRT94L31).

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AC18	PRD_L/DS*/WE*	I	TTL	**READ Strobe /Data Strobe:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - RD* - READ Strobe Input:** If the Microprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the RD* (Active "Low" READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT94L31 will place the contents of the addressed register (or buffer location) on the Microprocessor Bi-directional Data Bus (D[7:0]). When this signal is negated, the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode - DS* - Data Strobe Input:** If the Microprocessor Interface is operating in the Motorola Asynchronous Mode, then this input will function as the DS* (Data Strobe) input signal. **PowerPC 403 Mode - WE* - Write Enable Input:** If the Microprocessor Interface is operating in the PowerPC 403 Mode, then this input pin will function as the WE* (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with CS* and WR*/R/W*) also being asserted (at a logic level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the target on-chip register or buffer location within the XRT94L31.
AG23	ALE/AS_L	I	TTL	**Address Latch Enable/Address Strobe:T** he function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - ALE** If the Microprocessor Interface (of the XRT94L31) has been configured to operate in the Intel-Asynchronous Mode, then this active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus input pins (A[14:0]) into the XRT94L31 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "High" enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT94L31 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - AS*** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this active-low input pin is used to latch the data (residing on the Address Bus, A[14:0]) into the Microprocessor Interface circuitry of the XRT94L31. Pulling this input pin "Low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **PowerPC 403 Mode - No Function - Tie to GND:** If the MIcroprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this input pin has no role nor function and should be tied to GND.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AE19	PCS_L	I	TTL	**Chip Select Input:** This active-low signal must be asserted in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT94L31 on-chip registers, LAPD and Trace Buffer locations.

AD18	PRDY_L/
	DTACK*RDY
		O	CMOS	**READY or DTACK Output:**
				The function of this input pin depends upon wich mode the Microprocessor Interface has been configured to operate in, as described below.
				Intel Asynchronous Mode - RDY* - READY output:
				If the Microprocessor Interface has been configured to operate in the Intel-Asyncrhronous Mode, then this output pin will function as the active-low READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic "Low" level ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detect this output pin being toggled to the logic "Low" level.
				Motorola Mode - DTACK* - Data Transfer Acknowledge Output:
				If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the active-low DTACK* ouytput.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic "Low" level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" leve, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic "Low" level.
				PowerPC 403 Mode - RDY - Ready Output:
				If the Microprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this output pin will function as the active-high READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic "High" level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at a logic "High" level (upon the rising edge of PCLK) then it is now safe for it to move on and execute the next READ or WRITE cycle.
				The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AF21	PDBEN_L	I	TTL	**Bi-directional Data Bus Enable Input pin:** This input pin is used to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. Setting this input pin "Low" enables the Bi-directional Data bus. Setting this input "High" tri-states the Bi-directional Data Bus.
AF20	PBLAST_L	I	TTL	**Last Burst Transfer Indicator input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. ***NOTE:*** *Connect this input pin to GND whenever the Microprocessor Interface has been configured to operate in the Intel-Async, Motorola 68K and IBM PowerPC 403 modes.*
AG22	PINT_L	O	CMOS	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Mapper/Framer device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the Interrupt Request input of the Microprocessor.
AB24	RESET_L	I	TTL	**Reset Input:** When this active-low signal is asserted, the XRT94L31 will be asynchronously reset. When this occurs, all outputs will be tri-stated and all on-chip registers will be reset to their default values.
AE18	DIRECT_ADD_SEL	I	TTL	**Address Location Select input pin:** This input pin must be pulled "High" in order to permit normal operation of the Microprocessor Interface.
SONET/SDH SERIAL LINE INTERFACE PINS				
T3	RXLDAT_P	I	LVPECL	**Receive STS-3/STM-1 Data - Positive Polarity PECL Input:** This input pin, along with RXLDAT_N functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_N functions as the Primary STS-3/STM-1 Receive Data Input Port.*
T2	RXLDAT_N	I	LVPECL	**Receive STS-3/STM-1 Data - Negative Polarity PECL Input:** This input pin, along with RXLDAT_P functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_P functions as the Primary Receive STS-3/STM-1 Data Input Port*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
U2	RXLDAT_R_P	I	LVPECL	**Receive STS-3/STM-1 Data - Positive Polarity PECL Input - Redundant Port:** This input pin, along with RXLDAT_R_N functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_R_N functions as the Redundant Receive STS-3/STM-1 Data Input Port.*
U1	RXLDAT_R_N	I	LVPECL	**Receive STS-3/STM-1 Data - Negative Polarity PECL Input - Redundant Port:** This input pin, along with RXLDAT_R_P functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_R_N functions as the Redundant Receive STS-3/STM-1 Data Input Port.*
AE27	RXCLK_19MHZ	O	CMOS	**19.44MHz Recovered Output Clock:** This pin outputs a 19.44MHz clock signal that has been derived from the incoming STS-3/STM-1 LVPECL line signal (via the Receive STS-3/STM-1 PECL Interface block) and has been extracted out and derived by Clock and Data Recovery PLL (within the Receive STS-3/STM-1 PECL Interface block). To operate the STS-3/STM-1 Interface of the XRT94L31 in the loop-timing mode, route this particular output signal through a narrow-band PLL (in order to attenuate any jitter within this signal) prior to routing it to the REFTTL input pin.
P3	REFCLK_P	I	LVPECL	**Transmit Reference Clock - Positive Polarity PECL Input:** This input pin, along with REFCLK_N and REFTTL can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If these two input pins are configured to function as the timing source, a 155.52MHz clock signal must be applied to these input pins in the form of a PECL signal. Configure these two inputs to function as the timing source by writing the appropriate data into the Transmit Line Interface Control Register (Address Location = 0x0383) ***NOTE:*** *If REFTTL clock input is used, set this pin to a logic "High"*
P2	REFCLK_N	I	LVPECL	**Transmit Reference Clock - Negative Polarity PECL Input:** This input pin, along with REFCLK_P and REFTTL can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If these two input pins are configured to function as the timing source, then the user must apply a 155.52MHz clock signal, in the form of a PECL signal to these input pins. These two inputscan be configured to function as the timing source by writing the appropriate data into the Transmit Line Interface Control Register (Address Location = 0x0383). ***NOTE:*** *Set this pin to a logic "Low" if REFTTL clock input is used*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
P5	TXLDATO_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity LVPECL Output:** This output pin, along with TXLDATO_N functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System-Board). For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_P/TXLCLKO_N. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_N functions as the Primary Transmit STS-3/STM-1 Data Output Port.*
P6	TXLDATO_N	O	LVPECL	**Transmit STS-3/STM-1 Data - Negative Polarity LVPECL Output:** This output pin, along with TXLDATO_P functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System board). For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_P/TXLCLKO_N. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_P functions as the Primary Transmit STS-3/STM-1 Data Output Port.*
M4	TXLDATO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity LVPECL Output - Redundant Port:** This output pin, along with TXLDATO_R_N functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver or to the system back-plane. For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_R_P/ TXLCLKO_R_N). ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_N functions as the Redundant Transmit STS-3/STM-4 Data Output Port.*
M3	TXLDATO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Data - Negative Polarity LVPECL Output - Redundant Port:** This output pin, along with TXLDATO_R_P functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System board). For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_R_P/ TXLCLKO_R_N).Note: ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_R_P functions as the Redundant Transmit STS-3/STM-1 Data Output Port.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
N6	TXLCLKO_P	O	LVPECL	**Transmit STS-3/STM-1 Clock - Positive Polarity PECL Output:** This output pin, along with TXLCLKO_N functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_P/TXLDATO_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_N functions as the Primary Transmit Output Clock signal.*
N5	TXLCLKO_N	O	LVPECL	**Transmit STS-3/STM-1 Clock - Negative Polarity PECL Output:** This output pin, along with TXLCLKO_P functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_P/TXLDATO_N output pins upon the falling edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_N functions as the Primary Transmit Output Clock signal.*
M1	TXLCLKO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Clock - Positive Polarity PECL Output - Redundant Port:** This output pin, along with TXLCLKO_R_N functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_R_P/TXLDATO_R_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_R_N functions as the Redundant Transmit Output Clock signal.*
M2	TXLCLKO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Clock - Negative Polarity PECL Output - Redundant Port:** This output pin, along with TXLCLKO_R_P functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_R_P/TXLDATO_R_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_R_P functions as the Redundant Transmit Output Clock signal.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
P1	REFTTL	I	TTL	**19.44MHz or 77.76MHz Clock Synthesizer Reference Clock Input Pin:** The function of this input pin depends upon whether or not the Clock Synthesizer block is enabled. **If Clock Synthesizer is Enabled.** If the Clock Synthesizer block is enabled, then it will be used to generate the 155.52MHz, 19.44MHz and/or 77.76MHz clock signal for the Transmit STS-3/STM-1 circuitry. In this mode, the user should apply a clock signal of any of the following frequencies to this input pin. • 19.44 MHz • 38.88 MHz • 51.84 MHz • 77.76 MHz Afterwards, the user needs to write the appropriate data into the Transmit Line Interface Control Register (Address Location = 0x0383) in order to (1) configure the Clock Synthesizer Block to accept any of the above-mentioned signals and generate a 155.52MHz, 19.44MHz or 77.76MHz clock signal, (2) to configure the Clock Synthesizer to function as the Clock Source for the STS-3/STM-1 block. **If Clock Synthesizer is NOT Enabled:** If the Clock Synthesizer block is NOT enabled, then it will NOT be used to generate the 19.44MHz and/or 77.76MHz clock signal, for the STS-3/STM-1 block. In this configuration seting, the user MUST apply a 19.44MHz clock signal to this input pin. ***NOTE:*** *The user must place a clock signal to this input pin in order to perform READ and WRITE operations to much of the SONET/SDH-related registers via the Microprocessor Interface.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>AG3</td><td>LOSTTL</td><td>I</td><td>TTL</td><td>
Loss of Optical Carrier Input - Primary Receive STS-3/STM-1 PECL Interface - TTL Input:
If the user is using an Optical Transceiver that contains an LOS (or Signal Detect) output that is of the CMOS/TTL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSTTL input pin to be either an active-low or an active-high signal, by pulling the LOSPECL input pin to the appropriate level as described below.
<table>
<tr><th>LOSPECL</th><th>LOSTTL Active-Low/ Active-High</th><th>Description of LOSTTL</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>
If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
• The Primary Receive STS-3 TOH Processor block will declare the Loss of Optical Carrier condition.
• The Primary Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Primary Receive STS-3 TOH Processor block to declare the LOS defect condition.
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>AG25</td><td>LOSTTL_R</td><td>I</td><td>TTL</td><td>
Loss of Optical Carrier Input - Redundant Receive STS-3/STM-1 PECL Interface - TTL Input:
If the user is using the Optical Transceiver that contains an LOS (or Signal Detect) output that is of the CMOS/TTL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSTTL_R input pin to either an active-low or an active-high signal, by pulling the LOSPECL_R input pin to the appropriate level as described below.
<table>
<tr><th>LOSPECL_R</th><th>LOSTTL_R Active-Low/ Active-High</th><th>Description of LOSTTL_R</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>
If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
The Redundant Receive STS-3 TOH Processor block wil declare the Loss of Optical Carrier condition
The Redundant Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Redundant Receive STS-3 TOH Processor block to declare the LOS defect condition.
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>L4</td><td>LOSPECL_P</td><td>I</td><td>LVPECL</td><td>
Loss of Optical Carrier/Signal Input - Single-Ended PECL Interface Input - Primary Receive STS-3/STM-1 PECL Interface:
If the user is using an Optical Transceiver that contains an LOS (or Signal Detect) output pin that is of the LVPECL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSPECL_P input pin to function as either an active-low or active-low signal by pulling the LOSTTL input pin to the appropriate level as described below.

<table>
<tr><th>LOSTTL</th><th>LOSPECL_P Active-Low/ Active-High</th><th>Description of LOSPECL_P</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>

If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
• The Primary Receive STS-3 TOH Processor block will declare the Loss of Optical Carrier condition.
• The Primary Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Primary Receive STS-3 TOH Processor block to declare the LOS defect condition.
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>L3</td><td>LOSPECL_R</td><td>I</td><td>LVPECL</td><td>
Loss of Optical Carrier/Signal Input - Single-Ended PECL Interface Input - Redundant Receive STS-3/STM-1 PECL Interface:
If the user is using an Optical Transceiver that contains an LOS (or Signal Detect) output pin that is of the LVPECL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSPECL_R input pin to function as either an active-low or active-low signal by pulling the LOSTTL input pin to the appropriate level as described below.

<table>
<tr><th>LOSTTL</th><th>LOSPECL_R Active-Low/ Active-High</th><th>Description of LOSPECL_R</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>

If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
• The Redundant Receive STS-3 TOH Processor block will declare the Loss of Optical Carrier condition.
• The Redundant Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.Note:
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Redundant Receive STS-3 TOH Processor block to declare the LOS defect condition..
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
V1	LOCKDET	O	CMOS	**Lock Detect Output Pin - Clock and Data Recovery PLL Block** This output pin indicates whether or not the Clock and data recovery PLL block has obtained lock to incoming STS-3/STM-1 signal. As the Receive STS-3/STM-1 PECL Interface block receives this STS-3/STM-1 signal, the CDR (Clock and Data Recovery) PLL will attempt to lock onto this STS-3/STM-1 PECL signal. The Receive STS-3/STM-1 PECL Interface block will (internally) derive a 19.44MHz clock signal from this incoming STS-3/STM-1 PECL signal. The CDR PLL will then continuously compare the frequency of this 19.44MHz clock signal, with that derived from either the Clock Synthesizer block (or from the 19.44MHz clock signal applied to the REFTTL input pin). If the CDR PLL determines that the frequency difference between these two signals is less than 0.05%, then it will declare that the CDR PLL is in Lock. If the CDR PLL determines that the frequency difference between these two signals is greater than 0.05%, then it will declare the the CDR PLL is Out of Lock. 0 - Indicates that the CDR PLL (within the Receive STS-3/STM-1 PECL Interface Block) is declaring the Lock Condition. 1 - Indicates that the CDR PLL is declaring the Out of Lock Condition.
STS-3/STM-1 TELECOM BUS INTERFACE - TRANSMIT DIRECTION				
E1	TXA_CLK	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Clock Output Signal:** This output clock signal functions as the clock source for the Transmit STS-3/STM-1 Telecom Bus Interface. All signals, that are output via the Transmit STS-3/STM-1 Telecom Bus Interface (e.g., TXA_C1J1, TXA_ALARM, TXA_DP, TXA_PL and TXA_D[7:0]) are updated upon the rising edge of this clock signal. This clock signal operates at 19.44MHz and is derived from the Clock Synthesizer block.
F2	TXA_C1J1whether or not the	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Output Signal:** This output pin pulses "High" under the following two conditions; • Coincident to whenever the C1/J0 byte (of the outbound STS-3/STM-1 signal) is being output via the TxA_D[7:0] output, and • Coincident to whenever the J1 byte(s) (of the outbound STS-3/STS-3c/STM-1 signal) is being output via the TxA_D[7:0] output. ***NOTES:*** *1. The Transmit STS-3/STM-1 Telecom Bus Interface will indicate that it is currently transmitting the C1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "High" (for one period of TXA_CLK) and keeping the TXA_PL output pin pulled "Low".* *2. The Transmit STS-3/STM-1 Telecom Bus will indicate that it is currently transmitting the J1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "High" (for one period of TXA_CLK) while the TXA_PL output pin is pulled "High".* *3. This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface block is enabled and is configured to operate in the Re-Phase OFF Mode.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E2	TXA_ALARM	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus - Alarm Indicator Output signal:** This output pin pulses "High", coincdent to the instant that the Transmit STS-3/STM-1 Telecom Bus outputs a byte (via the TxA_D[7:0] output pins) that pertains to any that STS-1 or STS-3c signal is carrying the AIS-P indicator. This output pin is "Low" for all other conditions. ***NOTE:*** *This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface is enabled and has been configured to operate in the Re-Phase OFF Mode.*
H3	TXA_DP	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus - Parity Output pin:** This output pin can be configured to function as one of the following.To reflect either the EVEN or ODD parity value of the bits which are currently being output via the TXA_D[7:0] output pins. To reflect either the EVEN or ODD parity value of the bits which are currently being output via the TXA_D[7:0] output pins and the states of the TXA_PL and TXA_C1J1 output pins. ***NOTE:*** *Any one of these configuration selections can be made by writing the appropriate value into the Telecom Bus Control Register (Address Location = 0x0137).*
G4	TxSBFP	I	TTL	**Transmit STS-3/STM-1 Frame Alignment Sync Input:** The Transmit STS-3 TOH Processor Block can be configured to initiate its generation of a new outbound STS-3/STM-1 frame based upon an externally supplied 8kHz clock signal to this input pin. If this feature is used, the Transmit STS-3/STM-1 Telecom Bus Interface will begin transmitting the very first byte of given STS-3 or STM-1 frame, upon sensing a rising edge (of the 8kHz signal) at this input pin. ***NOTES:*** 1. *If this input pin is connected to GND, then the Transmit STS-3 TOH Processor block will generate its outbound STS-3/STM-1 frames asynchronously, with respect to any input signal.* 2. *This input signal must be synchronized with the signal that is supplied to the REFTTL input pin. Failure to insure this will result in bit errors being generated within the outbound STS-3/STM-1 signal.* 3. *The user must supply an 8kHz pulse (to this input pin) that has a width of approximately 51.4412.8ns (one 19.44MHz clock period). The user must not apply a 50% duty cycle 8kHz signal to this input pin.* 4. *Register HRSYNC_DLY (Address Location: 0x0135) defines the timing for TxSBFP input pin.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
K5	TxA_PL	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Payload Data Indicator Output Signal:** This output pin indicates whether or not the Transmit STS-3/STM-1 Telecom Bus Interface is currently placing a Transport Overhead byte or a non-Transport Overhead Byte (e.g., STS-1 SPE, STS-3c SPE, VC-3 or VC-4 data) via the TXA_D[7:0] output pins. This output pin is pulled "Low" for the duration that the Transmit STS-3/STM-1 Telecom Bus Interface is transmitting a Transport Overhead byte via the TXA_D[7:0] output pins. Conversely, this output pin is pulled "High" for the duration that the Transmit STS-3/STM-1 Telecom Bus Interface is transmitting something other than a Transport Overhead byte via the TXA_D[7:0] output pins.
J4 G3 D1 F3 J5 H4 D2 E3	TxA_D0 TxA_D1 TxA_D2 TxA_D3 TxA_D4 TxA_D5 TxA_D6 TxA_D7	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Transmit Output Data Bus pins:** These 8 output pins function as the Transmit STS-3/STM-1 Telecom Bus Interface - Output data bus. If the STS-3/STM-1 Telecom Bus Interface is enabled, then all outbound STS-3/STM-1 data is output via these pins (in a byte-wide manner), upon the rising edge of the TXA_CLK output pin.
STS-3/STM-1 TELECOM BUS INTERFACE - RECEIVE DIRECTION				
W2	RxD_CLK	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Clock Input Signal:** This input clock signal functions as the clock source for the Receive STS-3/STM-1 Telecom Bus Interface. All input signals are sampled upon the falling edge of this input clock signal. This clock signal should operate at 19.44MHz.Note: ***NOTE:*** *This input pin is only used if the STS-3/STM-1 Telecom Bus has been enabled. It should be connected to GND otherwise.*
AA3	RxD_PL	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Payload Data Indicator Output Signal:** This input pin indicates whether or not the Receive STS-3/STM-1 Telecom Bus Interface is currently receiving Transport Overhead bytes or non-Transport Overhead bytes (e.g., STS-1 SPE, STS-3c SPE,VC-3 or VC-4 data) via the RXD_D[7:0] input pins. This input pin should be pulled "Low" for the duration that the Receive STS-3/STM-1 Telecom Bus Interface is receiving a Transport Overhead byte via the RXD_D[7:0] input pins. Conversely, this input pin should be pulled "High" for the duration that the Receive STS-3/STM-1 Telecom Bus Interface is receiving something other than a Transport Overhead byte via the RXD_D[7:0] input pins. ***NOTE:*** *Connect this pin to GND if the STS-3/STM-1 Telecom Bus is NOT enabled*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AD1	RxD_C1J1	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Input Signal:** This input pin should be pulsed "High" during both of the following conditions. a. Coincident to whenever the C1/J0 byte (within the incoming STS-3/STM-1 signal) is being applied to the Receive STS-3/STM-1 Telecom Bus - Data Input pins (RXD_D[7:0]). b. Coincident to whenever the J1 byte(s) (within the incoming STS-3/STM-1 signal) is being applied to the Receive STS-3/STM-1 Telecom Bus - Data Input pins (RXD_D[7:0]) input. ***NOTE:*** *This input pin should be pulled "Low" during all other times.*
AB3	RxD_DP	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Parity Input pin:** This input pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits (within the incoming STS-3/STM-1 signal) which are currently being input via the RXD_D[7:0] input pins. The EVEN or ODD parity value of the bits (within the incoming STS-3/STM-1 signal) which are being input via the RXD_D[7:0] input and the states of the RXD_PL and RXD_C1J1 input pins. The Receive STS-3/STM-1 Telecom Bus Interface block will use this input signal to compute and verify the Parity of each byte within the incoming STS-3/STM-1 data-stream. ***NOTES:*** 1. *Any one of these configuration selections can be made by writing the appropriate value into the Telecom Bus Control register (Address Location = 0x0137).* 2. *Tie this input pin to GND if the STS-3/STM-1 Telecom Bus Interface is disabled.*
W1	RxD_ALARM	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Alarm Indicator Input:** This input pin should be pulsed "High" for one RxD_CLK period coincident to whenever the Receive STS-3/STM-1 Telecom Bus Interface is accepting a byte from an incoming STS-1 or STS-3c signal (via the RxD_D[7:0] input pins) that is carrying the AIS-P indicator. This input pin should be held at a logic "Low" at all other times. ***NOTES:*** 1. *If the RxD_ALARM input signal pulses "High" for any given STS-1 signal (within the incoming STS-3), the XRT94L31 will automatically declare the AIS-P defect condition for that STS-1 or STS-3c channel.* 2. *Tie this input pin to GND, if the STS-3/STM-1 Telecom Bus Interface is disabled.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
Y2 AD2 AC3 AA4A B4 Y1 AD3 AA5	RxD_D0 RxD_D1 RxD_D2 RxD_D3 RxD_D4 RxD_D5 RxD_D6 RxD_D7	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Receive Input Data Bus pins:** These 8 input pins function as the Receive STS-3/STM-1 Telecom Bus Interface Receive Input data bus. All STS-3/STM-1 data is sampled and latched (into the XRT94L31, via these input pins) upon the falling edge of the RXA_CLK input pin. ***NOTE:*** *These input pins are only active if the Receive STS-3/STM-1 Telecom Bus Interface has been enabled. If the XRT94L31 is configured to exchange STS-3/STM-1 data via the PECL Interface (instead), tie these pins to GND.*
SONET/SDH OVERHEAD INTERFACE - TRANSMIT DIRECTION				
H6	TxTOHClk	O	CMOS	**Transmit TOH Input Port - Clock Output:** This output pin, along with the TxTOHEnable, TxTOHFrame output pins and the TxTOH and TxTOHIns input pins function as the Transmit TOH Input Port.The Transmit TOH Input Port is usedr to insert the users own value for the TOH bytes (in the outbound STS-3/STM-1 signal). This output pin provides the user with a clock signal. If the TxTOHEnable output pin is "High" and if the TxTOHIns input pin is pulled "High", then the user is expected to provide a given bit (within the TOH) to the TxTOH input pin, upon the falling edge of this clock signal. The data, residing on the TxTOH input pin will be latched into the XRT94L31 upon the rising edge of this clock signal. The XRT94L31 will then insert this particular TOH bit value into the appropriate TOH bit positions within the outbound STS-3 data-stream. ***NOTE:*** *The Transmit TOH Input Port only supports the insertion of the TOH within the first STS-1, within the outbound STS-3 signal.*
G5	TxTOHEnable	O	CMOS	**Transmit TOH Input Port - TOH Enable (or READY) indicator:** This output pin, along with the TxTOHClk, TxTOHFrame output pins and the TxTOH and TxTOHIns input pins function as the Transmit TOH Input Port. This output pin will toggle and remain "High" anytime the Transmit TOH Input Port is ready to externally accept TOH data. To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHFrame and this output pin upon the rising edge of TxTOHClk. • Whenever this output pin pulses "High", then the user's external circuitry should drive the TxTOHIns input pin "High". • Next, output the next TOH bit, onto the TxTOH input pin, upon the rising edge of TxTOHClk

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
F8	TxTOH	I	TTL	**Transmit TOH Input Port - Input pin:** This input pin, along with the TxTOHIns input pin, the TxTOHEnable and TxTOHFrame and TxTOHClk output pins function as the Transmit TOH Input Port.To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHFrame and TxTOHEnable upon the rising edge of TxTOHClk • Whenever TxTOHEnable pulses "High", then the user's external circuitry should drive the TxTOHIns input pin "High" • Next, output the next TOH bit, onto this input pin, upon the rising edge of TxTOHClk. The Transmit TOH Input Port will sample the data (on this input pin) upon the falling edge of TxTOHClk. ***NOTE:*** *Data at this input pin will be ignored (e.g., not sampled) unless the TxTOHEnable output pin is "High" and the TxTOHIns input pin is pulled "High".*
E8	TxTOHFrame	O	CMOS	**Transmit TOH Input Port - STS-3/STM-1 Frame Indicator:** This output pin, along with TxTOHClk, TxTOHEnable output pins, and the TxTOH and TxTOHIns input pins function as the Transmit TOH Input Port.This output pin will pulse "High" (for one period of TxTOHClk), one TxTOHClk clock period prior to the first TOH bit of a given STS-3 frame, being expected via the TxTOH input pin.To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHEnable and this output pin upon the rising edge of TxTOHClk. • Whenever the TxTOHEnable output pin pulse "High", then the user's external circuitry should drive the TxTOHIns input pin "High". • Next, output the next TOH bit, onto the TxTOH input pin, upon the rising edge of TxTOHClk. ***NOTE:*** *The external circuitry (which is being interfaced to the Transmit TOH Input Port can use this particular output pin to denote the boundary of STS-3 frames.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D6	TxTOHIns	I	TTL	**Transmit TOH Input Port - Insert Enable Input pin:** This input pin, along with the TxTOH input pin, and the TxTOHEnable, TxTOHFrame and TxTOHClk output pins function as the Transmit TOH Input Port. This input pin is used to either enable or disable the Transmit TOH Input Port. If this input pin is "Low", then the Transmit TOH Input Port will be disabled and will not sample and insert (into the outbound STS-3 data stream) any data residing on the TxTOH input, upon the rising edge of TxTOHClk. If this input pin is "High", then the Transmit TOH Input Port will be enabled. In this mode, whenever the TxTOHEnable output pin is also "High", the Transmit TOH Input Port will sample and latch any data that is presented on the TxTOH input pin, upon the rising edge of TxTOHClk. To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHFrame and TxTOHEnable upon the rising edge of TxTOHClk. • Whenever the TxTOHEnable output pin is sampled "High" then the user's external circuitry should drive this input pin "High". • Next, output the next TOH bit, onto the TxTOH input pin, upon the falling edge of TxTOHClk. The Transmit TOH Input Port will sample the data (on this input pin) upon the falling edge of TxTOHClk.] ***NOTES:*** *1. Data applied to the TxTOH input pin will be sampled according to the following insertion priority scheme:* *2. For DCC, E1, F1, E2 bytes, TxTOH input pin will be sampled if both TxTOHEnable and TxTOHIns are "High".* *3. For other TOH bytes, TxTOH input pin will be sampled if both TxTOHEnable and TxTOHIns are "High" or if both TxTOHIns and Software Insertion Enabled are "Low".*
B4	TxLDCCEnable	O	CMOS	**Transmit - Line DCC Input Port - Enable Output pin:** This output pin, along with the TxTOHClk output pin and the TxLDCC input pin are used to insert their value for the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D4, D5, D6, D7, D8, D9, D10, D11 and D12 byte-fields, within the outbound STS-3 data-stream. The Line DCC HDLC Controller circuitry (which is connected to the TxTOHClk, the TxSDCC and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "High", then the Line DCC HDLC Controller circuitry should place the next Line DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxLDCC input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxLDCC input pin, will be sampled upon the falling edge of TxOHClk.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D7	TxSDCCEnable	O	CMOS	**Transmit - Section DCC Input Port - Enable Output pin:** This output pin, along with the TxTOHClk output pin and the TxSDCC input pin is used to insert their value for the D1, D2 and D3 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D1, D2 and D3 byte-fields, within the outbound STS-3 data-stream. The Section DCC HDLC Controller circuitry (which is connected to the TxTOHClk, the TxSDCC and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "High", then the Section DCC HDLC Controller circuitry should place the next Section DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxSDCC input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxSDCC input pin, will be sampled upon the falling edge of TxOHClk.
C5	TxSDCC	I	TTL	**Transmit - Section DCC Input Port - Input pin:** This input pin, along with the TxSDCCEnable and the TxTOHClk output pins is used to insert their value for the D1, D2 and D3 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the D1, D2 and D3 byte fields, within the outbound STS-3 data-stream. The Section DCC HDLC Circuitry that is interfaced to this input pin, the TxSDCCEnable and the TxTOHClk pins is suppose to do the following. It should continuously monitor the state of the TxSDCCEnable input pin. Whenever the TxSDCCEnable input pin pulses "High", then the Section DCC HDLC Controller circuitry should place the next Section DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto this input pin upon the rising edge of TxTOHClk. Any data that is placed on the TxSDCC input pin, will be sampled upon the falling edge of TxTOHClk.Note: ***NOTE:*** *This pin should be connected to GND if it is not used.*
D8	TxLDCC	I	TTL	**Transmit - Line DCC Input Port:** This input pin, along with the TxLDCCEnable and the TxTOHClk pins is used to insert their value for the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the D4, D5, D6, D7, D8, D9, D10, D11 and D12 byte-fields, within the outbound STS-3 data-stream. Whatever Line DCC HDLC Controller Circuitry is interface to the this input pin, the TxLDCCEnable and the TxTOHClk is suppose to do the following. It should continuously monitor the state of the TxLDCCEnable input pin. Whenever the TxLDCCEnable input pin pulses "High", then the Section DCC Interface circuitry should place the next Line DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxLDCC input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxLDCC input pin, will be sampled upon the falling edge of TxTOHClk.Note: ***NOTE:*** *This pin should be connected to GND if it is not used.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E9	TxE1F1E2Enable	O	CMOS	**Transmit E1-F1-E2 Byte Input Port - Enable (or Ready) Indicator Output pin:** This output pin, along with the TxTOHClk output pin and the TxE1F1E2 input pin is used to insert their value for the E1, F1 and E2 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the E1, F1 and E2 byte-fields, within the outbound STS-3 data-stream. Whatever external circuitry (which is connected to the TxTOHClk, the TxE1F1E2 and this output pin), is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "High", then the external circuitry should place the next orderwire bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxE1F1E2 input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxE1F1E2 input pin, will be sampled upon the falling edge of TxOHClk.
C6	TxE1F1E2Frame	O	CMOS	**Transmit E1-F1-E2 Byte Input Port - Framing Output Pin.** This output pin pulses "High" for one period of TxTOHClk, one TxTOHClk bit-period prior to the Transmit E1-F1-E2 Byte Input Port expecting the very first byte of the E1 byte, within a given outbound STS-3 frame.
A4	TxE1F1E2	I	TTL	**Transmit E1-F1-E2 Byte Input Port - Input Pin:** This input pin, along with the TxE1F1E2Enable and the TxTOHClk output pins are used to insert their value for the E1, F1 and E2 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the E1, F1 and E2 byte fields, within the outbound STS-3 data-stream. Whatever external circuitry that is interfaced to this input pin, the TxE1F1E2Enable and the TxTOHClk pins is suppose to do the following. It should continuously monitor the state of the TxE1F1E2Enable input pin. Whenever the TxE1F1E2Enable input pin pulses "High", then the external circuitry should place the next orderwire bit (to be inserted into the Transmit STS-3 TOH Processor block) onto this input pin upon the rising edge of TxTOHClk. Any data that is placed on the TxE1F1E2 input pin, will be sampled upon the falling edge of TxTOHClk.Note: ***NOTE:*** *This pin should be connected to GND if it is not used.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C7	TXPOH	I	TTL	**Transmit Path Overhead Input Port - Input pin.** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used.This input pin is used to insert the POH data into the Transmit AU-4/VC-4 Mapper POH Processor blocks for insertion and transmission via the outbound STS-3 signal.In this mode, the external circuitry (which is being interfaced to the Transmit Path Overhead Input Port is suppose to monitor the following output pins; • TxPOHFrame_n • TxPOHEnable_n • TxPOHClk_n The TxPOHFrame_n output pin will toggle "High" upon the rising edge of TxPOHClk_n approximately one TxPOHClk_n period prior to the TxPOH port being ready to accept and process the first bit within J1 byte (e.g., the first POH byte). The TxPOHFrame_n output pin will remain "High" for eight consecutive TxPOHClk_n periods. The external circuitry should use this pin to note STS-1 SPE frame boundaries. The TxPOHEnable_n output pin will toggle "High" upon the rising edge of TxPOHClk_n approximately one TxPOHClk_n period prior to the TxPOH port being ready to accept and process the first bit within a given POH byte. To externally insert a given POH byte: a. assert the TxPOHIns_n input pin by toggling it "High", and b. place the value of the first bit (within this particular POH byte) on this input pin upon the very next rising edge of TxPOHClk_n. This data bit will be sampled upon the very next falling edge of TxPOHClk_n. The external circuitry should continue to keep the TxPOHIns_n input pin "High" and advancing the next bits (within the POH bytes) upon each rising edge of TxPOHClk_n.
D9	TXPOHCLK	O	TTL	**Transmit Path Overhead Input Port - Clock Output pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. This output pin, along with TxPOH, TxPOHEnable, TxPOHIns and TxPOHFrame function as the Transmit Path Overhead (TxPOH) Input Port. The TxPOHFrame and TxPOHEnable output pins are updated upon the falling edge this clock output signal. The TxPOHIns input pins and the data residing on the TxPOH input pins are sampled upon the next falling edge of this clock signal.
B5	TXPOHFRAME	O	TTL	Transmit Path Overhead Input Port - Frame Output pin: This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. This output pin, along with the TxPOH, TxPOHEnable, TxPOHIns and TxPOHClk function as the Transmit Path Overhead Input Port.If the user is only inserting POH data via these input pins: ***NOTE:*** *In this mode, the TxPOH port will pulse these output pins "High" whenever it is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port.*