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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER IC DATA SHEET

N0VEMBER 2006 *REV.1.2.0.*

GENERAL DESCRIPTION

The XRT94L33 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L33 interfaces directly to the optical transceiver

The XRT94L33 processes the section, line and path overhead in the SONET/SDH data stream and also performs ATM and PPP PHY-layer processing. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L33 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L33 memory map or from external interface. A1, A2 framing pattern, C1 byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L33 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L33 provides 3 mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

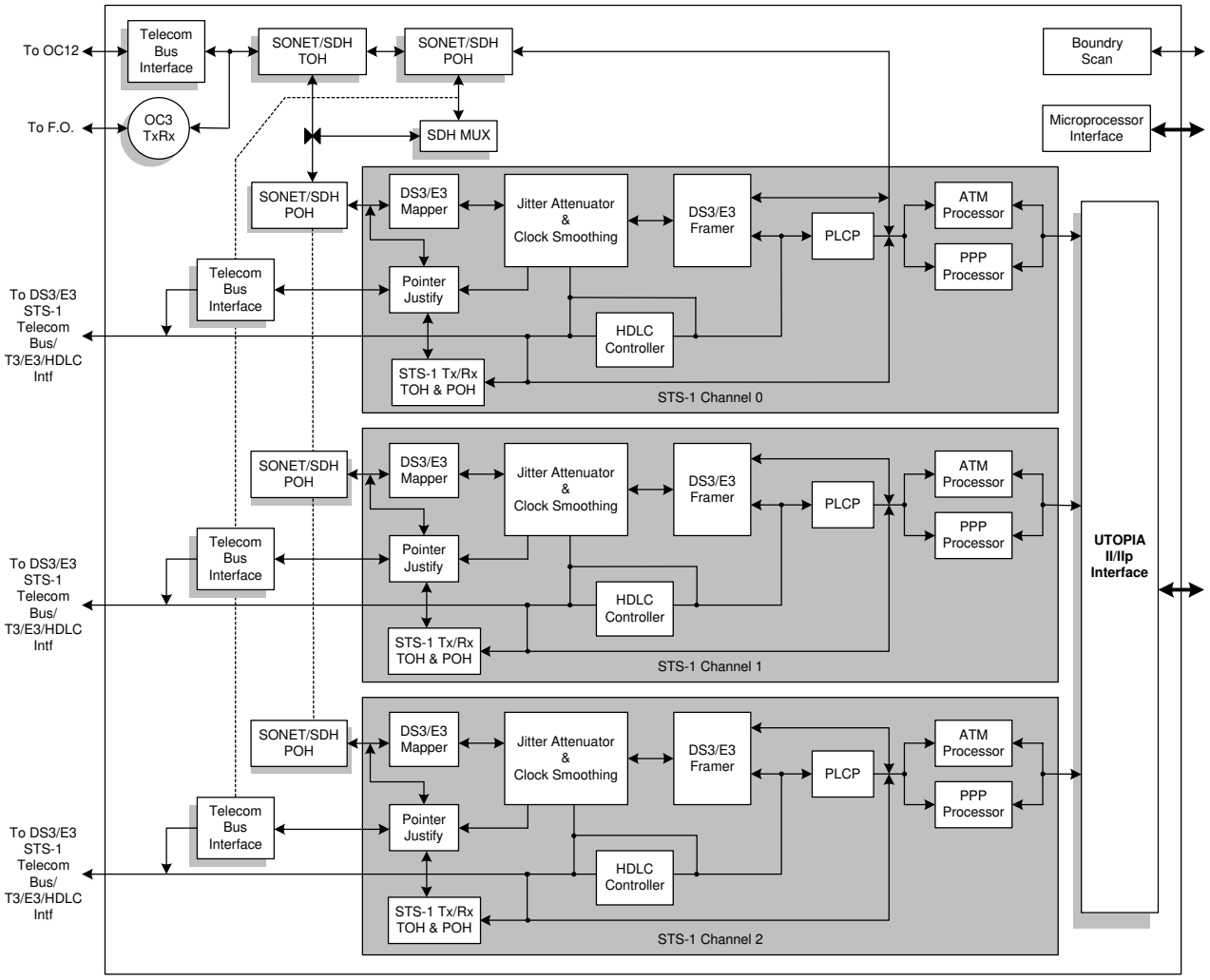
APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/19.44/77.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05UIpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- UTOPIA Level 2 interface for ATM or level 2P for Packets
- E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Single PHY and Multi-PHY operations supported
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149
- 8-bit microprocessor interface
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 504 Ball TBGA package

Block Diagram of the XRT94L33



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L33IB	27 x 27 504 Lead TBGA	-40°C to +85°C

PIN DESCRIPTION of the XRT94L33 (Rev. B)

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
				MICROPROCESSOR INTERFACE
Y22	PCLK	I	TTL	**Microprocessor Interface Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in one of the Synchronous Mode (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in one of these modes, then it will use this clock signal to do the following. • To sample the CS*, WR*/R/W*, A[14:0], D[7:0], RD*/DS* and DBEN input pins, and • To update the state of D[7:0] and the RDY/DTACK output signals. ***NOTES:*** 1. The Microprocessor Interface can work with μPCLK frequencies ranging up to 33MHz. 2. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronousl Modes. In this case, the user should tie this pin to GND.
AD25 AD23 AC21	PTYPE_0 PTYPE_1 PTYPE_2	I	TTL	**Microprocessor Type Select input:** These three input pins permit the user to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. **PTYPE[2:0] Microprocessor Interface Mode** 000 Intel-Asynchronous Mode 001 Motorola – Asynchronous Mode 010 Intel X86 011 Intel I960 100 IDT3051/52 (MIPS) 101 Power PC 403 Mode 111 Motorola 860

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AD27 AB25 W23 Y24 AD26 AC25 AA24 Y23 AE24 AB20 AD22 AC20 AD21 AE23 AF24	PADDR_0 PADDR_1 PADDR_2 PADDR_3 PADDR_4 PADDR_5 PADDR_6 PADDR_7 PADDR_8 PADDR_9 PADDR_10 PADDR_11 PADDR_12 PADDR_13 PADDR_14	I	TTL	**Address Bus Input pins (Microprocessor Interface):** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations (within the XRT94L33) whenever it performs READ and WRITE operations with the XRT94L33.
AD20 AC19 AE22 AG24 AE21 AD19 AF23 AE20	PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	I/O	TTL	**Bi-Directional Data Bus pins (Microprocessor Interface):** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ and WRITE operations with the Microprocessor Interface of the XRT94L33.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AF22	PWR_L/ R/W*	I	TTL	**Write Strobe/Read-Write Operation Identifier:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode – WR* - Write Strobe Input:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the WR* (Active-Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pins, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT94L33) upon the rising of this input. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input Pin:** If the Microprocessor Interface is operating in the "Motorola-Asynchronous" Mode, then this pin is functionally equivalent to the "R/W*" input pin. In the Motorola Mode, a "READ" operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. **PowerPC 403 Mode – R/W* - Read/Write Operation Identification Input:** If the Microprocessor Interface is configured to operate in the PowerPC 403 Mode, then this input pin will function as the "Read/Write Operation Identification" input pin. Anytime the Microprocessor Interface samples this input signal at a logic "low" (while also sampling the CS* input pin "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A]14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the DBEN*/OE* input pin, and the Microprocessor Interface will then place the contents of the "target" register (or address location within the XRT94L33) upon the Bi-Directional Dat Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic high (while also sampling the CS* input pin at a logic "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the RD*/DS*/WE* input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the "target" register or buffer location (within the XRT94L33).

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AC18	PRD_L/ DS*/ WE*	I	TTL	**READ Strobe /Data Strobe:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode – RD* - READ Strobe Input:** If the Microprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the RD* (Active Low READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT94L33 will place the contents of the addressed register (or buffer location) on the Microprocessor Bi-directional Data Bus (D[7:0]). When this signal is negated, the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode – DS* - Data Strobe Input:** If the Microprocessor Interface is operating in the Motorola Asynchronous Mode, then this input will function as the DS* (Data Strobe) input signal. **PowerPC 403 Mode – WE* - Write Enable Input:** If the Microprocessor Interface is operating in the PowerPC 403 Mode, then this input pin will function as the WE* (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with CS* and WR*/R/W*) also being asserted (at a logic level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the “target” on-chip register or buffer location within the XRT94L33.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AG23	ALE/ AS_L	I	TTL	**Address Latch Enable/Address Strobe:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - ALE** If the Microprocessor Interface (of the XRT94L33) has been configured to operate in the Intel-Asynchronous Mode, then this active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus input pins (A[14:0]) into the XRT94L33 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "high" enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT94L33 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode – AS*** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this active-low input pin is used to latch the data (residing on the Address Bus, A[14:0]) into the Microprocessor Interface circuitry of the XRT94L33. Pulling this input pin "low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **PowerPC 403 Mode – No Function – Tie to GND**: If the MIcroprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this input pin has no role nor function and should be tied to GND.
AE19	PCS_L	I	TTL	**Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT94L33 on-chip registers, LAPD and Trace Buffer locations.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION

AD18	PRDY_L/
	DTACK*
	RDY
		O	CMOS	**READY or DTACK Output:**
				
				The exact function of this input pin depends upon wich mode the Microprocessor Interface has been configured to operate in, as described below.
				
				Intel Asynchronous Mode – RDY* - READY output:
				
				If the Microprocessor Interface has been configured to operate in the Intel-Asyncrhronous Mode, then this output pin will function as the “active-low” READY output.
				
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic “low” level ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detect this output pin being toggled to the logic low level.
				
				Motorola Mode – DTACK* - Data Transfer Acknowledge Output:
				
				If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the “active-low” DTACK* ouytput.
				
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” leve, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				
				PowerPC 403 Mode – RDY – Ready Output:
				
				If the Microprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this output pin will function as the “active-high” READY output.
				
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at a logic “high” level (upon the rising edge of PCLK) then it is now safe for it to move on and execute the next READ or WRITE cycle.
				
				The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AF21	PDBEN_L	I	TTL	**Bi-directional Data Bus Enable Input pin:** This input pin permits the user to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. Setting this input pin "low" enables the Bi-directional Data bus. Setting this input "high" tri-states the Bi-directional Data Bus.
AF20	PBLAST_L	I	TTL	**Last Burst Transfer Indicator input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. ***Note:*** *The user should connect this input pin to GND whenever the Microprocessor Interface has been configured to operate in the Intel-Async, Motorola 68K and IBM PowerPC 403 modes.*
AG22	PINT_L	O	CMOS	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Mapper/Framer device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the Microprocessor.
AB24	RESET_L	I	TTL	**Reset Input:** When this "active-low" signal is asserted, the XRT94L33 will be asynchronously reset. When this occurs, all outputs will be "tri-stated" and all on-chip registers will be reset to their "default" values.
AE18	DIRECT_ADD_SEL	I	TTL	**Address Location Select input pin:** This input pin must be pulled "HIGH" in order to permit normal operation of the Microprocessor Interface.
SONET/SDH SERIAL LINE INTERFACE PINS				
T3	RXLDAT_P	I	LVPECL	**Receive STS-3/STM-1 Data – Positive Polarity PECL Input:** This input pin, along with RXLDAT_N functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_N" functions as the "Primary" STS-3/STM-1 Receive Data Input Port.*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
T2	RXLDAT_N	I	LVPECL	**Receive STS-3/STM-1 Data – Negative Polarity PECL Input:** This input pin, along with RXLDAT_P functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_P" functions as the "Primary Receive STS-3/STM-1 Data Input Port"*
U2	RXLDAT_R_P	I	LVPECL	**Receive STS-3/STM-1 Data – Positive Polarity PECL Input – Redundant Port:** This input pin, along with "RXLDAT_R_N" functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_R_N" functions as the "Redundant Receive STS-3/STM-1 Data Input Port".*
U1	RXLDAT_R_N	I	LVPECL	**Receive STS-3/STM-1 Data – Negative Polarity PECL Input – Redundant Port:** This input pin, along with "RXLDAT_R_P" functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_R_N" functions as the "Redundant Receive STS-3/STM-1 Data Input Port".*
AE27	RXCLK_19MHZ	O	CMOS	**19.44MHz Recovered Output Clock:** This pin outputs a 19.44MHz clock signal that has been derived from the incoming STS-3/STM-1 line signal (via the Receive STS-3/STM-1 Clock and Data Recovery PLL). If the user wishes to operate the STS-3/STM-1 Interface in the "loop-timing" mode, then the user should route this particular signal through a "narrow-band" PLL (in order to attenuate any jitter within this signal) prior to routing it to the REFTTL input pin.
P3	REFCLK_P	I	LVPECL	**Transmit Reference Clock – Positive Polarity PECL Input:** This input pin, along with "REFCLK_N" and "REFTTL" can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If the user configures these two input pins to function as the timing source, then the user must apply a 155.52MHz clock signal, in the form of a PECL signal to these input pins. The user can configure these two inputs to function as the timing source by writing the appropriate data into the "Transmit Line Interface Control Register " (Address Location = 0x0383) ***Note:*** *Users should set this pin to "1" if "REFTTL" clock input is used*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
P2	REFCLK_N	I	LVPECL	**Transmit Reference Clock – Negative Polarity PECL Input:** This input pin, along with "REFCLK_P" and "REFTTL" can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If the user configures these two input pins to function as the timing source, then the user must apply a 155.52MHz clock signal, in the form of a PECL signal to these input pins. The user can configure these two inputs to function as the timing source by writing the appropriate data into the "Transmit Line Interface Control Register " (Address Location = 0x0383) ***Note:*** *Users should set this pin to "0" if "REFTTL" clock input is used*
P5	TXLDATO_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity PECL Output:** This output pin, along with TXLDATO_N functions as the Transmit Data Output, to the Optical Transceiver or to the system back-plane. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXLCLKO_P/TXLCLKO_N". ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_N" functions as the "Primary" Transmit STS-3/STM-1 Data Output Port.*
P6	TXLDATO_N	O	LVPECL	**Transmit STS-3/STM-1 Data – Negative Polarity PECL Output:** This output pin, along with TXLDATO_P functions as the Transmit Data Output, to the Optical Transceiver or to the system back-plane. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of TXLCLKO_P/TXLCLKO_N. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_P" functions as the "Primary" Transmit STS-3/STM-1 Data Output Port.*
M4	TXLDATO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity PECL Output - Redundant Port:** This output pin, along with TXLDATO_R_N functions as the Transmit Data Output, to the Optical Transceiver or to the system back-plane. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXLCLKO_R_P/TXLCLKO_R_N"). ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_N" functions as the "Redundant" Transmit STS-3/STM-4 Data Output Port.*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
M3	TXLDATO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Data - Negative Polarity PECL Output - Redundant Port:** This output pin, along with TXLDATO_R_P functions as the Transmit Data Output, to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System board) For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXLCLKO_R_P/TXLCLKO_R_N"). ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_R_P" functions as the "Redundant" Transmit STS-3/STM-1 Data Output Port.*
N6	TXLCLKO_P	O	LVPECL	**Transmit STS-3/STM-1 Clock – Positive Polarity PECL Output:** This output pin, along with TXLCLKO_N functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_P/TXLDATO_N" output pins upon the rising edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_N" functions as the "Primary Transmit Output Clock" signal.*
N5	TXLCLKO_N	O	LVPECL	**Transmit STS-3/STM-1 Clock – Negative Polarity PECL Output:** This output pin, along with TXLCLKO_P functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_P/TXLDATO_N" output pins upon the falling edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_N" functions as the "Primary Transmit Output Clock" signal.*
M1	TXLCLKO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Clock – Positive Polarity PECL Output – Redundant Port:** This output pin, along with TXLCLKO_R_N functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_R_P/TXLDATO_R_N" output pins upon the rising edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_R_N" functions as the "Redundant Transmit Output Clock" signal.*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
M2	TXLCLKO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Clock – Negative Polarity PECL Output – Redundant Port:** This output pin, along with TXLCLKO_R_P functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_R_P/TXLDATO_R_N" output pins upon the rising edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_R_P" functions as the "Redundant Transmit Output Clock" signal.*
P1	REFTTL	I	TTL	**19.44MHz or 77.76MHz Clock Synthesizer Reference Clock Input Pin:** The exact function of this input pin depends upon whether the user enables the "Clock Synthesizer" block or not. **If Clock Synthesizer is Enabled.** If the "Clock Synthesizer" block is enabled, then it will be used to generate the 155.52MHz, 19.44MHz and/or 77.76MHz clock signal for the STS-3/STM-1 block. In this mode, the user should apply a clock signal of either of the following frequencies to this input pin. • 19.44 MHz • 38.88 MHz • 51.84 MHz • 77.76 MHz Afterwards, the user needs to write the appropriate data into the "Transmit Line Interface Control Register" (Address Location = 0x0383) in order to (1) configure the Clock Synthesizer Block to accept any of the above-mentioned signals and generate a 155.52MHz, 19.44MHz or 77.76MHz clock signal, (2) to configure the Clock Synthesizer to function as the Clock Source for the STS-3/STM-1 block. **If Clock Synthesizer is NOT Enabled:** If the "Clock Synthesizer" block is NOT enabled, then it will NOT be used to generate the 19.44MHz and/or 77.76MHz clock signal, for the STS-3/STM-1 block. In this configuration seting, the user MUST apply a 19.44MHz clock signal to this input pin.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AG3	LOSTTL	I	TTL	**Loss of Optical Carrier Input – Primary:** The user is expected to connect the "Loss of Carrier" output (from the Optical Transceiver) to this input pin. If this input pin and the LOSPECL_P pin are pulled "high", or if both of these input pins are pulled "low", tthen the Receive STS-3 TOH Processor block will declare a "Loss of Optical Carrier" condition. ***Note:*** *This input pin is only active if the "Primary Port" is active. This input pin is inactive if the "Redundant Port" is active.*
AG25	LOSTTL_R	I	TTL	**Loss of Optical Carrier Input – Redundant:** The user is expected to connect the "Loss of Carrier" output (from the Optical Transceiver) to this input pin. If this input pin and the LOSPECL_R are pulled "high", or if both of these input pins are pulled "low", then the Receive STS-3 TOH Processor block will declare a "Loss of Optical Carrier" condition. ***Note:*** *This input pin is only active if the "Redundant Port" is active. This input pin is inactive if the "Primary Port" is active.*
L4	LOSPECL_P	I	LVPECL	**Loss of PECL Interface Input – Primary:** If this input pin is pulled "high", then the Receive STS-3 TOH Processor block will declare a "Loss of PECL Interface" condition. ***Note:*** *This input pin is only active if the "Primary Port" is active. This input pin is inactive if the "Redundant Port" is active.*
L3	LOSPECL_R	I	LVPECL	**Loss of PECL Interface Input – Redundant:** If this input pin is pulled "high", then the Receive STS-3 TOH Processor block will declare a "Loss of PECL Interface" condition. ***Note:*** *This input pin is only active if the "Redundant Port" is active. This input pin is inactive if the "Primary Port" is active.*
V1	LOCKDET	O	CMOS	**Lock Detect Output Pin – Clock and Data Recovery PLL Block** This output pin indicates whether the Clock and data recovery PLL block has obtained lock to incoming STS-3/STM-1 signal or not. This pin pulses high if internal VCO frequency is within 0.05% of external reference clock This pin pulses low if internal VCO frequency is beyond 0.05% of external reference clock, and Loss of lock is declared.

STS-3/STM-1 TELECOM BUS INTERFACE – TRANSMIT DIRECTION				
E1	TXA_CLK/ TxAPSCLK	O I/O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Clock Output Signal:** This output clock signal functions as the clock source for the Transmit STS-3/STM-1 Telecom Bus. All signals, that are output via the Transmit STS-3/STM-1 Telecom Bus Interface (e.g., TXA_C1J1, TXA_ALARM, TXA_DP, TXA_PL and TXA_D[7:0]) are updated upon the rising edge of this clock signal. This clock signal operates at 19.44MHz and is derived from the Clock Synthesizer block. **Transmit Payload APS Bus Interface Clock Input/Output signal – TxAPSCLK:** This pin can only be configured to operate in this mode if the XRT94L33 has been configured to operate in either the "ATM UNI" over "PPP over STS-3c" Mode.
F2	TXA_C1J1	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Output Signal:** This output pin pulses "high" under the following two conditions. • Whenever the C1 byte is being output via the "TxA_D[7:0]" output, and • Whenever the J1 byte is being output via the "TxA_D[7:0]" output. ***Notes:*** 1. *The Transmit STS-3/STM-1 Telecom Bus Interface will indicate that it is currently transmitting the C1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "TXA_CLKTXA_CK") and keeping the "TXA_PL" output pin pulled "LOW".* 2. *The Transmit STS-3/STM-1 Telecom Bus will indicate that it is currently transmitting the J1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "TXA_CLKTXA_CK") while the "TXA_PL" output pin is pulled "HIGH".* 3. *This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface block is enabled and is configured to operate in the "Re-Phase OFF" Mode.*

E2	TXA_ALARM/ TxAPSPAR	O I/O	CMOS TTL/ CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface – Alarm Indicator Output signal:** This output pin pulses "high", coincident to the instant that the Transmit STS-3/STM-1 Telecom Bus Interface outputs an byte of any STS-1 or STS-3c signal (via the "TXD_D[7:0]" output pins) that is carrying an AIS-P indicator. This output pin is "low" for all other conditions. **NOTE:** This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface is enabled and has been configured to operate in the "Re-Phase OFF" Mode. **Transmit Payload APS Bus Interface – Parity Input/Output pin:** This pin can only be configured to operate in this role/function if the XRT94L33 has been configured to operate in the "ATM UNI" or the "PPP over STS-3c" Mode. Please see the "XRT94L33_Pin_Description_ATM_PPP.pdf" document for more information.
H3	TXA_DP	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface – Parity Output pin:** This output pin can be configured to function as either one of the following. The EVEN or ODD parity value of the bits which are output via the "TXA_D[7:0]" output pins. The EVEN or ODD parity value of the bits which are being output via the "TXA_D[7:0]" output pins and the states of the "TXA_PL" and "TXA_C1J1" output pins. *NOTES:* *a. The user can make any one of these configuration selections by writing the appropriate value into the "Telecom Bus Control" Register (Address Location = 0x0137).* b. *This output pin is only active if the XRT94L33 has been configured to output its STS-3/STM-1 or STS-3c data via the Transmit STS-3/STM-1 Telecom Bus Interface block.*

G4	TxSBFP	I	TTL	**Transmit STS-3/STM-1 Frame Alignment Sync Input:** The Transmit STS-3 TOH Processor Block can be configured to initiate its generation of a new "outbound" STS-3/STM-1 frame based upon an externally supplied 8kHz clock signal to this input pin. If the user opts to use this feature, then the Transmit STS-3/STM-1 Telecom Bus Interface will begin transmitting the very first byte of given STS-3 or STM-1 frame, upon sensing a rising edge (of the 8kHz signal) at this input pin. ***Notes:*** 1. *If the user connects this input pin to GND, then the Transmit STS-3 TOH Processor block will generate its "outbound" STS-3/STM-1 frames asynchronously, with respect to any input signal.* 2. *This input signal must be synchronized with the signal that is supplied to the REFTTL input pin. Failure to insure this will result in bit errors being generated within the outbound STS-3/STM-1 signal.* 3. *The user must supply an 8kHz pulse (to this input pin) that has a width of approximately 51.4412.8ns (one 19.44MHz clock period). The user must not apply a 50% duty cycle 8kHz signal to this input pin.* 4. *Register "HRSYNC_DLY" (Address Location: 0x0135) defines the timing for TxSBFP input pin.*
K5	TxA_PL/ TxAPSReq	O I/O	CMOS TTL/ CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface – Payload Data Indicator Output Signal:** This output pin indicates whether the Transmit STS-3/STM-1 Telecom Bus Interface is currently placing a Transport Overhead byte or a "non-Transport Overhead Byte (e.g., STS-1 SPE, STS-3c SPE, VC-3 or VC-4 data) via the "TXA_D[7:0]" output pins. This output pin is pulled "low" for the duration that the Transmit STS-3/STM-1 Telecom Bus Interface is transmitting a Transport Overhead byte via the "TXA_D[7:0]" output pins. Conversely, this output pin is pulled "high" for the duration that the STS-3/STM-1 Transmit Telecom Bus is transmitting something other than a Transport Overhead byte via the "TXA_D[7:0]" output pins. **Transmit Payload APS Bus Interface – Request Input/Output pin:** This pin can only be configured to operate in this role if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

J4 G3 D1 F3 J5 H4 D2 E3	TxA_D0/ TxAPSDat0 TxA_D1/ TxAPSDat1 TxA_D2/ TxAPSDat2 TxA_D3/ TxAPSDat3 TxA_D4/ TxAPSDat4 TxA_D5/ TxAPSDat5 TxA_D6/ TxAPSDat6 TxA_D7/ TxAPSDat7	O O I/O	CMOS CMOS CMOS/ TTL	**Transmit STS-3/STM-1 Telecom Bus Interface – Transmit Output Data Bus pins:** These 8 output pins function as the "Transmit STS-3/STM-1 Telecom Bus Interface" – Data bus output pins. If the STS-3/STM-1 Telecom Bus Interface is enabled, then all "outbound" STS-3/STM-1 data is output via these pins (in a byte-wide manner), upon the rising edge of the "TXA_CLK" output clock signal. **Transmit Payload APS Bus Interface – Data Input/Output pins:** These pins can only be configured to operate in this function/role if the XRT94L33 has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode.

STS-3/STM-1 TELECOM BUS INTERFACE – RECEIVE DIRECTION				
W2	RxD_CLK/ RxAPSClk	I I I/O	TTL TTL TTL/ CMOS	**Receive STS-3/STM-1 Telecom Bus Interface - Clock Input Signal:** This input clock signal functions as the clock source for the Receive STS-3/STM-1 Telecom Bus Interface block. All input signals are sampled upon the falling edge of this input clock signal. This clock signal should operate at 19.44MHz. ***Note:*** *This input pin is only used if the "STS-3/STM-1 Telecom Bus" has been enabled. It should be connected to GND otherwise.* **Receive Payload APS Bus Interface - Clock input/output signal:** This input can only be configured to operate in this role/function if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

AA3	RxD_PL	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface – Payload Data Indicator Output Signal:** This input pin indicates whether or not the Receive STS-3/STM-1 Telecom Bus Interface is currently receiving Transport Overhead bytes or "non-Transport Overhead bytes (e.g., STS-1 SPE, STS-3c SPE,VC-3 or VC-4 data) via the "RXD_D[7:0]" input pins. This input pin should be pulled "low" for the duration that "STS-3/STM-1 Receive STS-3/STM-1 Telecom Bus Interface is receiving a Transport Overhead byte via the "RXD_D[7:0]" input pins. Conversely, this input pin should be pulled "high" for the duration that the Receive STS-3/STM-1 Telecom Interface Bus is receiving something other than a Transport Overhead byte via the "RXD_D[7:0]" input pins. ***Note:*** *The user should connect this pin to GND if the STS-3/STM-1 Telecom Bus is NOT enabled.*
AD1	RxD_C1J1/ RxAPSVal	I I/O	TTL TTL/ CMOS	**Receive STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Input Signal/Receive APS Valid Indicator Input/Output signal:** The exact function of this input pin depends upon (1) whether the STS-3/STM-1 Telecom Bus Interface has been enabled or not, and (2) whether the Payload APS Bus has been enabled or not. **If the STS-3/STM-1 Telecom Bus Interface has been enabled – RxD_C1J1:** This input pin should be pulsed "high" during both of the following conditions. a. Coincident to whenever the C1/J0 byte is being applied to the Receive STS-3/STM-1 Telecom Bus – Data Input pins (RXD_D[7:0]). b. b. Coincident to whenever the J1 byte is being applied to the Receive STS-3/STM-1 Telecom Bus – Data Input pins (RXD_D[7:0]) input. *NOTE: This input pin should be pulled "low" during all other times.* **Receive Payload APS Bus Interface – Data Valid Input/Output Signal:** This pin can only be configured to operate in this role if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

AB3	RxD_DP	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface – Parity Input pin:** This input pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits which are input via the "RXD_D[7:0]" input pins. The EVEN or ODD parity value of the bits which are being input via the "RXD_D[7:0]" input and the states of the "RXD_PL" and "RXD_C1J1" input pins. ***Notes:*** 1. *The user can make any one of these configuration selections by writing the appropriate value into the "Telecom Bus Control" register (Address Location = 0x0137).* 2. *The user should connect this pin to GND if the STS-3/STM-1 Telecom Bus Interface is disabled.*
W1	RxD_ALARM/ RxAPSPAR	I I/O	TTL TTL/ CMOS	**Receive STS-3/STM-1 Telecom Bus Interface – Alarm Indicator Input:** This input pin pulses "high" coincident to whether the Receive STS-3/STM-1 Telecom Bus Interface block is receiving a byte (via the "RxD_D[7:0] input pins) that is a part of any STS-1 or STS-3c signal that is carrying the AIS-P indicator. ***Note:*** *If the RxD_ALARM input signal pulses "HIGH" for any given STS-1 signal (within the "incoming" STS-3), then the corresponding Receive SONET POH Processor block will automatically declare the AIS-P defect condition.* **RxAPSParity – Receive Payload APS Bus Interface – Parity Input/Output Pin:** This pin can only be configured to operate in this role if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

Y2	RxD_D0/ RxHRDat0/ RxAPSDat0	I I I/O	TTL TTL TTL/	**Receive STS-3/STM-1 Telecom Bus Interface – Receive Input Data Bus pins - RxD_D[7:0]:** These 8 input pins function as the Receive STS-3/STM-1 Telecom Bus Interface - Input data bus. All incoming STS-3/STM-1 data is sampled and latched (into the XRT94L33, via these input pins) upon the falling edge of the "RXD_CLK" input clock signal. **RxHRDat[7:0]: Receive data inputs for high-rate device** **Receive Payload APS Bus Interface – Data Bus Input/Output Pins:** These pins can only be configured to function in this role if the XRT94L33 has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. These pins cannot be configured to support "Payload APS" operation if the XRT94L33 has been configured to operate in an "Aggregation" role.
AD2	RxD_D1 RxHRDat1/ RxAPSDat1		CMOS	
AC3	RxD_D2 RxHRDat2/ RxAPSDat2			
AA4	RxD_D3 RxHRDat3/ RxAPSDat3			
AB4	RxD_D4 RxHRDat4/ RxAPSDat4			
Y1	RxD_D5 RxHRDat5/ RxAPSDat5			
AD3	RxD_D6 RxHRDat6/ RxAPSDat6			
AA5	RxD_D7 RxHRDat7/ RxAPSDat7			

SONET/SDH OVERHEAD INTERFACE – TRANSMIT DIRECTION				
H6	TxTOHClk	O	CMOS	**Transmit TOH Input Port – Clock Output:** This output pin, along with the "TxTOHEnable", "TxTOHFrame" output pins and the "TxTOH" and "TxTOHIns" input pins function as the "Transmit TOH Input Port". The Transmit TOH Input Port permits the user to externally insert his/her own value(s) for the TOH bytes (within the outbound STS-3/STM-1 signal). This output pin provides the user with a clock signal. If the "TxTOHEnable" output pin is "HIGH" and if the "TxTOHIns" input pin is pulled "HIGH", then the user is expected to provide a given bit (within the "TOH") to the "TxTOH" input pin, upon the falling edge of this clock signal. The data, residing on the "TxTOH" input pin will be latched into the XRT94L33 upon the rising edge of this clock signal. ***Note:*** *The Transmit TOH Input Port only supports the insertion of the TOH within the very first STS-1 of the outbound STS-3 signal.*
G5	TxTOHEnable	O	CMOS	**Transmit TOH Input Port – TOH Enable (or READY) indicator:** This output pin, along with the "TxTOHClk", "TxTOHFrame" output pins and the "TxTOH" and "TxTOHIns" input pins function as the "Transmit TOH Input Port". This output pin will toggle and remain "HIGH" anytime the "Transmit TOH Input Port" is ready to externally accept TOH data via the "TxOH" input pin. To externally insert user values of TOH into the "outbound" STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHFrame" and this output pin upon the rising edge of "TxTOHClk". • Whenever this output pin pulses "HIGH", then the user's external circuitry should drive the "TxTOHIns" input pin "HIGH". • Next, the user should output the next TOH bit, onto the "TxTOH" input pin, upon the rising edge of "TxTOHClk"

F8	TxTOH	I	TTL	**Transmit TOH Input Port – Input pin:** This input pin, along with the "TxTOHIns" input pin, the "TxTOHEnable" and "TxTOHFrame" and "TxTOHClk" output pins function as the "Transmit TOH Input Port". To externally insert user values of TOH into the outbound STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHFrame" and "TxTOHEnable" upon the rising edge of "TxTOHClk. • Whenever "TxTOHEnable" pulses "HIGH", then the user's external circuitry should drive the "TxTOHIns" input pin "HIGH". • Next, the user should output the next TOH bit, onto this input pin, upon the rising edge of "TxTOHClk". The "Transmit TOH Input Port" will sample the data (on this input pin) upon the falling edge of "TxTOHClk". ***Note:*** *Data at this input pin will be ignored (e.g., not sampled) unless the "TxTOHEnable" output pin is "HIGH" and the "TxTOHIns" input pin is pulled "HIGH".*
E8	TxTOHFrame	O	CMOS	**Transmit TOH Input Port – STS-3/STM-1 Frame Indicator:** This output pin, along with "TxTOHClk", "TxTOHEnable output pins, and the "TxTOH" and "TxTOHIns" input pins function as the "Transmit TOH Input Port". This output pin will pulse high (for one period of TxTOHClk), one "TxTOHClk" clock period prior to the first "TOH bit" of a given STS-3 frame, being expected via the "TxTOH" input pin. To externally insert user values of TOH into the "outbound" STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHEnable" and this output pin upon the rising edge of "TxTOHClk". • Whenever the "TxTOHEnable" output pin pulse "HIGH", then the user's external circuitry should drive the "TxTOHIns" input pin "HIGH". • Next, the user should output the next TOH bit, onto the "TxTOH" input pin, upon the rising edge of "TxTOHClk". ***Note:*** *The external circuitry (which is being interfaced to the "Transmit TOH Input Port" can use this particular output pin to denote the boundary of STS-3 frames.*

D6	TxTOHIns	I	TTL	**Transmit TOH Input Port – Insert Enable Input pin:** This input pin, along with the "TxTOH" input pin, and the "TxTOHEnable", "TxTOHFrame" and "TxTOHClk" output pins function as the "Transmit TOH Input Port". This input pin permits the user to either enable or disable the "Transmit TOH Input Port". If this input pin is "LOW", then the "Transmit TOH Input Port" will be disabled and will not sample and insert (into the "outbound" STS-3 data stream) any data residing on the "TxTOH" input, upon the rising edge of "TxTOHClk" If this input pin is "HIGH", then the "Transmit TOH Input Port" will be enabled. In this mode, whenever the "TxTOHEnable" output pin is also "HIGH", the "Transmit TOH Input Port" will sample and latch any data that is presented on the "TxTOH" input pin, upon the rising edge of "TxTOHClk". To externally insert user values of TOH into the "outbound" STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHFrame" and "TxTOHEnable" upon the rising edge of "TxTOHClk". • Whenever the "TxTOHEnable" output pin is sampled "high" then the user's external circuitry should drive this input pin "HIGH". • Next, the user should output the next TOH bit, onto the "TxTOH" input pin, upon the falling edge of "TxTOHClk". The "Transmit TOH Input Port" will sample the data (on this input pin) upon the falling edge of "TxTOHClk".] ***Notes:*** *1. Data applied to the "TxTOH" input pin will be sampled according to the following insertion priority scheme:* *2. For DCC, E1, F1, E2 bytes, "TxTOH" input pin will be sampled if both "TxTOHEnable" and "TxTOHIns" are high.* *3. For other TOH bytes, "TxTOH" input pin will be sampled if both "TxTOHEnable" and "TxTOHIns" are high or if both "TxTOHIns" and "Software Insertion Enabled" are "low".*

B4	TxLDCCEnable	O	CMOS	**Transmit – Line DCC Input Port – Enable Output pin:** This output pin, along with the "TxTOHClk" output pin and the "TxLDCC" input pin permit the user to insert their value for the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D4, D5, D6, D7, D8, D9, D10, D11 and D12 byte-fields, within the "outbound" STS-3 data-stream. The Line DCC HDLC Controller circuitry (which is connected to the "TxTOHClk", the "TxSDCC" and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "HIGH", then the Line DCC HDLC Controller circuitry should place the next Line DCC bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto the "TxLDCC" input pin, upon the rising edge of "TxTOHClk". Any data that is placed on the "TxLDCC" input pin, will be sampled upon the falling edge of "TxOHClk".
D7	TxSDCCEnable	O	CMOS	**Transmit – Section DCC Input Port – Enable Output pin:** This output pin, along with the "TxTOHClk" output pin and the "TxSDCC" input pin permit the user to insert their value for the D1, D2 and D3 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D1, D2 and D3 byte-fields, within the "outbound" STS-3 data-stream. The Section DCC HDLC Controller circuitry (which is connected to the "TxTOHClk", the "TxSDCC" and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "HIGH", then the Section DCC HDLC Controller circuitry should place the next Section DCC bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto the "TxSDCC" input pin, upon the rising edge of "TxTOHClk". Any data that is placed on the "TxSDCC" input pin, will be sampled upon the falling edge of "TxOHClk".