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GENERAL DESCRIPTION

The XRT94L43 is an SDH to PDH physical layer processor with integrated SONET OC-12 and 12 DS3/E3 framing controller. The XRT94L43 contains an integral SONET framer which provides framing and error accumulation in accordance with ANSI/ITU-T specifications. For a multiple channel DS3/E3 feature, each channel contains identical elements. The configuration of this device is through internal registers accessible via an 8-bit parallel, memory mapped, microprocessor interface.

The SONET/SDH transmit and receive blocks are used to transmit/receive an STS-12/STM-4 signals or compose and decompose 12, STS-1/DS3/E3 signals. The blocks operate at a peak internal clock speed of 77 MHz and support 8-bit internal data paths. The transmit and receive blocks are compliant with both SONET and SDH standards.

The XRT94L43 performs all SONET transport and path overhead processing for use in broadband data transport applications.

FEATURES

- Single Chip solution for 12 DS3/E3 to SONET/SDH Mapping
- Generates and terminates SONET section, line and path layers.
- Provides SONET frame scrambling and descrambling.
- Differential Line Interfaces
- 8-bit microprocessor interface
- Requires +2.5 and +3.3V power supplies with +5V input tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 516 Ball PBGA package

APPLICATIONS

- Network switches
- Concentrators
- Frame Relay Switches
- SONET Customer Premises Multiplexers
- Network Access Equipment
- Test/Monitoring Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT94L43 WHEN CONFIGURED IN SONET MODE

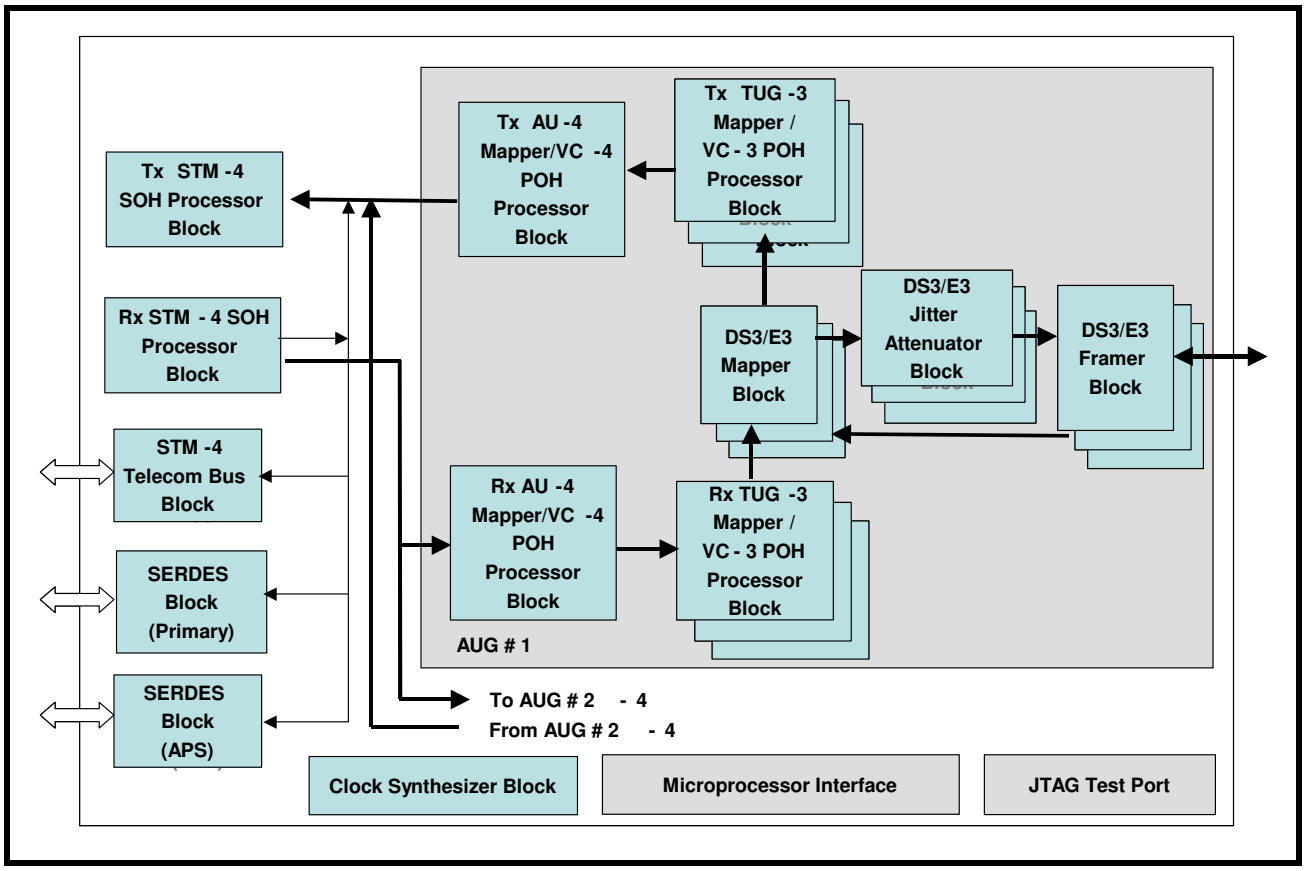


FIGURE 2. BLOCK DIAGRAM OF THE XRT94L43 WHEN CONFIGURED IN SDH/TUG-3 MODE

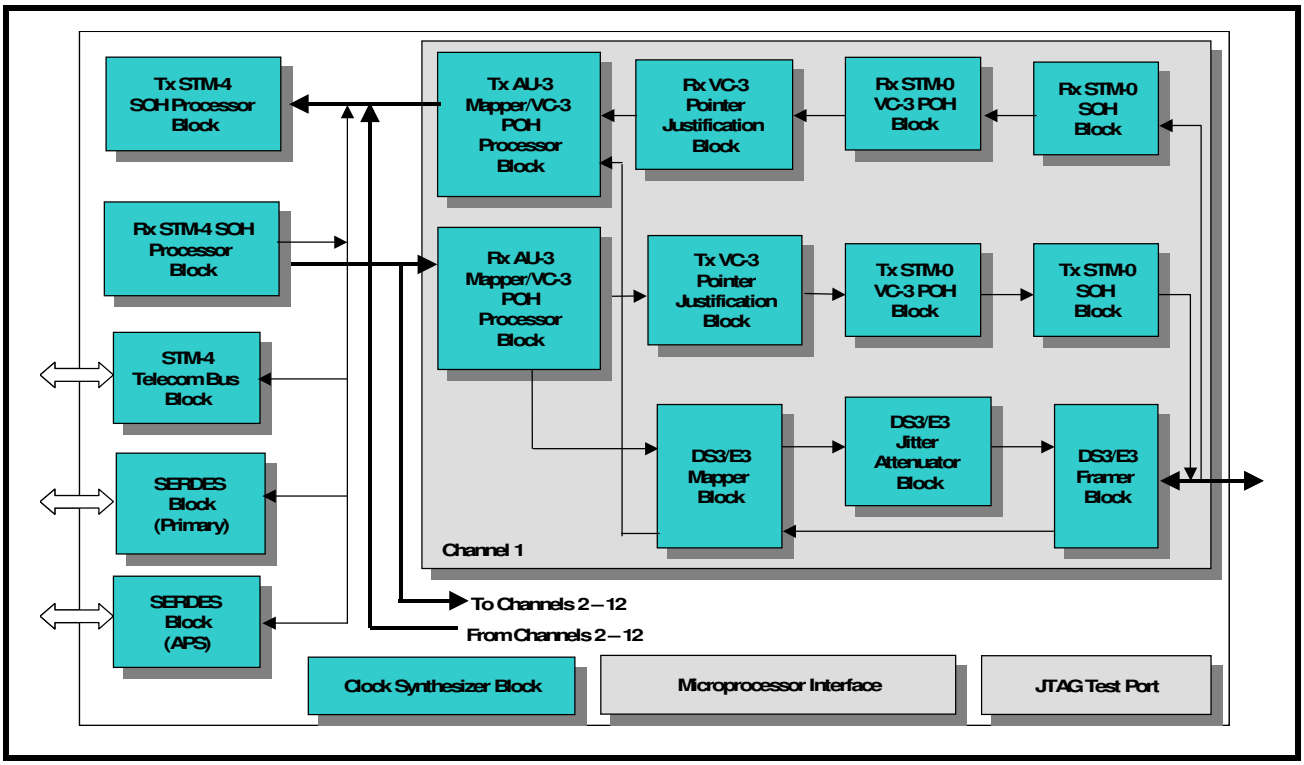
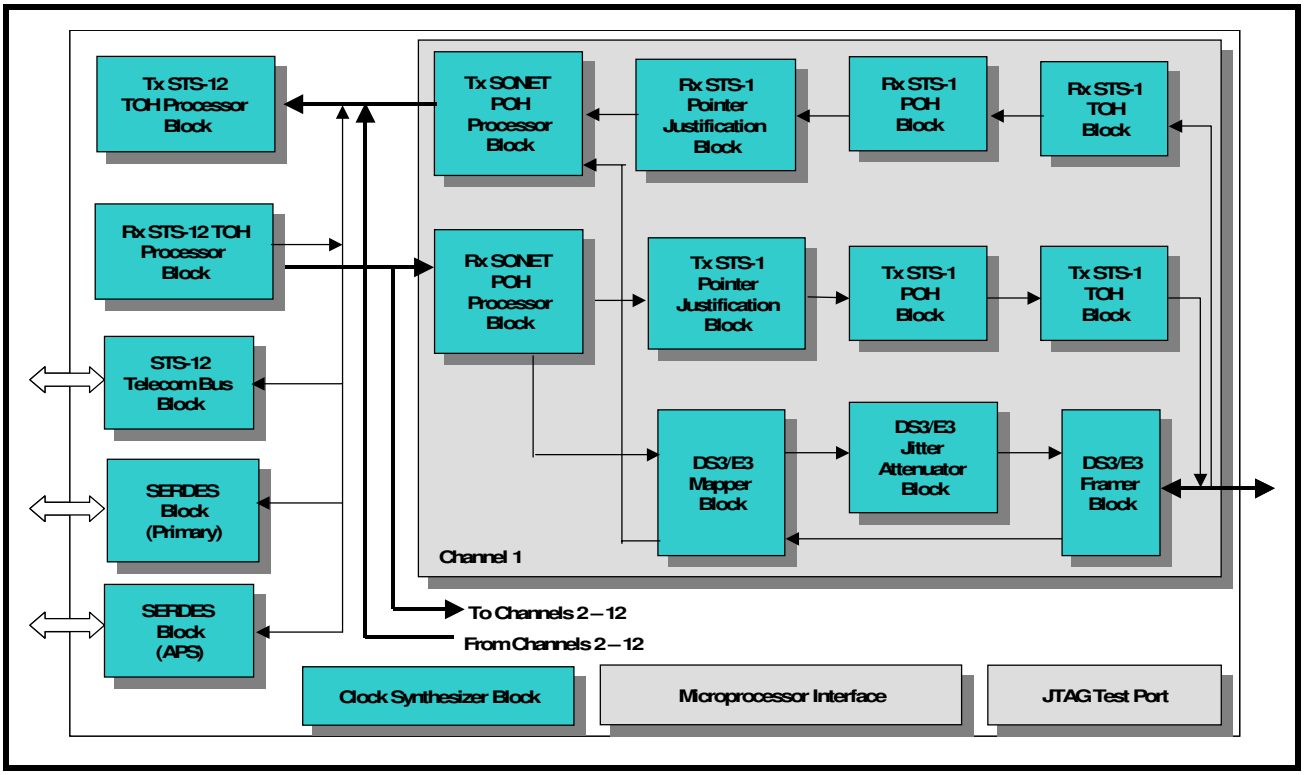


FIGURE 3. BLOCK DIAGRAM OF THE XRT94L43 WHEN CONFIGURED IN SDH/AU-3 MODE



PRODUCT FEATURES

SONET TRANSMITTER

- Generates and Transmits Standard STS-12/STM-4 data
- Generates and Transmits either an STM-4/TUG-3 or STM-4/AU-3 signals for SDH applications
- Conforms to ITU-T 1.432, ANSI T1.105 and Bellcore GR-253 Standards
- Performs SONET frame insertion and accepts external frame synchronization
- Performs Optional Transmit Data Scrambling
- Permits the user to externally insert their own values for the POH and TOH into the outbound STS-12/STM-4 traffic
- Generates transmit payload pointer (H1,H2) (fixed at 522) with NDF insertion
- Inserts A1/A2 with optional error mask
- Computes and inserts BIP-8 (B1,B2) with optional error mask
- Generates and transmits REI-L and RDI-L either upon Software Command or automatically based upon errors and defects that are detected/declared by the SONET Receiver.
- Permits the user to transmit the LOS pattern via Software Command.
- Generates and transmits RDI-P and REI-P either upon Software Command or automatically based upon errors and defects that are detected/declared by the SONET Receiver.
- Inserts the fixed-stuff columns, calculates and inserts the B3 byte value into each outbound STS-1 SPE/VC-3 or STS-3c SPE/VC-4

SONET RECEIVER

- Receives and processes standard STS-12/STM-4 signals
- Receives and processes either an STM-4/TUG-3 or STM-4/AU-3 signal for SDH Applications
- Permits the user to fully program the B2 Byte Error-rate thresholds for declaration and clearance of the SD and SF defect conditions
- Provides section trace buffer with mismatch detection and invalid message detection
- Performs SONET Frame Synchronization
- Supports NDF, positive stuff and negative stuff for pointer processor
- Performs receive data de-scrambling
- Performs POH and TOH interpretation/extraction
- Interprets payload pointer (H1,H2)
- Extracts data communication channels from D1-D3 and D4-D12
- Declares and Clears the SEF (Severely Erred Frame), LOF (Loss of Frame) and LOS (Loss of Signal) defect conditions
- Declares and clears the Line AIS (AIS-L) and the Line Remote Defect Indicator (RDI-L) defect conditions
- Declares and Clears the Path - AIS (AIS-P), Loss of Pointer (LOP-P) and Path - Unequipped (UNEQ-P) defect conditions.
- Supports either the Single-Bit or Extended form of RDI-P
- Monitors the Path Signal Label and declares/clears the PLM-P defect condition

- Contains 12 on-chip 64 byte Expected Receive Path Trace Message Buffer, in which the user will load in an expected Path Trace Message
- Contains 12 on-chip 64 byte Actual" Receive Path Trace Message Buffers, that will contain the actual Received Path Trace Message
- The SONET Receiver will use the contents within both the Expected and Actual Receive Path Trace Message Buffers to either declare or clear the TIM-P defect condition
- Computes and verifies the B3 bytes within each incoming STS-1 SPE/VC-3 or STS-3c SPE/VC-4 and increments on-chip Performance Monitoring registers each time it detects B3 byte errors.
- Detects and Flags Line - Remote Error Indicator (REI-L) and Path - Remote Error Indicator (REI-P) events, and increments on-chip Performance Monitoring registers each time it detects REI-L or REI-P events
- Computes and verifies both the B1 and B2 bytes within the incoming STS-12/STM-4 data-stream and increments on-chip Performance Monitoring registers each time it detects B1 or B2 byte errors

MAPPER

- Maps DS3 data into/De-maps DS3 data from an STS-1 SPE per the requirements in Telcordia GR-253-CORE
- Maps DS3/E3 data into/De-Maps DS3/E3 data from a VC-3 per ITU-T G.707
- Implements AU-3 to VC-3 multiplexing and de-multiplexing

DS3 RECEIVE FRAMER

- Offers off-line framing algorithm
- Complies with the standards as: Bellcore TR-NWT-000499 and TR-NWT-000009
- Supports overhead extraction
- Detects and flags LCV (Line Code Violations) and EXZ (Excessive Zero Events).
- Reports and counts FEBE
- HDLC controller complies with ITU-T Q.921 LAPD protocol
- Provides Line and Local Loop-backs
- Supports either the M13 or the C-bit Parity Framing formats
- Supports B3ZS line decoding which can be user enabled.Replaces valid B0V or 00V with 3 zeros
- Synchronizes to incoming frame based upon 10 valid F bits followed by 3 consecutive valid M frames, Offers optional AIC-bit or parity verification before declaration of sync
- Detects Out of Frame (OOF) upon 3 or 6 F bits out of 15 F bits in error or 1 or more M bits in 3 of 4 consecutive frames in error
- Detects Loss of Signal (LOS) upon encountering 180 consecutive 0's and clears on at least 60 of successive received 1's.Offers optional disable
- Detects idle state by checking C-bit in subframe 3 are all zero, X-bits are one and repeating 11001100 payloads. Declaration occurs when all the above conditions persist for 63 M-frames. Clears the condition when 63 valid M-frames are received
- Detects AIS with different algorithm
- Computes and verifies P and CP-Bits
- Validate FERF bits, sets to one when both X-bits are zero and clears when they are One
- Detects and validates FEAC codes upon 8 out of 10 last identical received codes.Invalidates on 3 in 10 mismatch

- Provides 15-bit PRBS lock

DS3 TRANSMIT FRAMER

- Offers following frame generation mechanism: Asynchronous operation, using receive side clock, external framing
- Supports either C-bit operation or M13 operation: optional all C bits set to "1" or C-bit parity ID bit (C11) toggled in each frame for M13 operation
- Provides start of frame control with external pin
- Inserts frame overhead bits via External serial port or Internal generation
- Generates and checks parity
- Automatically transmits the DS3 FERF/REI indicator whenever the DS3 Receiver declares either the DS3 LOS, DS3 AIS or DS3 OOF defect conditions.
- Permits the user to control the DS3 FEBE/REI bit-fields via Software Control, or to automatically transmit the FEBE/REI indicator whenever the DS3 Receiver detects CP-Bit or Framing (F or M) bit errors
- Provides FEAC channel processing including generation of valid FEAC patterns and transmissions of all 1's upon programming of idle code
- Inserts path maintenance data link through HDLC transmitter which contains the following features:
  - AM for storage of entire LAPD message
  - Selection of message length to 82 or 76 bytes
  - Optional frame header generation
  - Generation of flag sequences
  - Computation and insertion of CRC
  - Zero stuffing
  - Register bits for communication with microprocessor
  - Interrupt generation upon transmission of message
- LOS Insertion enabled by register bit
- AIS Insertion enabled by register bit or pin
- Idle signal insertion enabled by register bit
- Supports B3ZS encoding
- Generates AIS, Idle and Yellow force alarms
- Inserts errors optionally in the P, F, FEBE and M bits
- Provides 15-bit PRBS generator

E3 RECEIVE FRAMER

- Offers off-line framing algorithm
- Complies with standards as: ITU-T G.751 and G.832
- Provides line code violation detection and excess zero count
- LAPD controller complies with ITU Q.921 LAPD protocol
- Provides local loop-back
- Supports G.751 and G.832 framing formats
- Supports HDB3 line decoding which can be user enabled. Replaces valid B00V or 000V with 4 zero's

- Synchronizes to incoming frame based upon occurrence of two sets of FA1, FA2 with expected separation - G.832 or detection of three consecutive frame alignment signals (FAS) - G.751
- Detects Out of Frame (OOF) upon 4 consecutive invalid frames
- Detects Loss of Signal (LOS) upon encountering 32 consecutive 0's and clears on occurrence of 32 bits without a string of 4 0s
- Detects AIS if 7 or less 0s detected in each of 2 consecutive frames and clears if more than seven 0's detected in each of 2 consecutive frames
- Calculation and comparison of BIP-8 (G.832) or BIP-4 (G.751). BIP-4 calculation can be disabled
- Supports overhead extraction
- Microprocessor access to TR trail trace message - 16 TTB registers (G.832) or service (Alarm and Nation) bits (G.751)
- Detects MA FERF if 3 or 5 consecutive MA MSBs are 1and clears if 3 or 5 consecutive MA MSBs are 0 (only E3 G.832)
- Indicates last validated FERF value and interrupt upon a change in validated FERF value
- Extracts payload type (MA) bits and stores in a register (Only E3 G.832)
- Extracts Timing Marker bit and checks for consistency over 3 or 5 consecutive frames (only E3 G.832)
- Extracts Synchronous Status Message bits and stores it in register bits when enabled (only G.832)
- Overhead output on synchronous serial interface

E3 TRANSMIT FRAMER

- Offers following frame generation mechanism: Asynchronous operation, using receive side clock, external framing
- Supports either G.751 or G.832 framing format
- Generates and checks parity BIP-8 (G.832), BIP-4 (G.751) BIP-4 computation can be disabled
- Inserts data link message through E3 data line channel which contains the following features:
  - Insertion into NR or GC byte (programmable through register bit) (E3 G.832 only)
  - Insertion into Nation bit in case of E3 G.751 when LAPD is enabled
  - RAM storage of entire LAPD message
  - Selection of message length to 82 or 76 bytes
  - Generation of flag sequences
  - Computation and insertion of CRC-16
  - Zero stuffing
  - Register bits for communication with microprocessors
  - Interrupt generation upon complete transmission of message
- LOS insertion enabled by register bit to force all 0s in the transmit stream
- AIS insertion enabled by register bit and/or pin to force all 1's in the transmit stream
- Supports HDB3 encoding enabled by register bit
- Inserts frame overhead bits via External serial/nibble port (except for FA1,FA2 and EM bytes in case of E3 G.832 and FAS and BIP-4 in case of G.751) or through external overhead interface or from configuration register or internal generation
- Inserts FA1, FA2, EM, TR, MA and GC bytes into G.832 stream or FAS service bits and BIP4 (if enabled) into G.751 stream

- Inserts MA,NR,GC and TR (TTB) from microprocessor accessible registers (service bit for G.751)
- Inserts FEBE in MA upon receipt of EM byte errors.Programmable through register bit (G.832)
- Asserts FERF upon any combination of LOS,OOF or AIS received from receiver (G.832)
- Inserts synchronous status message from microprocessor accessible registers, when enabled (G.832)
- Error masks for framing bytes, and computed parity (BIP-8 in case of G.832 and BIP-4 in case of G.751)
- Optionally accepts overhead bits (except FA bytes for G.832 and FAS bits for G.751) from input interface

E3/DS3/STS-1 DE-JITTERING/DE-SYNC CIRCUIT

- Meets the E3/DS3/STS-1 jitter requirements
- Compliant with jitter transfer template outlined in ITU G.751,G.752,G.755 and GR-499-CORE
- Meets output jitter requirement as specified by ETSI TBR24
- Meets the jitter and wander specifications described in T1.105.03b,GR-253 and GR-499 standards
- Performs the De-synchronizer function and pointer adjustments for STS-1 to DS3 mapping

PERFORMANCE MONITORING

- Supports line and path performance monitoring
- Provides 32-bit saturating counter of OOF errors
- Provides 32-bit saturating counter LOF errors
- Provides 32-bit saturating counter of LOS errors
- Provides 32-bit saturating counter of SD errors
- Provides 32-bit saturating counter of SF errors
- Provides 32-bit saturating counter B3 errors
- Provides 32-bit saturating counter of the line RDI, path AIS,REI-L errors, REI-P errors and BIP-8(B1,B2),B3 errors and loss of pointer
- Provides 16-bit saturating counter of DS3 framing bit errors, DS3 frame parity errors, line code violations, frame parity (BIP) errors, DS3 frame CP bit errors and DS3 Far-End Block errors
- One second statistics
    1. Bipolar violations
    2. Frames with parity errors
    3. Frames with CP bit errors
    4. Errored second indication
    5. Severely errored second indication

INTERRUPT, STATUS AND TEST

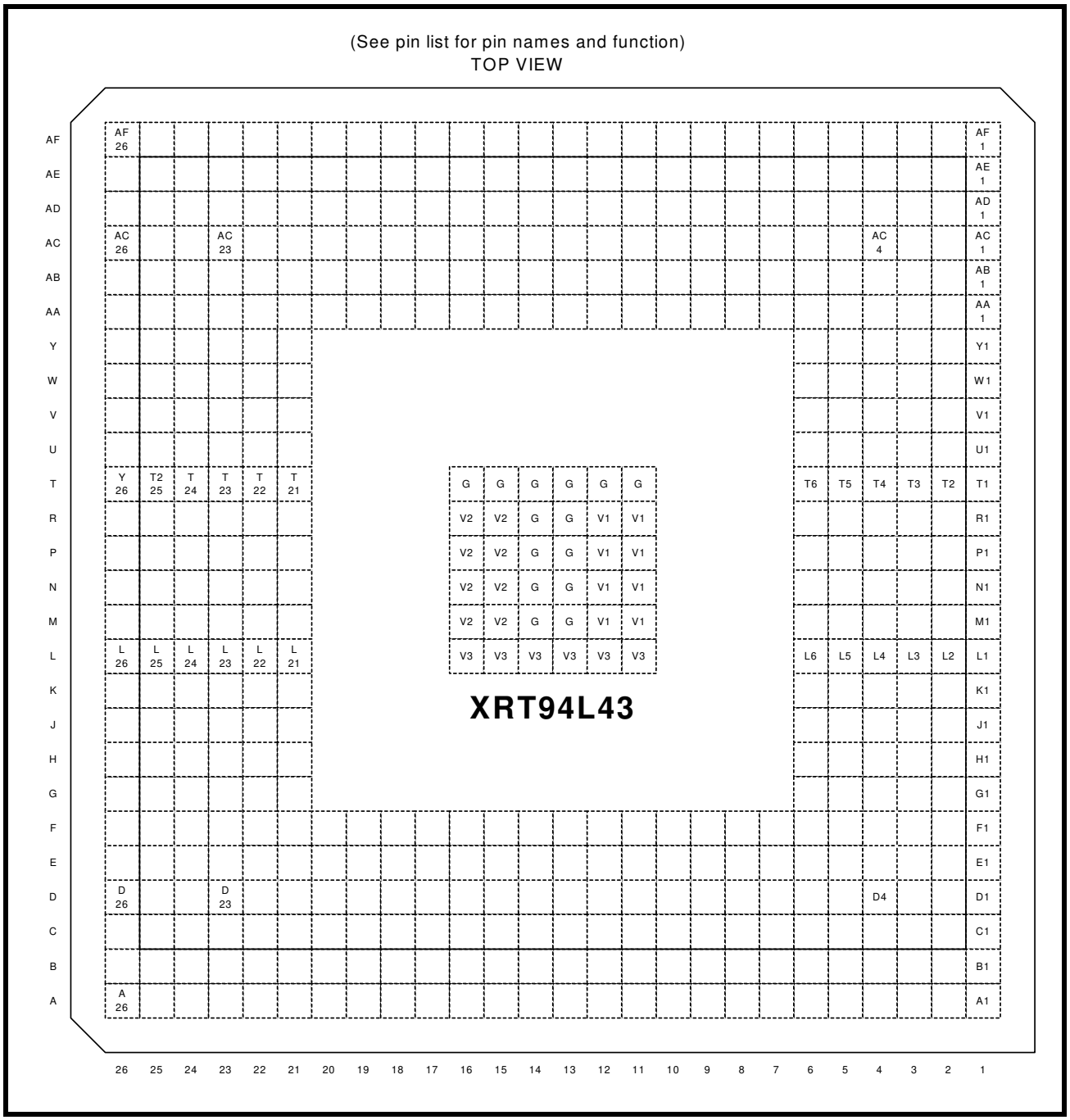
- Provides individually maskable interrupts
- Provides one second interrupt generations
- Generates interrupts from the following causes:
- DS3 OOF status change, LOS status change, DS3 AIS status, LAPD message received, DS3 parity error,DS3 FEAC validation, DS3 FEAC removal, DS3 IDLE status change, FEBE (E3) change, DS3 FERF change, DS3 format change (AIC), LAPD end of message transmission and DS3 FEAC end of message transmission, DS3 Framing alignment change, SONET OOF status change and COFA
- Provides local and remote line loopback

- Provides SONET remote loopback

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L43IB	516 Ball BGA	-40°C to +85°C

FIGURE 4. PIN OUT OF THE XRT94L43



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10.1 TRANSMIT LINE DCC INSERTION INPUT PORT 314
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11.1 RECEIVE TOH OVERHEAD OUTPUT PORT 315
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12.1 RECEIVE POH OVERHEAD OUTPUT PORT 316
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13.0 RECEIVE ORDERWIRE (E1, F1, E2) BYTES OVERHEAD OUTPUT PORT 317
13.1 RECEIVE E1, F1, E2 (ORDER-WIRE) BYTE OVERHEAD OUTPUT PORT 317
FIGURE 29. TIMING WAVEFORM OF THE RECEIVE ORDER-WIRE BYTE OVERHEAD OUTPUT PORT 318
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14.0 RECEIVE SECTION DCC EXTRACTION OUTPUT PORT 318
14.1 RECEIVE SECTION DCC OUTPUT PORT 318
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15.0 RECEIVE LINE DCC EXTRACTION OUTPUT PORT 319
15.1 RECEIVE LINE DCC OUTPUT PORT 319
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PIN DESCRIPTIONS - DIRECT ADDRESSING

MICROPROCESSOR INTERFACE

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
U22	PCLK	I	TTL	**Microprocessor Interface Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in one of the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in one of these modes, then it will use this clock signal to do the following. • To sample the $\overline{CS}$, $\overline{WR}$/R/$\overline{W}$, A[15:0], D[7:0], $\overline{RD}$/$\overline{DS}$ and DBEN input pins, and • To update the state of the D[7:0] and the RDY/DTACK output signals. ***NOTES:*** *1. The Microprocessor Interface can work with µPCLK frequencies ranging up to 66MHz.* *2. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronous Modes. In this case, the user should tie this pin to GND.*
L25 L23 L22	PTYPE_0 PTYPE_1 PTYPE_2	I	TTL	**Microprocessor Type Select input:** These three input pins are used to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. **PTYPE[2:0] Microprocessor Interface Mode** 000 Intel - Asynchronous Mode l001 Motorola - Asynchronous Mode (Motorola 68k) 010 Intel X86 011 Intel I960 100 IDT3051/52 (MIPS) 101 Power PC 403 Mode
A23 F24 W21 AE22 A25 H24 AB23 AD15 V26 R24 P26 M24 T26 M22 M25 L26	PADDR_0 PADDR_1 PADDR_2 PADDR_3 PADDR_4 PADDR_5 PADDR_6 PADDR_7 PADDR_8 PADDR_9 PADDR_10 PADDR_11 PADDR_12 PADDR_13 PADDR_14 PADDR_15	I	TTL	**Address Bus Input pins (Microprocessor Interface):** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations (within the XRT94L43) whenever it performs READ and WRITE operations with the XRT94L43.

MICROPROCESSOR INTERFACE

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
T22 R22 U24 R21 W26 T25 R25 R26	PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	I/O	TTL	**Bi-Directional Data Bus Pins (Microprocessor Interface):** These pins are used to drive and receive data over the bi-directional data bus,, whenever the Microprocessor performs READ or WRITE operations with the Microprocessor Interface of the XRT94L43.
Y26	$\overline{WR}$/ R/$\overline{W}$	I	TTL	**Write Strobe/Read-Write operation Identifier:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - $\overline{WR}$ - Write Strobe Input:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the $\overline{WR}$ (Active Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pin, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT94L43) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - R/$\overline{W}$ - Read/Write Operation Identification Input Pin:** If the Microprocessor Interface is operating in the "Motorola-Asynchronous Mode", then this pin is functionally equivalent to the "R/$\overline{W}$" input pin. In the Motorola Mode, a "READ" operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin. Similarly a WRITE operation occurs if this pin is at a logic "0", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin. **Power PC 403 Mode - R/$\overline{W}$ - Read/Write Operation Identification Input:** If the Microprocessor Interface is configured to operate in the Power PC 403 Mode, then this input pin will function as the "Read/Write Operation Identification Input" pin. Anytime the Microprocessor Interface samples this input signal at a logic low (while also sampling the $\overline{CS}$ input pin "low") upon the rising edge of μPCLK, then the Microprocessor Interface will (upon the very same rising edge of μPCLK) latch the contents of the Address Bus (A[15:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the $\overline{DBEN}$/$\overline{OE}$ input pin, and the Microprocessor Interface will then place the contents of the "target" register (or address location within the XRT94L43) upon the Bi-Directional Data Bus pins (D[7:0]), where it can be read by the Microprocessor . Anytime the Microprocessor Interface samples this input signal at a logic high (while also sampling the $\overline{CS}$ input pin a logic "low") upon the rising edge of μPCLK, then the Microprocessor Interface will (upon the very same rising edge of μPCLK) latch the contents of the Address Bus (A[15:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the $\overline{RD}$/$\overline{DS}$/$\overline{WE}$ input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the "target" register or buffer location (within the XRT94L43).

MICROPROCESSOR INTERFACE

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
T23	$\overline{RD}$/ $\overline{DS}$/ $\overline{WE}$	I	TTL	**READ Strob/Data Strobe:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - $\overline{RD}$ - READ Strobe Input:** If the Microprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the $\overline{RD}$ (Active Low Read Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT94L43 will place the contents of the addressed register (or buffer location) on the Microprocessor Interface Bi-directional data bus (D[7:0]). When this signal is negated, then the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode - $\overline{DS}$ - Data Strobe:** If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this input pin will function as the $\overline{DS}$ (Data Strobe) input signal. **Power PC 403 Mode - $\overline{WE}$ - Write Enable Input:** If the Microprocessor Interface is operating in the Power PC 403 Mode, then this input pin will function as the $\overline{WE}$ (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with $\overline{CS}$ and $\overline{WR}$/R/$\overline{W}$) also being asserted (at a logic low level) upon the rising edge of μPCLK, then the Microprocessor Interface will (upon the very same rising edge of μPCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the "target" on-chip register or buffer location within the XRT94L43.
R23	PALE/PAS_L	I	TTL	**Address Latch Enable/Address Strobe:** This input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[6:0]) into the Mapper/Framer Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. This input pin is active-High, in the Intel Mode and active-Low in the Motorola Mode.
V22	PCS_L	I	TTL	**Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT94L43 on-chip registers and buffer locations.

MICROPROCESSOR INTERFACE

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION

Y25	PRDY_L/ $\overline{\text{DTACK}}$/ RDY	O	CMOS	**READY or DTACK Output:**
				The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in.
				Intel-Asynchronous Mode - $\overline{\text{RDY}}$ - Ready Output:
				If the Microprocessor Interface has been configured to operate in the Intel-Asynchronous Mode, then this output pin will function as the "active-low" READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "high" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				Motorola-Asynchronous Mode - $\overline{\text{DTACK}}$ - Data Transfer Acknowledge Output
				If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the "active-low" DTACK output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "high" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				Power PC 403 Mode - RDY - Ready Output:
				If the Microprocessor Interface has been configured to operate in the Power PC 403 Mode, then this output pin will function as the "active-high" READY output.During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at the logic "high" level (upon the rising edge of PCLK), then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "low" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it samples this output pin being at the logic low level.
				NOTE: *The Microprocessor Interface will update the state of this output pin upon the rising edge of* μP*CLK.*

MICROPROCESSOR INTERFACE

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
T21	PDBEN_L	I	TTL	**Bi-directional Data Bus Enable Input Pin:** This input pin permits the user to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. Setting this input pin "low" enables the Bi-directional Data bus. Setting this input "high" tri-states the Bi-directional Data Bus.
U25	PBLAST_L	I	TTL	**Last Burst Transfer Indicator input Pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. ***NOTE:*** *If the user has configured the Microprocessor Interface to operate in the Intel-Asynchronous, the Motorola-Asynchronous or the Power PC 403 Mode, then he/she should tie this input pin to GND.*
AC26	PINT_L	O	CMOS	**Interrupt Request Output:** This active-Low, active-low output signal will be asserted when the XRT94L43 is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the Interrupt Request input of the Microprocessor.
L24	RESET_L	I	TTL	**Reset Input:** When this active-Low signal is asserted, the XRT94L43 will be asynchronously reset. When this occurs, all outputs will be tri-stated and all on-chip registers will be reset to their default values.
M26	FULL_ADDR_SEL	I	TTL	Full Address Select input pin:This input pin, along with "DIRECT_ADD_SEL" (pin M23) must both be pulled "HIGH" in order to configure the Microprocessor Interface block to operate in the "Full Address" Mode.If the Microprocessor Interface is configured to operate in the "Full Address" Mode, then it will then provide a 16-bit Address Bus (which is sufficient to "Directly Address" all of the on-chip registers.
M23	DIRECT_ADD_SEL	I	TTL	Direct Address Select input pin:This input pin, along with "FULL_ADDR_SEL" (pin M26) must both be pulled "HIGH" in order to configure the Microprocessor Interface block to operate in the "Full Address" Mode.If the Microprocessor Interface is configured to operate in the "Full Address" Mode, then it will then provide a 16-bit Address Bus (which is sufficient to "Directly Address" all of the on-chip registers.

SONET/SDH SERIAL LINE INTERFACE PINS

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
M5	RXL_CLKL_P	I	LVPECL	**Receive STS-12/STM-4 Clock - Positive Polarity PECL Input:** This input pin, along with RXL_CLKL_N functions as the Recovered Clock Input, from a System back-plane or an Optical Transceiver. The Receive STS-12/STM-4 Interface Block will sample the data, applied at the RXLDATA_P/RXLDATA_N input pins, upon the rising edge of this signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_CLKL_N functions as the Primary Receive Clock Input port.*
L5	RXL_CLKL_N	I	LVPECL	**Receive STS-12/STM-4 Clock - Negative Polarity PECL Input:** This input pin, along with RXL_CLKL_P functions as the Recovered Clock Input, from a System back-plane or an Optical Transceiver. The Receiver STS-12/STM-4 Interface Block will sample the data applied at the RXLDATA_P/RXLDATA_N input pins, upon the falling edge of this signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_CLKL_P functions as the Primary Receive Clock Input Port.*
K2	RXL_CLKL_R_P	I	LVPECL	**Receive STS-12/STM-4 Clock - Positive Polarity PECL Input - Redundant Port:** This input pin, along with RXL_CLKL_R_N functions as the Recovered Clock Input, from a System back-plane or an Optical Transceiver. The Receive STS-12/STM-4 Interface Block will sample the data, applied at the RXLDATA_P/RXLDATA_N input pins, upon the rising edge of this signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_CLKL_R_N functions as the Redundant Receive Clock Input Port.*
K1	RXL_CLKL_R_N	I	LVPECL	**Receive STS-12/STM-4 Clock - Negative Polarity PECL Input - Redundant Port:** This input pin, along with RXL_CLKL_P functions as the Recovered Clock Input, from a System back-plane or an Optical Transceiver. The Receiver STS-12/STM-4 Interface Block will sample the data applied at the RXLDATA_P/RXLDATA_N input pins, upon the falling edge of this signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_CLKL_R_ P functions as the Redundant Receive Clock Input Port.*
K4	RXL_DATA_P	I	LVPECL	**Receive STS-12/STM-4 Data - Positive Polarity PECL Input:** This input pin, along with RXL_DATA_N functions as the Recovered Data Input, from a System back-plane or an Optical Transceiver. The Receive STS-12/STM-4 Interface block will sample the data applied to these input pins, upon the rising edge of the RXL_CLKL_P (and the falling edge of the RXL_CLKL_N) signals. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_DATA_N functions as the Primary Receive Data Input Port.*

SONET/SDH SERIAL LINE INTERFACE PINS

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
L4	RXL_DATA_N	I	LVPECL	**Receive STS-12/STM-4 Data - Negative Polarity PECL Input:** This input pin, along with RXL_DATA_P functions as the Recovered Data Input, from a System back-plane or an Optical Transceiver. The Receive STS-12/STM-4 Interface block will sample the data applied to these input pins, upon the rising edge of the RXL_CLKL_P (and the falling edge of the RXL_CLKL_N) signals. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_DATA_P functions as the Primary Receive Data Input Port.*
K3	RXL_DATA_R_P	I	LVPECL	**Receive STS-12/STM-4 Data - Positive Polarity PECL Input - Redundant Port:** This input pin, along with RXL_DATA_R_N functions as the Recovered Data Input, from a System back-plane or an Optical Transceiver. The Receive STS-12/STM-4 Interface block will sample the data applied to these input pins, upon the rising edge of the RXL_CLKL_R_P (and the falling edge of the RXL_CLKL_R_N) signals. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_DATA_R_N functions as the Redundant Receive Data Input Port.*
L3	RXL_DATA_R_N	I	LVPECL	**Receive STS-12/STM-4 Data - Negative Polarity PECL Input - Redundant Port:** This input pin, along with RXL_DATA_R_P functions as the Recovered Data Input, from a System back-plane or an Optical Transceiver. The Receive STS-12/STM-4 Interface block will sample the data applied to these input pins, upon the rising edge of the RXL_CLKL_R_P (and the falling edge of the RXL_CLKL_R_N) signals. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXL_DATA_R_N functions as the Redundant Receive Data Input Port.*
T3	TXL_CLKI_P	I	LVPECL	**Transmit Reference Clock - Positive Polarity PECL Input:** This input pin, along with TxL_CLKI_N can be configured to function as the timing source for the STS-12/STM-4 Transmit Interface Block. If these two input pins are configured to function as the timing source, then a 622.08MHz clock signal must be applied to these input pins in the form of a PECL signal. These two inputs can be configured to function as the timing source by writing the appropriate data into the Interface Control Register - Byte 2 (Indirect Address = 0x00, 0x31), (Direct Address = 0x0131).

SONET/SDH SERIAL LINE INTERFACE PINS

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
T4	TXL_CLKI_N	I	LVPECL	**Transmit Reference Clock - Negative Polarity PECL Input:** This input pin, along with TxL_CLKI_P can be configured to function as the timing source for the STS-12/STM-4 Transmit Interface Block. If these two input pins are configured to function as the timing source, then a 622.08MHz clock signal must be applied to these input pins in the form of a PECL signal. These two inputs can be configured to function as the timing source by writing the appropriate data into the Interface Control Register - Byte 2 (Indirect Address = 0x00, 0x31), (Direct Address = 0x0131).
N1	TXL_DATA_P	O	LVPECL	**Transmit STS-12/STM-4 Data - Positive Polarity PECL Output:** This output pin, along with TXL_DATA_N functions as the Transmit Data Output, to the System back-plane (for transmission to some other System Board) or an Optical Transceiver (for transmission to remote terminal equipment). For High-Speed Back-Plane Applications, it should noted that data is output from these output pins upon the rising/falling edge of TXL_CLKO_P/TXL_CLKO_N). ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_DATA_N functions as the Primary Transmit Data Output Port.*
N2	TXL_DATA_N	O	LVPECL	**Transmit STS-12/STM-4 Data - Negative Polarity PECL Output:** This output pin, along with TXL_DATA_P functions as the Transmit Data Output, to the System back-plane (for transmission to some other System Board) or an Optical Transceiver (for transmission to remote terminal equipment). For High-Speed Back-Plane Applications, it should noted that data is output from these output pins upon the rising/falling edge of TXL_CLKO_P/TXL_CLKO_N). ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_DATA_P functions as the Primary Transmit Data Output Port.*
P1	TXL_DATA_R_P	O	LVPECL	**Transmit STS-12/STM-4 Data - Positive Polarity PECL Output - Redundant Port:** This output pin, along with TXL_DATA_R_N functions as the Transmit Data Output, to the System back-plane (for transmission to some other System Board) or an Optical Transceiver (for transmission to remote terminal equipment). For High-Speed Back-Plane Applications, it should noted that data is output from these output pins upon the rising/falling edge of TXL_CLKO_R_P/TXL_CLKO_R_N). ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_DATA_N functions as the Redundant Transmit Data Output Port.*

SONET/SDH SERIAL LINE INTERFACE PINS

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
P2	TXL_DATA_R_N	O	LVPECL	**Transmit STS-12/STM-4 Data - Negative Polarity PECL Output - Redundant Port:** This output pin, along with TXL_DATA_R_P functions as the Transmit Data Output, to the System back-plane (for transmission to some other System Board) or an Optical Transceiver (for transmission to remote terminal equipment). For High-Speed Back-Plane Applications, it should noted that data is output from these output pins upon the rising/falling edge of TXL_CLKO_R_P/TXL_CLKO_R_N). ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_DATA_R_P functions as the Redundant Transmit Data Output Port.*
M1	TXL_CLKO_P	O	LVPECL	**Transmit STS-12/STM-4 Clock - Positive Polarity PECL Output:** This output pin, along with TXL_CLKO_N functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the TXL_DATA_P/TXL_DATA_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_CLKO_N functions as the Primary Transmit Output Clock signal.*
M2	TXL_CLKO_N	O	LVPECL	**Transmit STS-12/STM-4 Clock - Negative Polarity PECL Output:** This output pin, along with TXLCLKO_P functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the TXL_DATA_P/TXL_DATA_N output pins upon the falling edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_CLKO_N functions as the Primary Transmit Output Clock signal.*
R1	TXL_CLKO_R_P	O	LVPECL	**Transmit STS-12/STM-4 Clock - Positive Polarity PECL Output - Redundant Port:** This output pin, along with TXL_CLKO_R_N functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the TXL_DATA_R_P/TXL_DATA_R_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_CLKO_R_N functions as the Redundant Transmit Output Clock signal.*

SONET/SDH SERIAL LINE INTERFACE PINS

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
R2	TXL_CLKO_R_N	O	LVPECL	**Transmit STS-12/STM-4 Clock - Negative Polarity PECL Output - Redundant Port:** This output pin, along with TXL_CLKO_R_P functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the TXL_DATA_R_P/ TXL_DATA_R_N output pins upon the rising edge of this clock signal. For APS (Automatic Protection Switching) purposes, this output pin, along with TXL_CLKO_R_P functions as the Redundant Transmit Output Clock signal.
R4	REFCLK	I	TTL	**77.76MHz or 622.08MHz Clock Synthesizer Reference Clock Input Pin:** The function of this input pin depends upon whether or not the Transmit STS-12/STM-4 Clock Synthesizer block is enabled. **If Clock Synthesizer is Enabled.** If the Transmit STS-12/STSM-4 Clock Synthesizer block is to be used to generate the 77.76MHz and/or 622.08MHz clock signal for the STS-12/STM-4 block, then a clock signal of either of the following frequencies, must be applied to this input pin. • 12.96MHz • 19.44MHz • 51.84 MHz • 77.76 MHz Afterwards, the appropriate data needs to be written into the Interface Control Register - Byte 2 (Indirect Address = 0x00, 0x31), (Direct Address = 0x0131) in order to; (1) configure the Clock Synthesizer Block to accept any of the above-mentioned signals and generate a 77.76MHz or 622.08MHz clock signal, (2) to configure the Clock Synthesizer to function as the Clock Source for the STS-12/STM-4 block. **If Clock Synthesizer is NOT Enabled:** If the Transmit STS-12/STSM-4 Clock Synthesizer block is NOT to be used to generate the 77.76MHz and/or 622.08MHz clock signal for the STS-12/STM-4 block, then a 77.76MHz clock signal must be applied to this input pin.
AF6	LOS	I	TTL	**Loss of Optical Carrier Input - Primary:** The Loss of Carrier output (from the Optical Transceiver) should be connected to this input pin. If this input pin is pulled "High", then the Primary Receive STS-12 TOH Processor block will declare a Loss of Optical Carrier condition. ***NOTE:*** *This input pin is only active if the Primary Port is active. This input pin is inactive if the Redundant Port is active.*

SONET/SDH SERIAL LINE INTERFACE PINS

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AE6	LOS-R	I	TTL	**Loss of Optical Carrier Input - Redundant:** The Loss of Carrier output (from the Optical Transceiver) should be connected to this input pin. If this input pin is pulled "High", then the Redundant Receive STS-12 TOH Processor block will declare a Loss of Optical Carrier condition. ***NOTE:*** *This input pin is only active if the Redundant Port is active. This input pin is inactive if the Primary Port is active.*
AB7	EXSWITCH	O	CMOS	**External (APS) Switch Output Pin:** This output pin can be used to permit the XRT94L43 to perform APS externally. Specifically, this output pin can be connected to some circuitry that permits the re-direction of STS-12/STM-4 traffic, should an APS event be needed. ***NOTE:*** *This output pin is disabled if the EXSWITCHDIS input pin number AB6 is pulled "High".*
AB6	EXSWITCHDIS	I	TTL	**External (APS) Switch Disable:** This input pin permits the user to configure the XRT94L43 to perform Line APS Switching internally or externally. 0 - Configures the XRT94L43 to perform APS externally. In this mode, the XRT94L43 will execute an APS by toggling the state of the "EXSWITCH" output pin. 1 - Configures the XRT94L43 to perform APS internally. In this mode, each of the 12 Receive SONET POH Processor blocks (within the XRT94L43) will internally switch from processing the incoming STS-1 SPE data from the "Primary" Receive STS-12 TOH Processor block, to now processing the incoming STS-1 SPE data from the "Redundant" Receive STS-12 TOH Processor block (or vice-versa).

STS-12/STM-4 TELECOM BUS INTERFACE - TRANSMIT DIRECTION

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
G2	TXA_CLK	O	CMOS	**STS-12/STM-4 Transmit Telecom Bus Clock Signal:** This output clock signal functions as the clock source for the STS-12/ STM-4 Transmit Telecom Bus. All output signals (on the Transmit STS-12/STM-4 Telecom Bus) are updated upon the rising edge of this clock signal. This clock signal operates at 77.76MHz and is derived from the Transmit Clock Synthesizer block.
J1	TXA_C1J1	O	CMOS	**STS-12/STM-4 Transmit Telecom Bus - C1/J1 Byte Phase Indicator Output Signal:** This output pin pulses "High" under the following two conditions. 1. Whenever the C1 byte is being output via the TxA_D[7:0] output, and 2. Whenever the J1 byte is being output via the TxA_D[7:0] output. ***NOTES:*** *1. The STS-12/STM-4 Transmit Telecom Bus will indicate that it is transmitting the C1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "High" (for one period of TXA_CLK) and keeping the TXA_PL output pin pulled "Low".* *2. The STS-12/STM-4 Transmit Telecom Bus will indicate that it is transmitting the J1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "High" (for one period of TXA_CLK) while the TXA_PL output pin is pulled "High".* *3. This output pin is only active if the STS-12/STM-4 Telecom Bus is enabled.*
J3	TXA_ALARM	O	CMOS	**Transmit STS-12/STM-4 Telecom Bus - Alarm Indicator Output signal:** This output pin pulses "High", corresponding to any STS-1 signal (that is being output via the TXA_D[7:0] output pins) is carrying the AIS-P indicator. This output pin is "Low" for all other conditions.
H1	TXA_DP	O	CMOS	**STS-12/STM-4 Transmit Telecom Bus - Parity Output Pin:** This output pin can be configured to function as one of the following. 1. The EVEN or ODD parity value of the bits which are output via the TXA_D[7:0] output pins. 2. The EVEN or ODD parity value of the bits which are being output via the TXA_D[7:0] output pins and the states of the TXA_PL and TXA_C1J1 output pins. ***NOTE:*** *Any one of these configuration selections can be made by writing the appropriate value into the Telecom Bus Control Register (Indirect Address = 0x00, 0x37), (Direct Address = 0x0137)..*