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VS6502

VGA Color CMOS Image Sensor Module

Features

- **Small physical size: integrated lens in a SmOP (Small Optical Package)**
- **640 x 480 VGA resolution**
- **Up to 30 frame/s VGA, 60 frame/s QVGA**
- **On-chip 10-bit ADC**
- **Automatic dark calibration**
- **2.6 V to 3.6 V power supply**
- **I^2C communications**
- **Low power suspend mode**
- **4 or 5 wire nibble output**
- **Socket available separately**

Description

The VS6502 is a VGA resolution SmOP sensor module. SmOP technology combines the image sensor and fixed focus lens system in a single module. The SmOP sensor module is connected to the PCB either via a socket or flex option. The socket allows the PCB to use standard reflow soldering techniques.

The sensor outputs 10-bit raw digital image data which directly interface to a range of STMicroelectronics companion processors via 4/5 wire interface.

An I^2C interface allows the processor to configure the device and control exposure and gain settings.

There are three different digital video output formats:

- VGA mode - 640 x 480 image size
- Sub-sampled QVGA mode - 320 x 240 image size
- Window Of Interest QVGA mode - 320 x 240 pixel

Applications

- Miniature USB web cameras (STV0676 - STV0674)
- Embedded cameras (STV0676 - STV0674): Handhelds, Cell phones, Network cameras
- Digital stills cameras (STV0674): Minicam, miniature USB flash drive cameras
- Digital video cameras (STV0674)

Technical Specifications

Pixel resolution	644 x 484 (VGA)
Pixel size	5.6 µm x 5.6 µm
Array size	3.6 mm x 2.7 mm
Dynamic range	> 52 dB
Analogue gain	0 to 24dB
Sensitivity (typical)	2.05 V / lux-s
Signal/Noise ratio	+ 37 dB
Supply voltage	2.6 to 3.6 V
Power consumption	Active (30 frame/s) < 30 mA
	Suspend (no clk) < 10 µA
Operating temperature	0 to 40°C
Package size	10.6 mm x 8.7 mm x 5.8 mm
Lens	47° HFOV, f#2.8
Package type	14 pad SmOP

Ordering information

Ordering code	Description
VS6502V015	VS6502 sensor module
XS0015/TR	Socket for sensor module

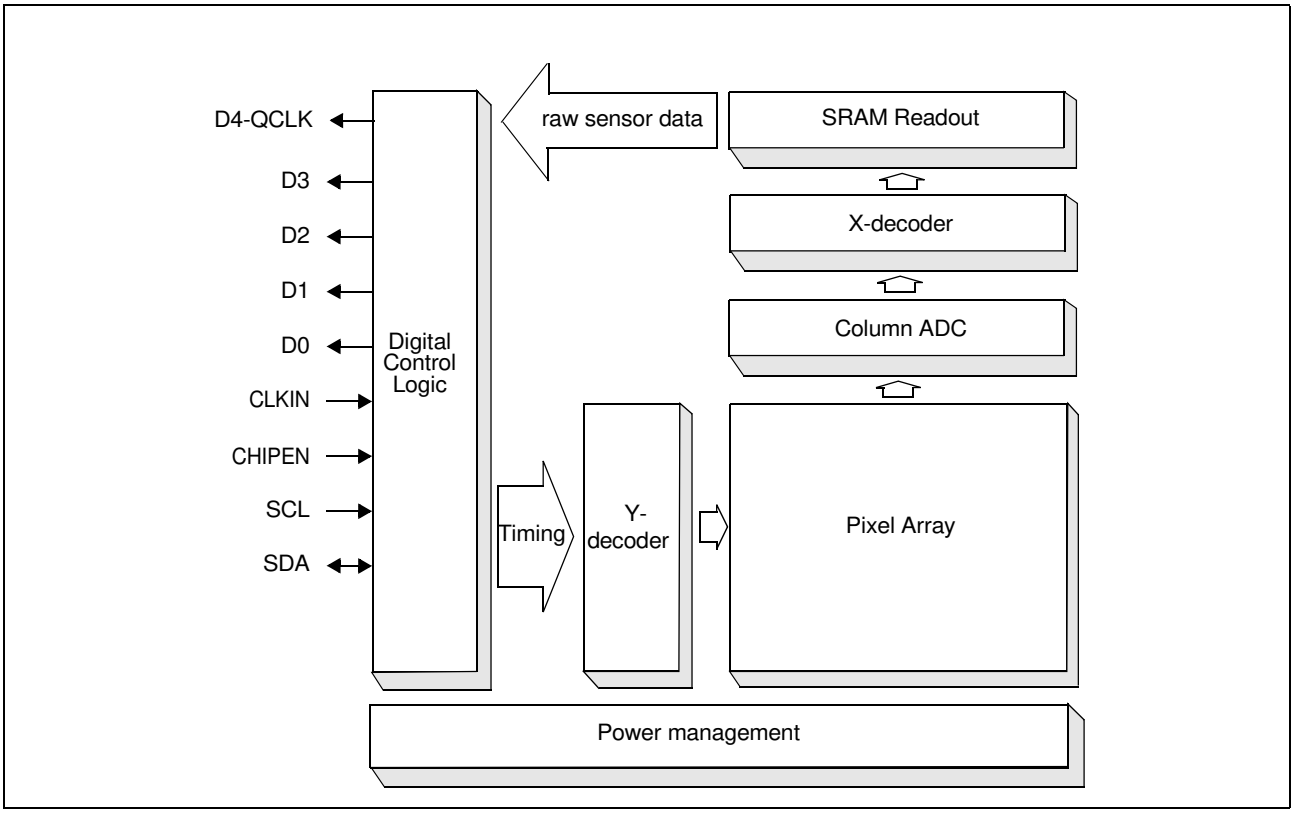
Table of Contents

1 Overview

1.1 Sensor overview

The VS6502 image sensor produces raw digital video data at up to 30 frames per second VGA or 60 frames per second QVGA. The image data is digitized using an internal 10-bit ADC. The resulting 10-bit output data includes embedded codes for synchronization. There are two data output modes; 4-bit nibbles with separate data qualification clock (QCK) or 5-bit nibbles without qualification clock. The sensor is controlled using an I^2C interface.

Figure 1: VS6502 block diagram

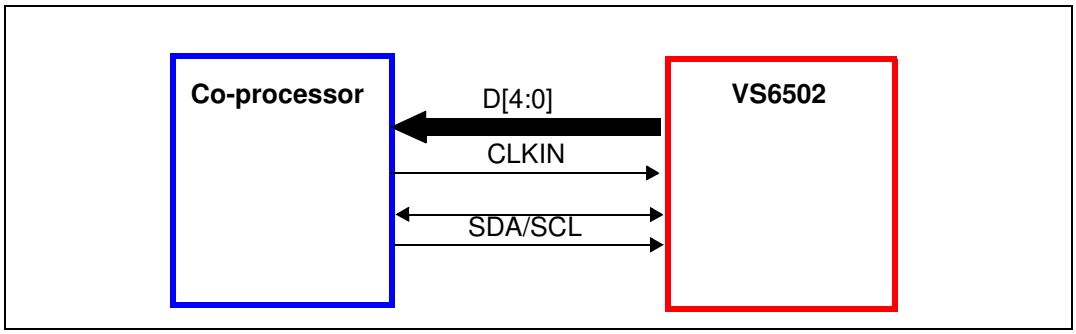


1.2 Typical applications

USB camera with STV0674 or STV0676

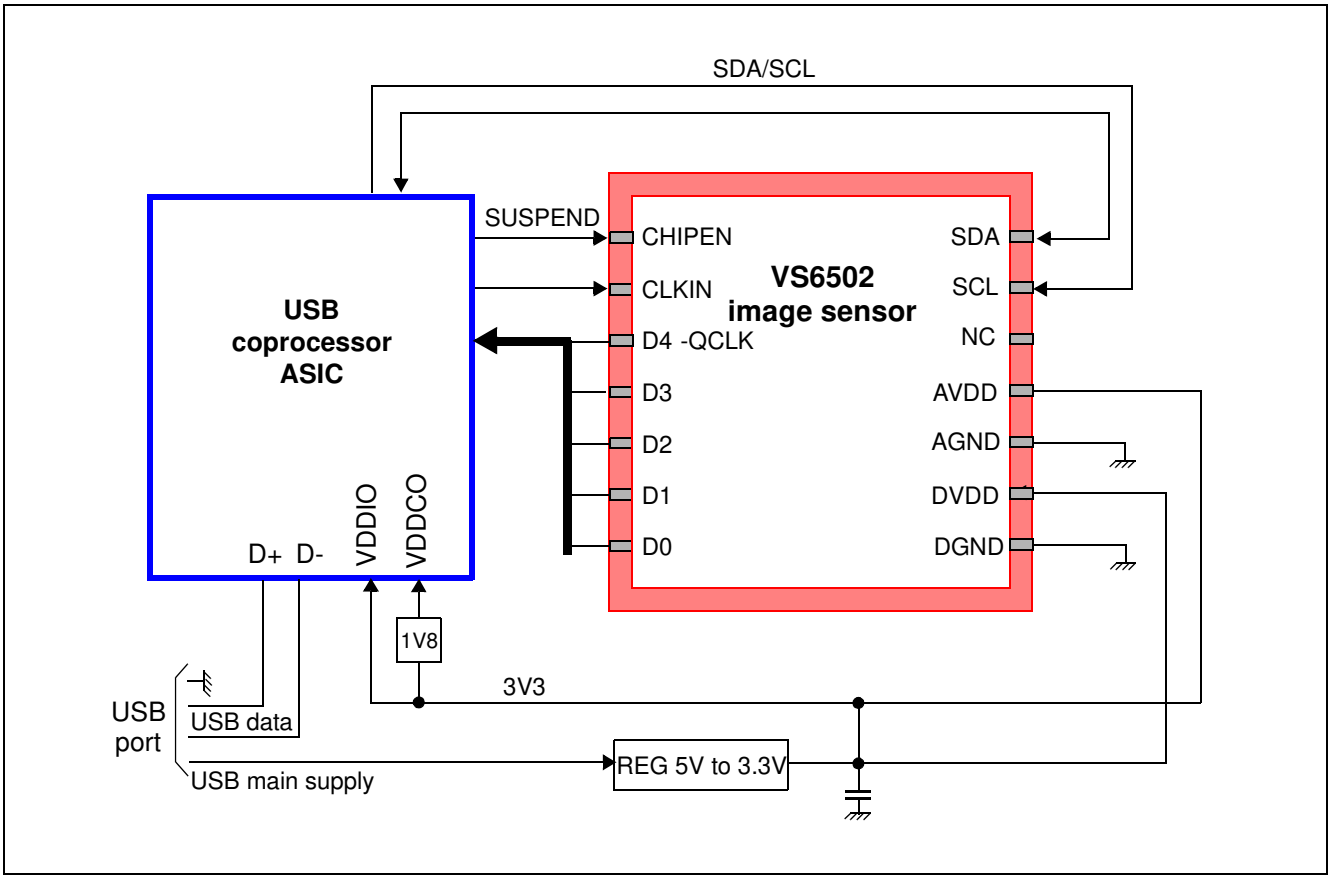
This is a USB video camera where the co-processor supplies the sensor clock CLKIN and uses the embedded control sequences to synchronize with the frame and line level timings.

Figure 2: Overview of USB camera using the VS6502



The USB input supply is 5 V. In the application, a regulator must deliver 3.3 V to both the co-processor and sensor analogue and digital blocks.

Figure 3: USB camera using STV0676/STV0674



1.3 Module Pad Description

1.3.1 Pad assignment

Figure 4: SmOP1.5 - pad assignment

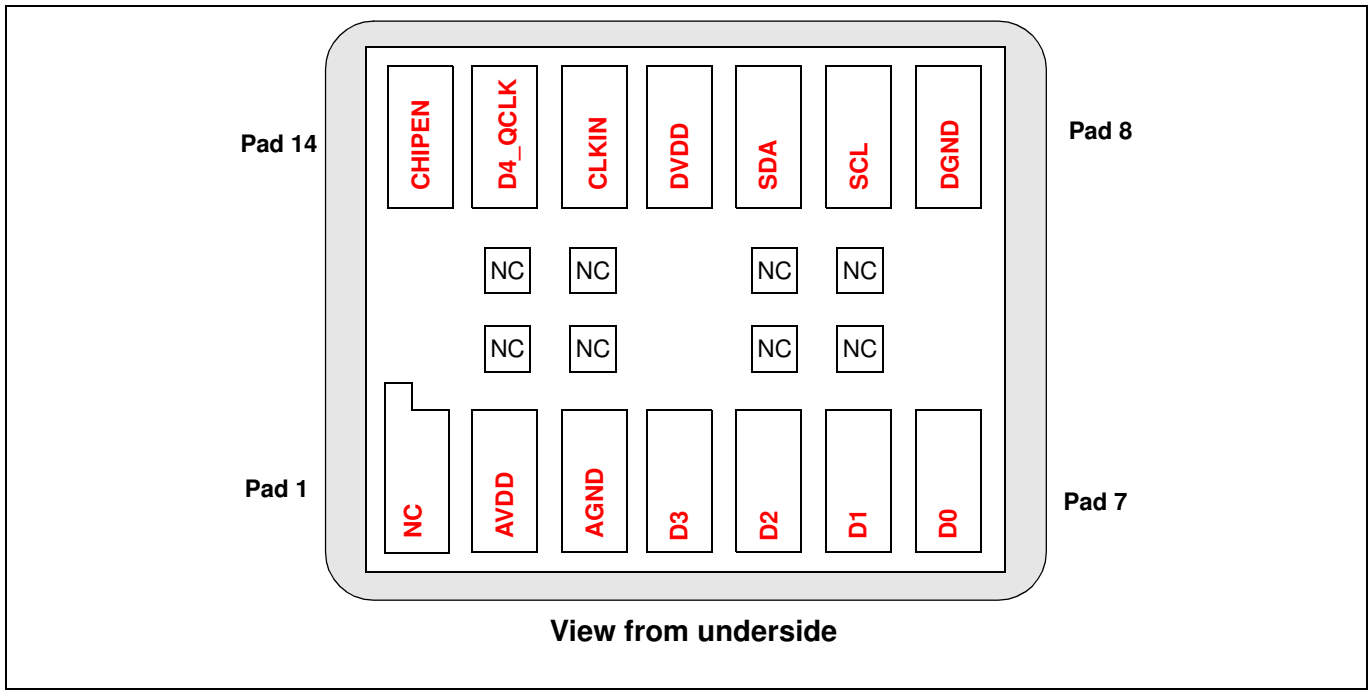


Table 1: Signal description

Pad Number	Pad Name	I/O Type	Description
1	NC	-	Not connected
2	AVDD	PWR	Analogue power supply 3.3V
3	AGND	PWR	Analogue ground
4	D3	O	Data output D3
5	D2	O	Data output D2
6	D1	O	Data output D1
7	D0	O	Data output D0
8	DGND	PWR	Digital Ground
9	SCL	I	I^2C Clock
10	SDA	I/O	I^2C Data
11	DVDD	PWR	Digital power supply 3.3V
12	CLKIN	I	Master clock input
13	D4_QCLK	O	Data output D4 (in 5 -wire mode) Data qualification clock (in 4-wire mode)
14	CHIPEN	I	Chip enable input (LOW = enabled)

2 Functional Description

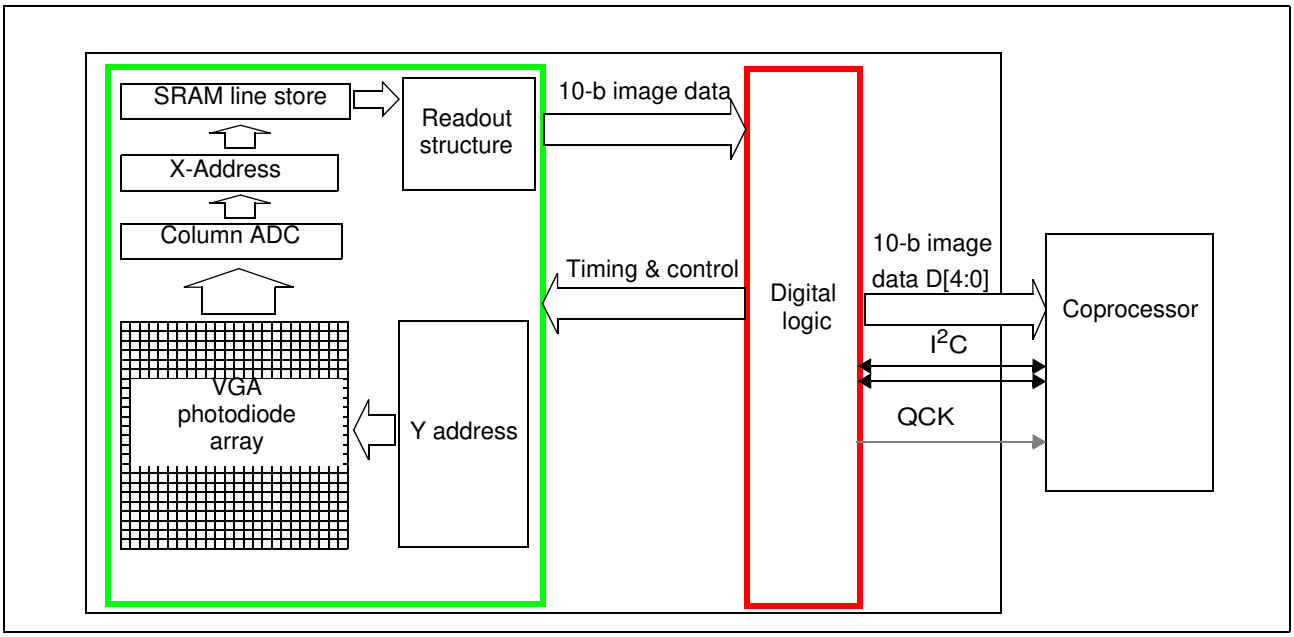
2.1 Video block

2.1.1 Overview

The analogue core of the video block contains a VGA sized pixel array. The integration time and access for a row of pixels is controlled by the Y-address block. The row of pixels being read is converted using a 10-bit in-column ADC. The digitised data is read out into the digital block for formatting. The 10-b data is transferred to the co-processor over a 5-wire digital bus as two 5-b nibbles. An alternative mode allows the transfer of the data as 8 bits per pixel with an additional qualification clock signal (QCK)

The exposure or integration time for the pixel array is calculated by the external co-processor and delivered to the sensor using the I2C interface.

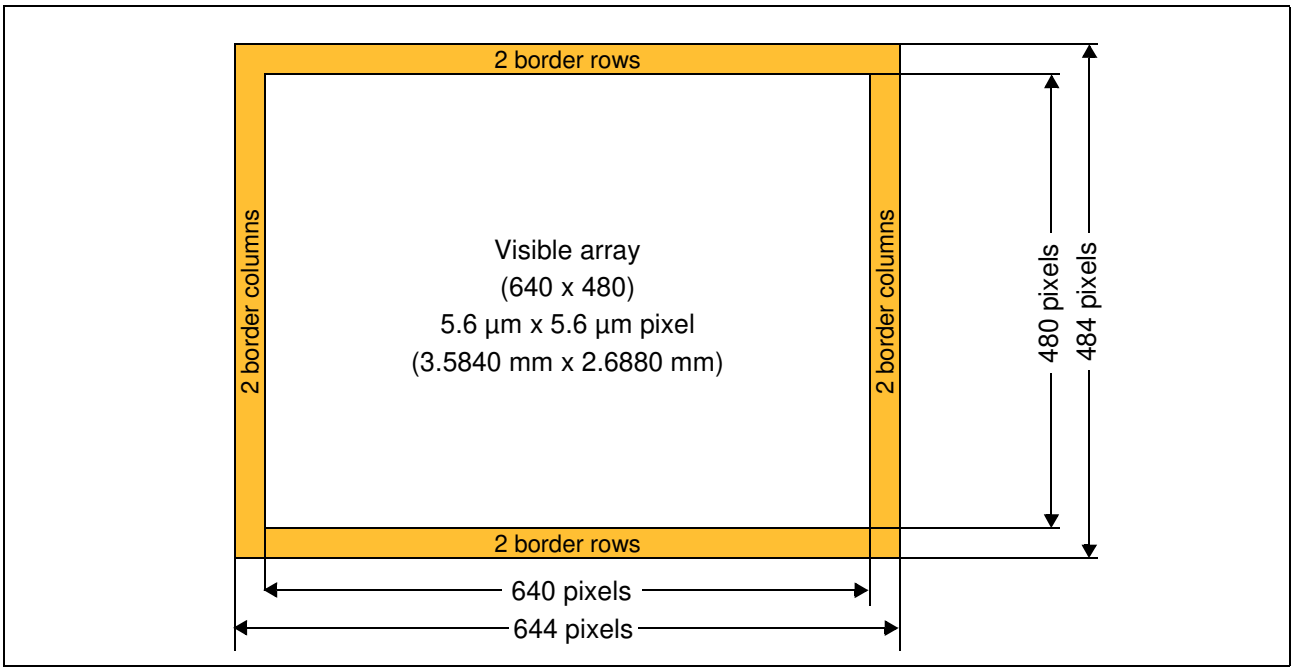
Figure 5: Overview of video block



2.1.2 Imaging array

The physical pixel array is 656 x 496 pixels. The pixel size is 5.6 µm by 5.6 µm. The image size is 644 x 484 pixels in VGA and 324 x 244 pixels in QVGA.

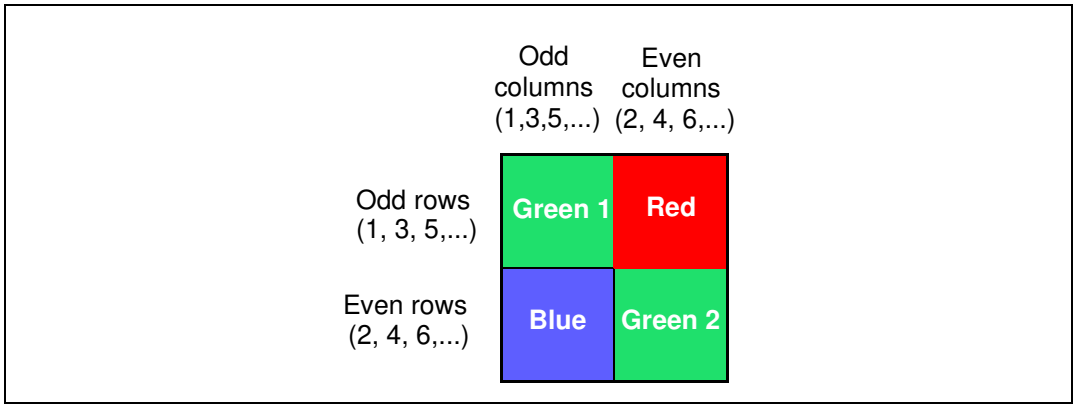
Figure 6: Pixel array interface diagram



2.1.3 Bayer colorization pattern

The image array is covered by a bayer colorization pattern as show in *Figure 7*.

Figure 7: Bayer colorization pattern



2.1.4 Microlenses

The device has microlenses on top of each pixel of the active array area, these micolenses improve the sensor sensitivity by refocusing light towards the sensing area of the pixel.

2.2 Image Formats

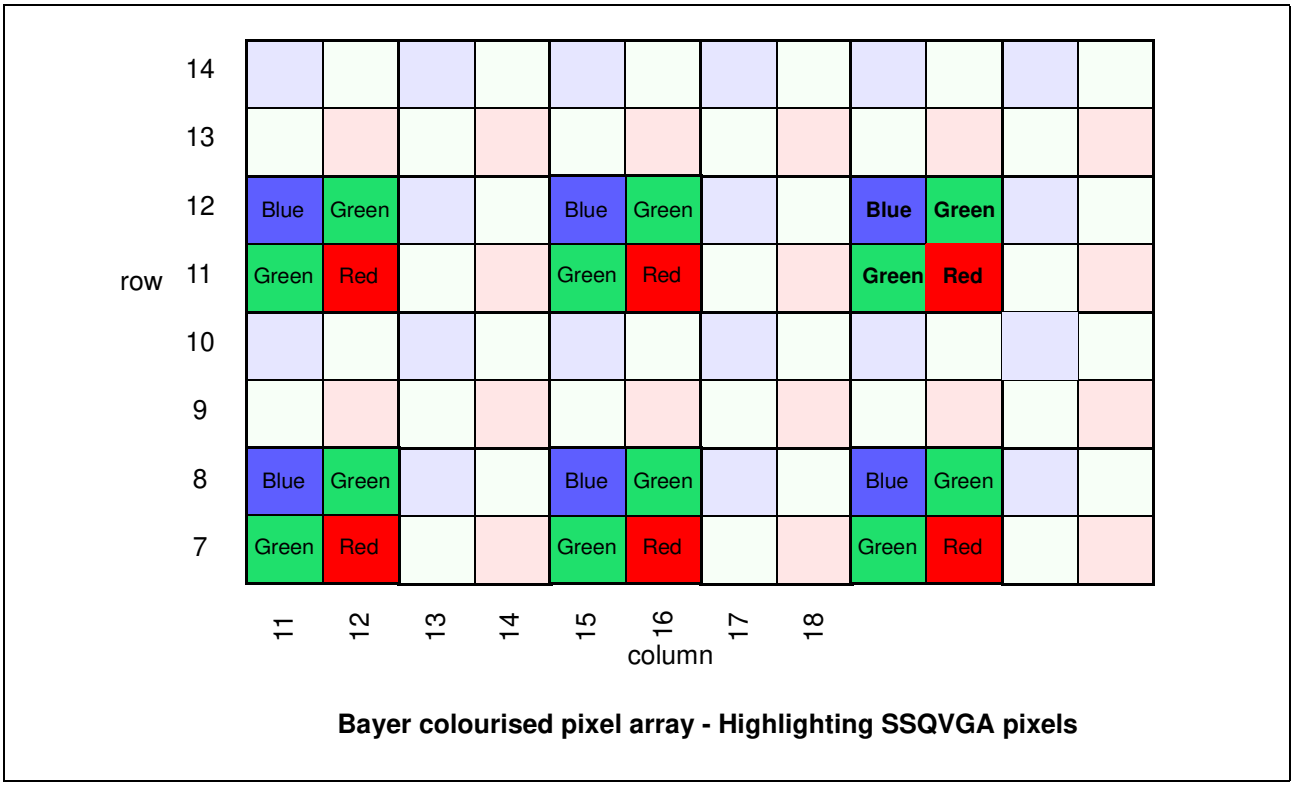
2.2.1 VGA Format

This is the default format and produces an output of 644 pixels by 484 pixels.

2.2.2 Sub-sampled QVGA format

In this mode the QVGA image is generated by sub-sampling the VGA image in groups of 4 to preserve the Bayer pattern with every second group of pixels and lines skipped as illustrated in *Figure 8*. Although the former would not necessarily apply to a monochrome sensor the same address sequence is preserved. Due to the crude nature of the sub-sampling, the resultant output image will be of inferior quality but contains full field of view and is intended as a preview option before switching to view the required scene region in more detail.

Figure 8: Sub-sampled QVGA image format



Bayer colourised pixel array - Highlighting SSQVGA pixels

2.2.3 Window Of Interest QVGA

In WOI mode the QVGA image is generated by cropping the VGA image. I2C registers 87, 88 and 90 allow the user to select the coordinate of the top left corner of the QVGA WOI within the VGA picture (an offsetof (0,0) means top left of the full VGA array). The default frame rate in this modeis twice that of the default VGA mode

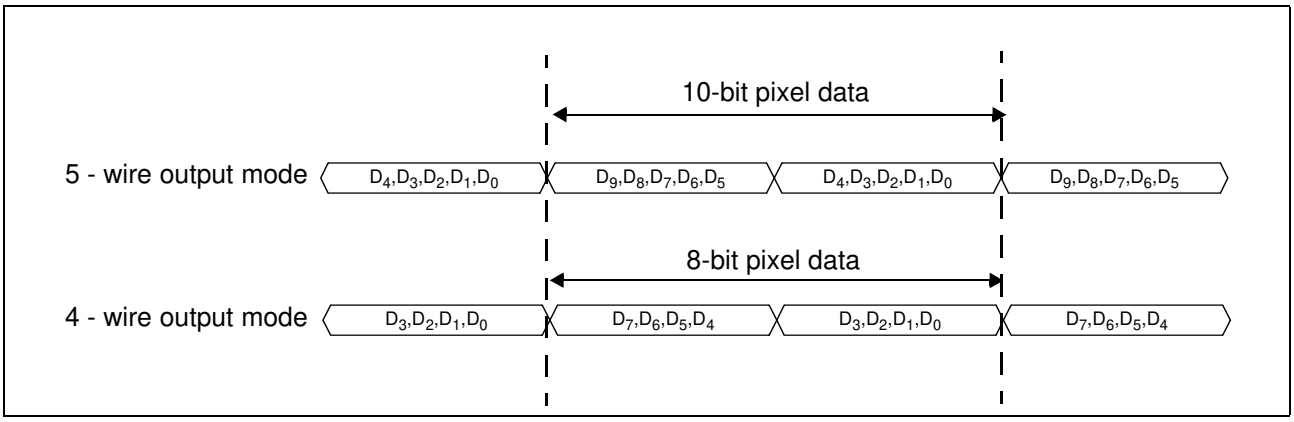
2.3 Data format

The video interface consists of a mono-directional, tri-stateable 5 wire data bus.

There are two data output modes controlled by serial register [23]

- **4- wire mode:** data is 8 bits per pixel, output as two 4-bit nibbles, most significant nibble first. In this mode a data qualification clock is also provided.
- **5-wire mode:** data is 10 bits per pixel, output as two 5-bit nibbles, most significant nibble first. , on 4 wires. In this mode there is NO qualification clock

Figure 9: Digital data output modes



2.3.1 QCLK Control

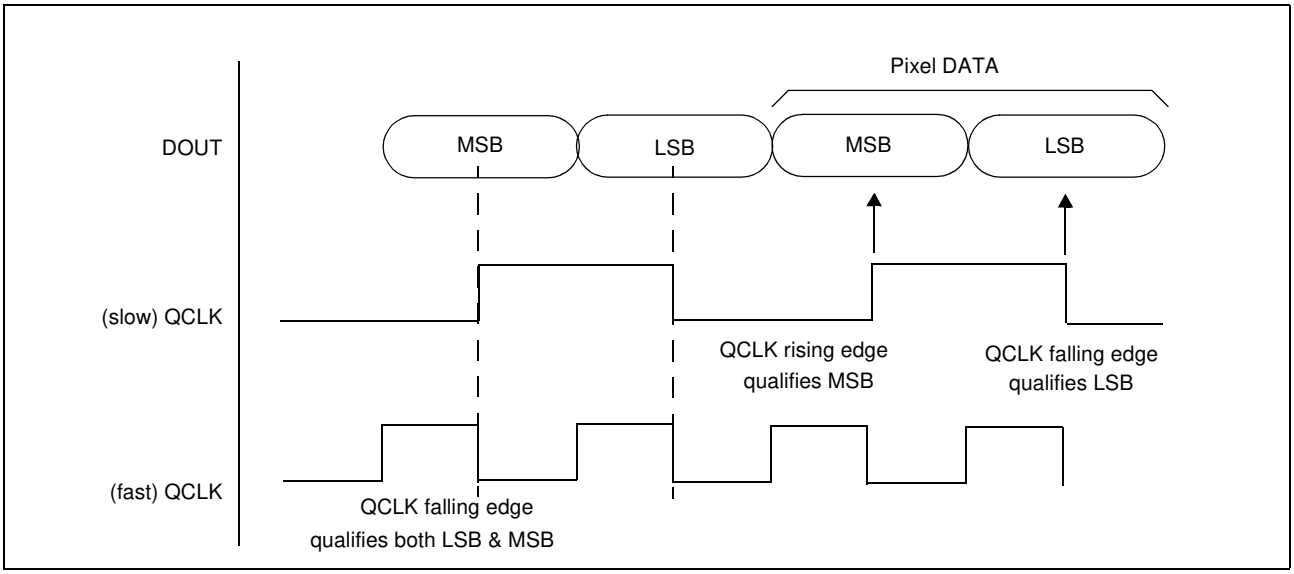
QCLK Type

The QCLK output (only available in 4-wire mode) may be one of two different types, controlled via serial register [20]

- **SLOW:** in this mode the rising edge of QCLK qualifies the MS nibble of each pixel and the falling edge of QCLK qualifies the LS nibble
- **FAST:** in this mode the falling edge of QCLK is used to qualify bith nibbles.

This is illustrated in *Figure 10* below;..

Figure 10: Pixel output timing



Frame-level position of QCLK signal

QCLK can operate in 2 different modes, selectable using register [20]

- **Free running**: in this mode, QCLK is runs continuously
- **Active only**: in this mode QCLK only qualifies the visible lines

2.3.2 Line format

The line format is shown in *Figure 11*. Each line starts with a Start of Active Video (SAV) sequence which consists of an escape sequence (FF-FF-00) followed by a single byte line code that identifies the line type and then two bytes containing the line number (with parity bits).

The line number format is shown in *Figure 12* and the line codes are described in *Section 2.3.3*.

Each line is terminated with an End of Active Video (EAV) sequence consisting of an escape sequence followed by the End of Line (EOL) code followed by the average value of the pixels on that line (repeated).

Following the EAV sequence there is a blanking period where the data is 0xFF. The length of this interline blanking period is shown in *Table 3 on page 12*.

Figure 11: Line format

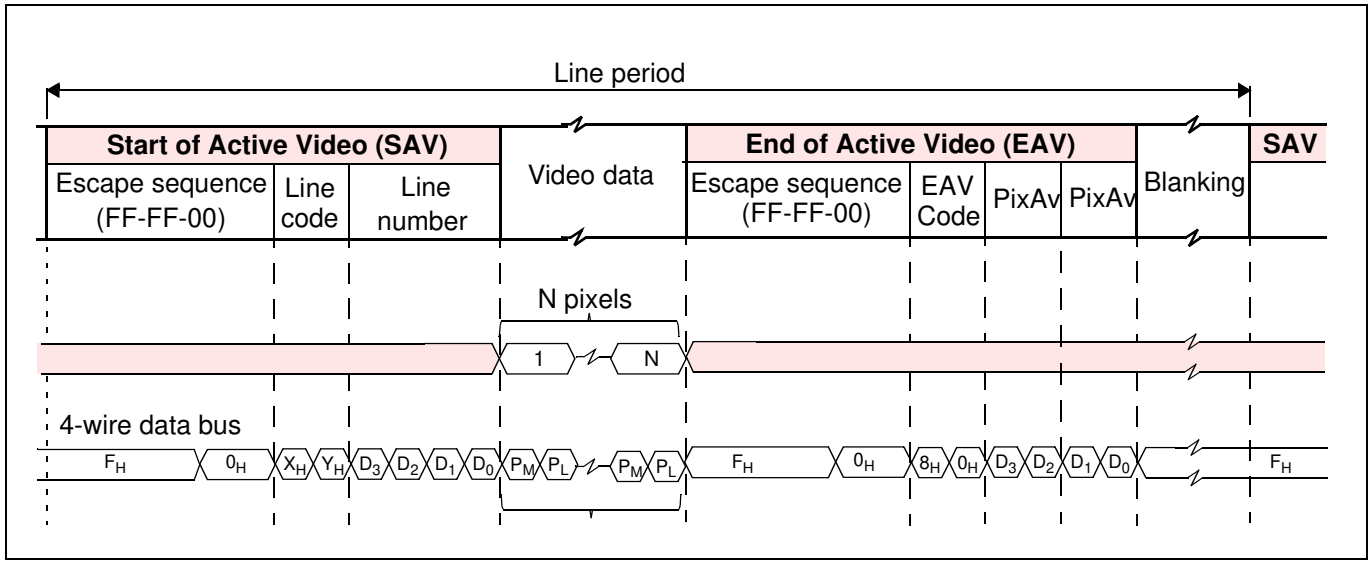
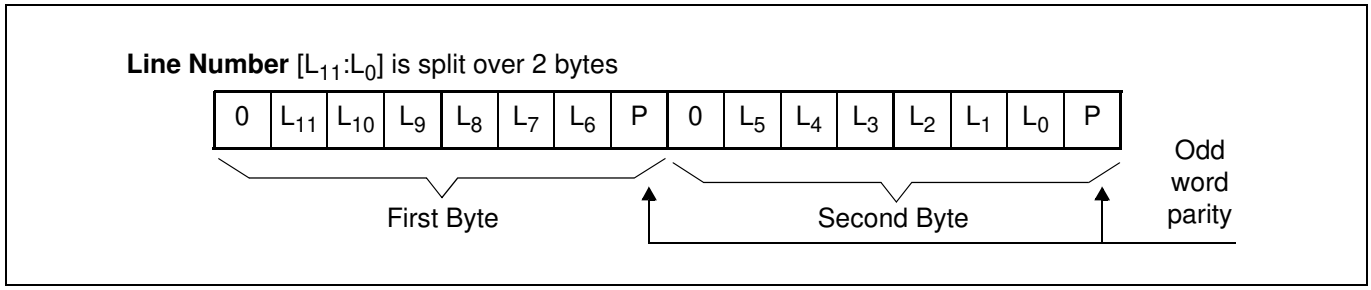


Figure 12: Line Number Data Format



2.3.3 Line Codes

All line codes are 8 bit numbers. When the 502 is in 5-wire mode ie outputting 10-bit pixel data then the codes are shifted left by 2 bits i.e. multiplied by 4.

Table 2: Line Codes

Line Type	Line Code
Start of Frame (SOF)	199 ($C7_H$)
Blank Line (BL)	157 ($9D_H$)
Dark line (DK)	171 (AB_H)
Visible Line (VL)	182 ($B6_H$)
End of Frame (EOF)	218 (DA_H)
End of Line (EOL)	128 (80_H)

2.3.4 Extending line length

The user can extend the line length by writing to serial registers 82 and 83. The line length padding is inserted after the EAV sequence, ensuring that the distance between the SAV and EAV sequences remains constant.

2.3.5 Line Timing

Table 3 lists the image durations and interline intervals in VGA and QVGA

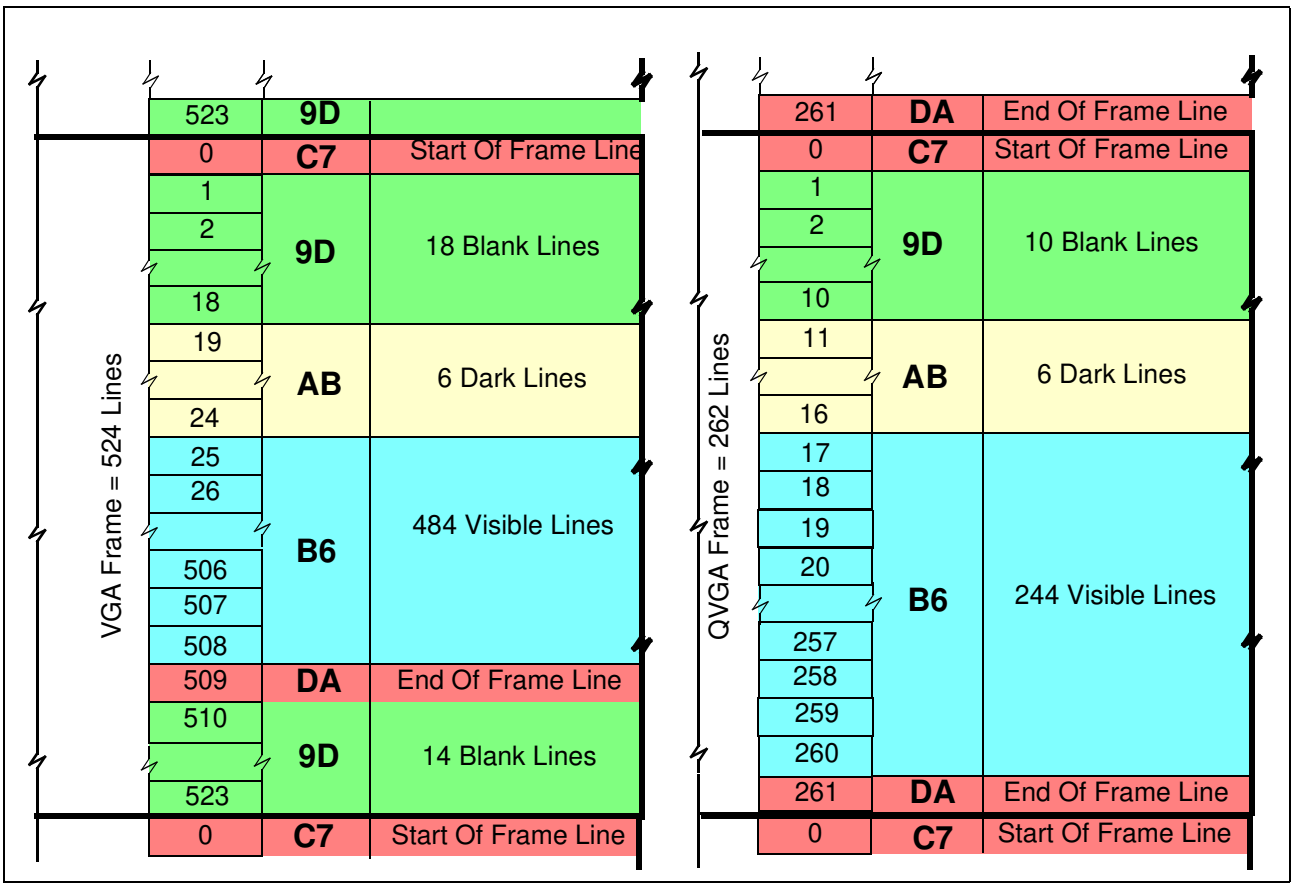
Table 3: Video mode line timing

Mode	QCK (MHz)	Image		Interline		Line total	
		QCKs	µs	QCKs	µs	QCKs	µs
VGA	12	644	53.6	118	9.8	762	63.5
QVGA	6	324	54	57	9.5	381	63.5
QVGA	12	324	27	57	4.75	381	31.75

2.3.6 Frame Format

Each frame is built as a sequence of lines, each line has an embedded line code.

Figure 13: Frame formats in VGA and QVGA modes



2.3.6.1 Start of Frame (SOF) line timing

The start of frame line at the beginning of each video frameframe contains status data. Please contact STMicroelectronics for details.

2.3.6.2 Blank lines

The blank lines contain blank bytes (07_H).

2.3.6.3 Dark lines

The dark line contains the dark calibrated values of the optically shielded lines. The average value is 16 when dark calibration is enabled.

2.3.6.4 End of frame line

The end of frame line at the end of each video frame contains no video data. Its sole purpose is to indicate the end of the active video portion of a frame.

2.3.6.5 Extending frame length

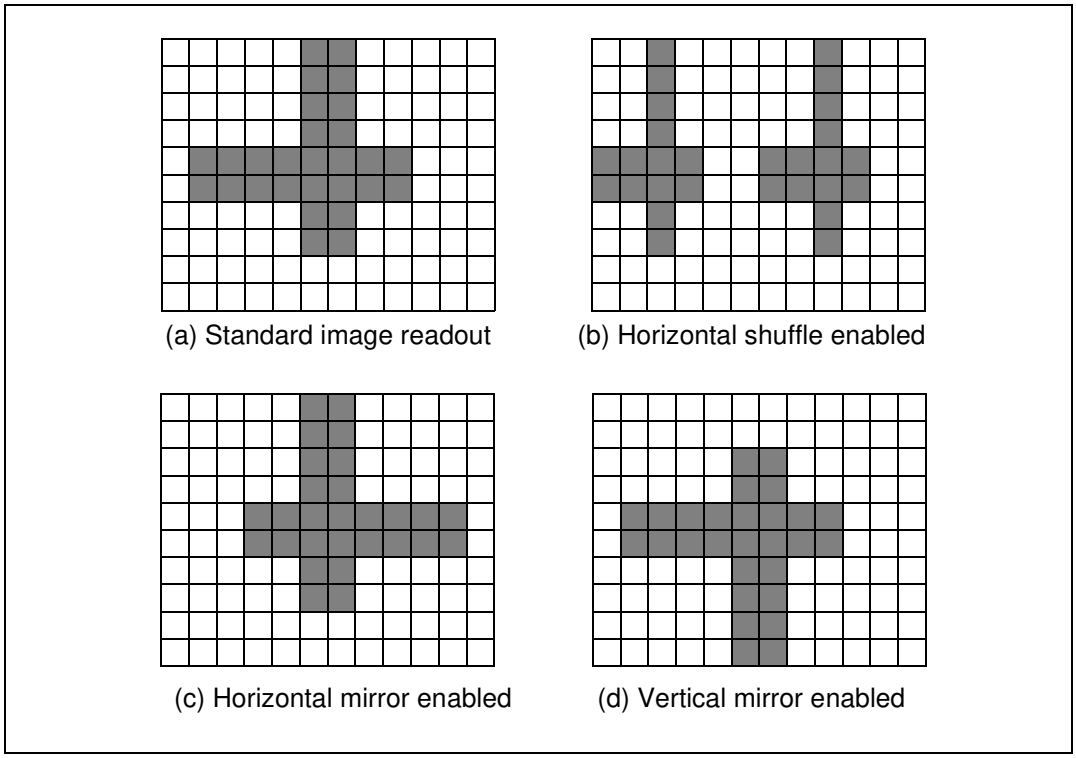
The user can extend the inter-frame period by increasing the frame length. This is achieved by writing to serial registers 97 and 98. In this event, the appropriate number of additional blank lines is inserted between the End Of frame (EOF) line and the Start Of Frame (SOF) line. This means that the distance between SOF and EOF remains constant.

2.3.7 Image translations

The imaging array can be readout with different modes as described here below:

- Shuffle horizontal readout, bit [7] of serial register [17]. Even columns (2,4,6.) are readout first.
- Mirror horizontal readout, bit [3] of serial register [22]. Columns are readout in reverse order.
- Mirror vertical readout, enabled by setting [4] of serial register [22]. Rows are readout in reverse order.

Figure 14: Image readout modes



2.3.8 Dark calibration

The VS6502 has an automatic dark calibration system which is used to set the black level of the output video data to 16. The VS6502 has special ‘dark’ pixel rows which have the same exposure setting as the visible lines but are shielded from incident light. The VS6502 uses these lines to calculate an offset which is then be applied to the video data AND to the dark lines themselves. In this case the mean value of the dark lines output will be 16.

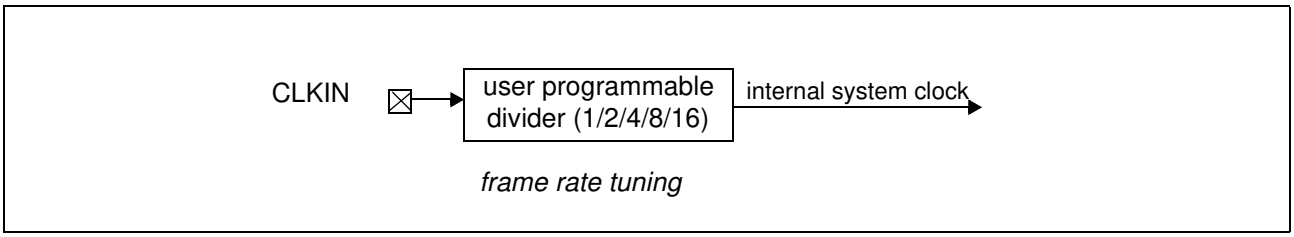
The measured dark line offsets are reported in registers [9] and [10]. By default these offsets are applied to the video data but a user may choose to apply no offset at all or their own offset which may be entered in registers [44] and [45] in 2’s complement format.

The dark calibration function is controlled via register [46].

2.3.9 Clock management and on-chip divider

The VS6502 has a built-in clock divider which acts on the input clock as shown in *Figure 15.* The clock divide ratio is controlled by register 37.

Figure 15: VS6502 clock divider



With the user programmable divider set to its default value of 1 (i.e. no divide), a 24 MHz input clock will generate the frame and pixel rates shown in *Table 4*.

Note: The VS6502 can operate with a maximun external clock frequency of 27 MHz.

Table 4: Default video frame rates

Video Mode	CLKIN (MHz)	Frame rate (Hz)	Pixel rate (MHz)
VGA	24	30	12
SSQVGA	24	60	6
WOIQVGA	24	60	6

For values of clock divider other than 1, the rates shown above can be divided accordingly.

These rates are based on the default line and frame lengths. If the user increases either of these then the frame rate will be reduced.

2.3.10 Exposure/gain control

The sensor does not contain any form of automatic exposure or gain control. To produce a correctly exposed image, exposure and gain values must be calculated externally and written to the sensor via the serial interface. This function is handled by ST co-processors.

Exposure calculation

The exposure time for a pixel and the ADC range (therefore the gain) are programmable via the serial interface. The explanation below assumes that the gain and exposure values are updated together as part of a 5 byte serial interface auto-increment sequence.

Exposure time combines coarse, fine exposure, pixel rate also related to frame and line lengths, all defined in *Table 5*.

Table 5: Definitions related to exposure

Frame length	Number of lines per frame [default=524] The frame length may be increased to 1023 by writing to the frame length register.
Line length	Number of pixels in a line [default = 762] The line length may be increased to 1023 by writing to the line length register.
Exposure	The pixel exposure time is determined by the course and fine exposure values
Coarse exposure value	The number of lines a pixel exposes for. Limited by frame length. Coarse exposure value is in the range [0 - (frame length -2)].
Fine exposure value	Number of additional pixel periods a pixel exposes for. Limited by line length. Fine exposure value is in the range [11 - (line length)].
Pixel period	Determined by the input clock frequency (Fclkin) and user clk_div setting. PixPeriod=(2*N)/Fclkin where N = clock divider ratio
Exposure time	PixPeriod x [($Coarse_{num\_lines}$ x $Line\_Length_{num\_pixels}$) + $Fine_{pixels}$]

Example of exposure calculation in default VGA video mode

coarse exposure = 522

fine exposure = 762

Input clock frequency - Fclkin = 24MHz,

Pixel period = $2/(24 \times 10^6) = 8.33 \times 10^{-8}$ s

Calculation: exposure time = 8.33×10^{-8} x [(522 x 762) +762] = 33.2 ms

The available range of exposure (without using clock division) is shown in *Table 6*.

Table 6: Exposure ranges [24MHz system clock]

Range	Coarse (no. lines)	Line length (no. pixels)	Fine (no. pixels)	Exposure	
				No. pixels	Time
Min.	0	762	11	0	0.92 µs
Max (default-VGA)	522	762	762	400,050	33.2 ms
Max (available)	1023	1023	1023	$1023^2 + 1023$	87.3 ms

2.3.11 Gain timing and exposure updates

Exposure and gain values are re-timed within the sensor to ensure that a new set of values is only applied to the sensor array at the start of each frame. The status register [2] shows is set high when a new exposure value is written via the serial interface but has not yet been applied to the sensor array.

There is a 1 frame latency between a new exposure value being applied to the sensor array and the results of the new exposure value being read-out. The same latency does not exist for the gain value. To ensure that the new exposure and gain values are aligned up correctly the sensor delays the application of the new gain value by one frame relative to the application of the new exposure value.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain settings, if the serial interface communication extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to any location in the exposure page of the serial interface register map. Thus, if the 5 bytes of exposure and gain data is sent as an auto-increment sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

2.4 Device operating modes

The VS6502 sensor has three main operating modes. The current mode of the device is reported in register [29].

2.4.1 Sleep Mode (also referred to as low power)

This is the default state of the sensor on power up. In this mode all analogue circuitry is powered down and there is no video output. All I2C registers are accessible (provided that a system clock is present).

2.4.2 Idle Mode

In this mode the analogue circuitry is powered up and the QCLK output is present. There is no video data output and the FST and LST signals remain low.

2.4.3 Run Mode

In this mode the device is fully operational and produces video output.

2.5 Mode Control

The VS6502 modes are controlled by two I2C registers:

- Register[16] - Setup0
- Register[28] - IDLE mode control

On power up, the VS6502 is in low-power mode and bit 0 of register [16] is set. Clearing this bit via the I2C interface causes the VS6502 to go directly into RUN mode and start producing video data.

Warning:Entering RUN mode directly from SLEEP does not give the analogue circuitry in the sensor enough time to stabilise before video data is produced. The first few frames of video data will not appear to be correctly exposed. For streaming video applications this may be perfectly acceptable but this could cause problems for systems which wish to capture and use the first video frame output from the sensor.

In order to guarantee a valid first video frame it is necessary to enter IDLE mode to allow the analogue circuitry to be powered on. The sensor must remain in IDLE mode for at least 10 ms.

IDLE mode may be entered from SLEEP mode as follows:

- set bits 0 and 1 of register[28]
- clear bit 0 of register[16]

The transition from IDLE to RUN is now controlled by bit 1 of register[28].

The first video frame will appear (along with the first FST pulse) one exposure time after the sensor goes into RUN mode.

Note: The default value of exposure is maximum (ie 1/30th second) but may be changed as required.

2.5.1 Standby mode (CHIPEN high)

Standby mode is entered asynchronously by driving the CHIPEN pin high. In this mode the analogue blocks of the sensor are powered down and the video timing logic is reset with all data lines driven high.The external sensor clock is gated and no I2C communication is possible. To achieve absolute minimum power consumption, the external clock should be switched off. During standby mode the register contents are preserved.

2.5.2 Sensor reset via the serial interface

It is possible to completely reset the VS6502 via the serial interface by setting bit 1 of the SETUP0 register. This will reset all the VS6502 registers.

3 Serial Control Bus

3.1 General description

The 2-wire I2C serial interface bus is used to read and write the sensor control registers.

Some status registers are read-only.

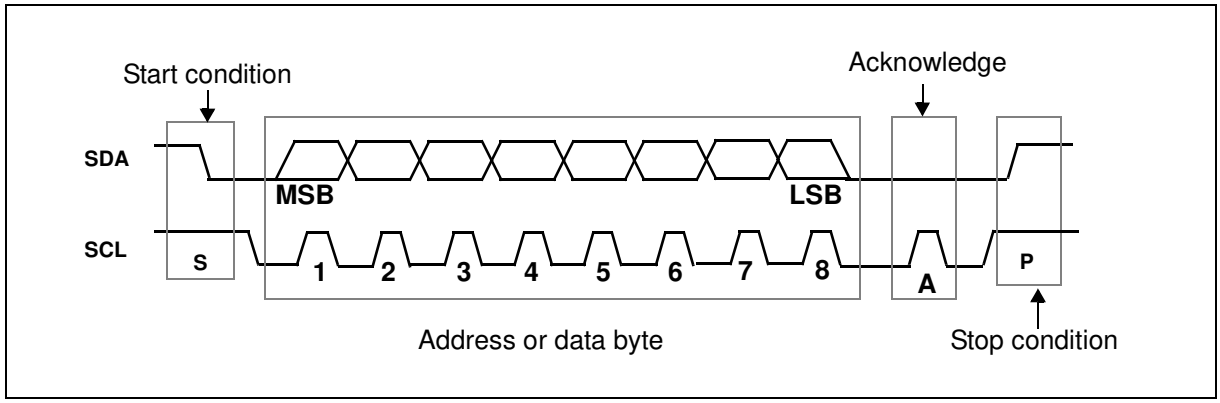
The main features of the serial interface include:

- Variable length read/write messages
- Indexed addressing of information source or destination within the sensor
- Automatic update of the index after a read or write message
- Message abort with negative acknowledge from the master
- Byte oriented messages

3.2 Serial communication protocol

The co-processor must perform the role of communication ‘master’ and the sensor acts as a ‘slave’. The communication from host to sensor takes the form of 8-bit data with a maximum serial clock frequency of 100 kHz. Since the serial clock is generated by the bus master it determines the data transfer rate. Data transfer protocol on the bus is illustrated in *Figure 16*.

Figure 16: Serial Interface data transfer protocol



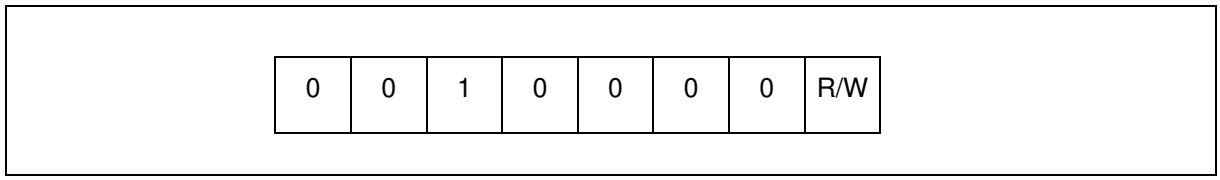
3.2.1 Data format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling *sda* at a rising edge of *scl*. The external data must be stable during the high period of *scl*. Exceptions to this are *start* (S) or *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

A message contains at least two bytes preceded by a *start* condition and followed by either a *stop* or *repeated start, (Sr)* followed by another message.

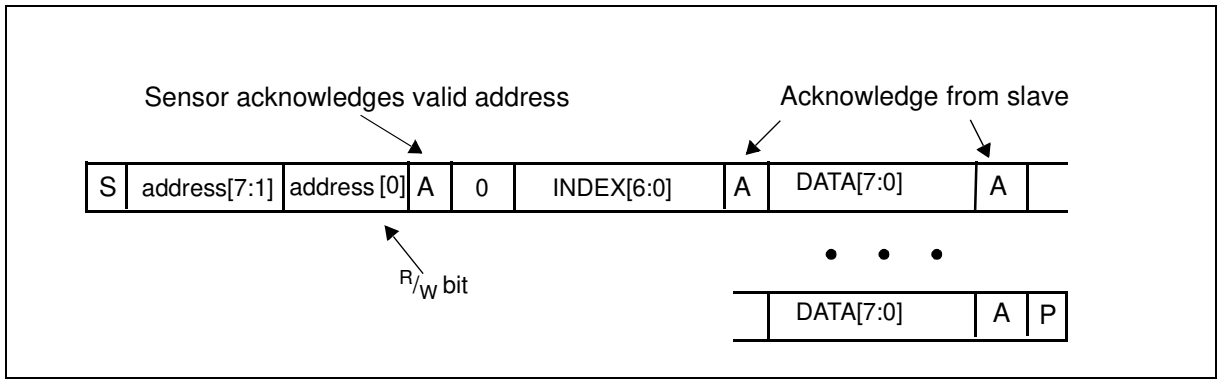
The first byte contains the device address byte which includes the data direction *read,* (r)*, ~write*, (~w), bit.

Figure 17: VS502 Serial interface address



The byte following the address byte contains the address of the first data byte (also referred to as the *index*). The serial interface can address up to 128 byte registers.

Figure 18: Serial interface data format



3.2.2 Message interpretation

All serial interface communications with the sensor must begin with a *start* condition. If the *start* condition is followed by a valid address byte then further communications can take place. The sensor will acknowledge the receipt of a valid address by driving the *sda* wire low. The state of the *read/~write* bit (LSB of the address byte) is stored and the next byte of data, sampled from *sda,* can be interpreted.

During a write sequence the second byte sent to the sensor is an index and is used to point to one of the internal registers.

The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition or sends a *repeated start (Sr)*.

As data is received by the slave, it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the current index is read out in the byte following the device address byte. The next byte read from the slave device includes the contents of the register addressed by the current index. The contents of this register are then parallel loaded into the serial/parallel register and clocked out of the device by *scl.*

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. Although VS6502 is always considered to be a slave device, it acts as a transmitter when the bus master requests a read from the sensor.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

3.3 Types of messages

This section gives guidelines on the basic operations to read data from and write data to the serial interface.

The serial interface supports variable length messages. A message may contain no data bytes, one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available is detailed below.

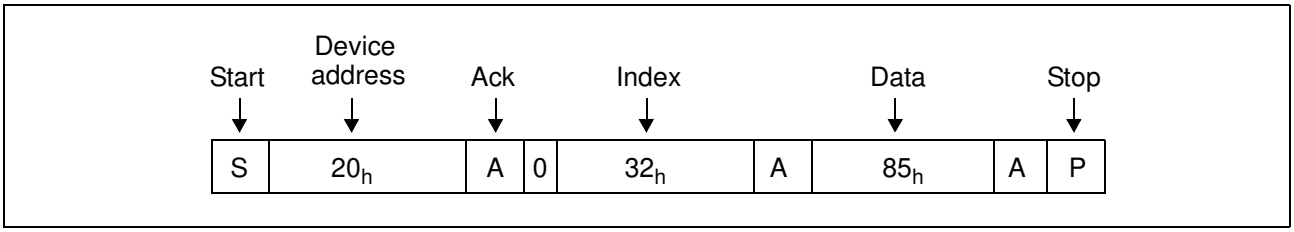
- No data writes are used to set the index for a subsequent read message.
- Multiple location writes may be used for fast information transfers.

Examples of these operations are given below. A full description of the internal registers is given in *Chapter 4*. For all examples, the slave address used is 0x20 for writing and 0x21 for reading. The write address includes the read/write bit (the LSB) set to zero while this bit is set in the read address.

3.3.1 Single location, single data write

When a single value is written to the sensor, the message looks as shown in *Figure 19*.

Figure 19: Single location, single write

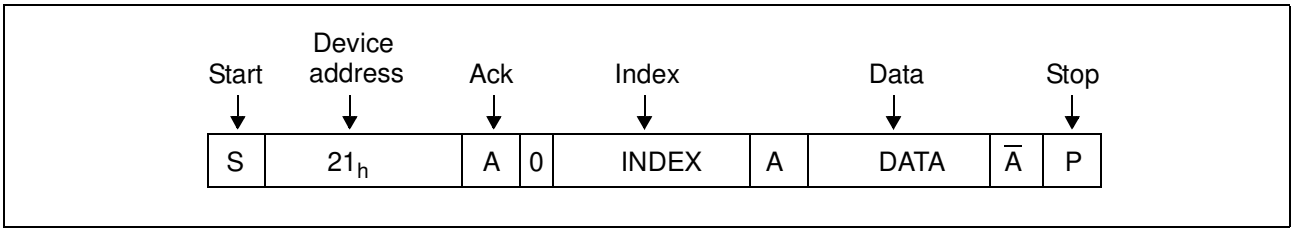


In this example, the register with index = 32 is set to 85. The index value is preserved in the sensor and may be used by a subsequent read. The write message is terminated with a stop condition from the master.

3.3.2 Single location, single data read

During a read sequence the sensor always sends the index used to get the first byte of data before sending the data itself. The index can only be set by a write message.

Figure 20: Single location, single read

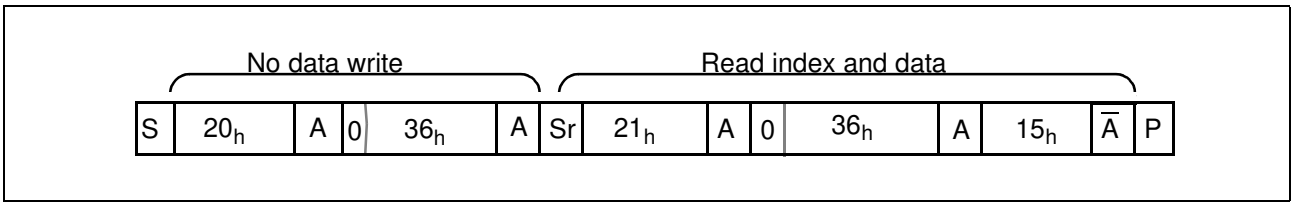


3.3.3 No data write followed by same location read

When a location is to be read and the value of the stored index is not known, a write message with no data byte must be written first in order to set the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master, a repeated start

condition is asserted between the write and read messages.
In this example, the *gain* value (index = 36_{10}) is read as 15_{10} (see *Figure 21*).

Figure 21: No data write followed by same location read

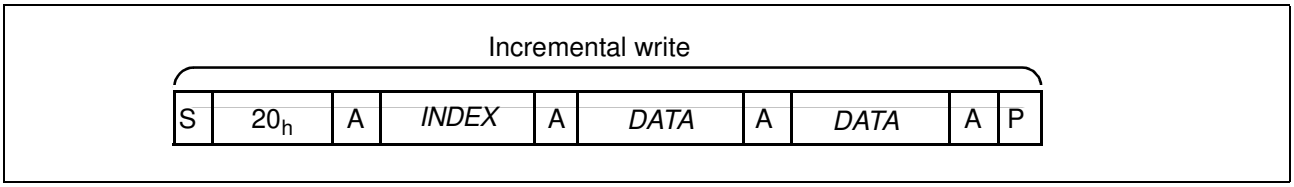


As in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

3.3.4 Multiple location write

It is possible to write data bytes to consecutive internal registers without having to send explicit indexes prior to sending each data byte. After sending the first data byte, the master sends an acknowledge followed by the next byte and so on as shown in *Figure 22*.

Figure 22: Multiple location write

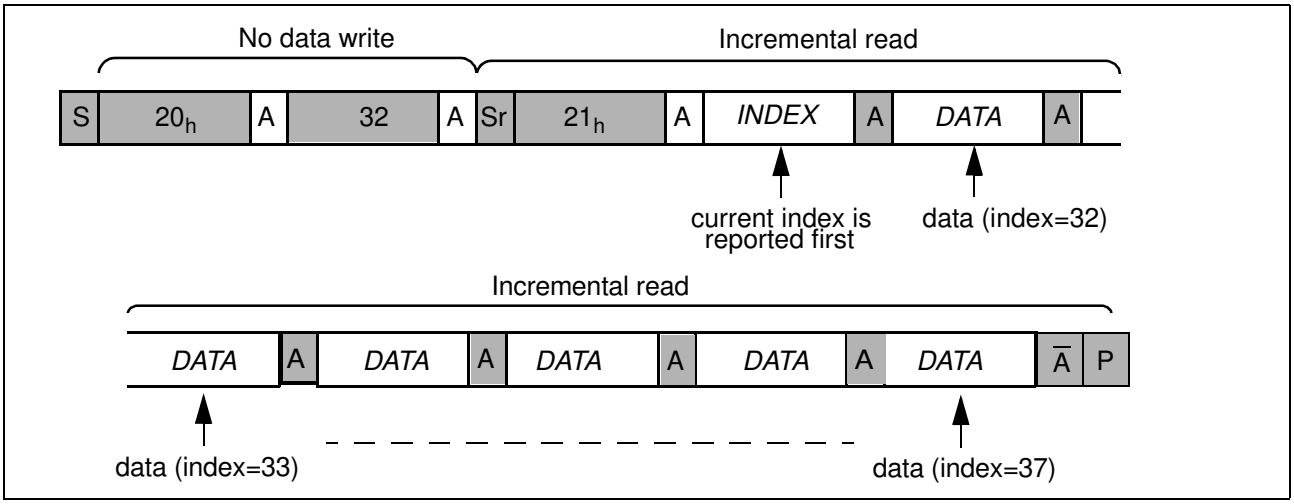


3.3.5 Multiple location read

In the same manner as writing, multiple locations can be read with a single read message. In this example a no data write is performed first in order to set the required index and then six consecutive indexes are read. After each data byte is received the master issues an acknowledge (ACK).

After the last required byte is received, the master issues a negative acknowledge (NACK) followed by a stop condition to terminate the transaction.

Figure 23: Multiple location read



4 I²C Register Description

4.1 Register summary

The 8-bit registers within the sensor are accessible via the serial interface. Registers are grouped according to their function. The primary register groups for the VS6502 are:

- Status registers
- Setup registers with bit significant functions
- Exposure register for parameters that influence the output image brightness
- Format registers

Some registers are Read Only (RO), all others are readable and writable (R/W).

Table 7: Serial interface address map

Index	Name	Length	Type	Comments
Status registers				
0	deviceH	8	RO	Chip identification number including revision indicator (502 Rev0).
1	deviceL	8	RO	
2	status0	8	RO	User can determine whether timed serial interface data has been consumed by interrogating flag states
9	dark_avgH	4	RO	This is the average pixel value returned from the dark line offset cancellation algorithm (2's complement notation)
10	dark_avgL	8	RO	
14	frame counter	8	RO	Current frame number (0 to 255)
Setup registers				
16	setup0	8	R/W	Low-power & video timing
17	Shuffle	8	R/W	Shuffle
20	fg_modes	8	R/W	Frame grabbing modes (FST and QCK)
22	shuffle/mirror	8	R/W	Read-out order of data
23	op_format	7	R/W	Output coding formats
28	IDLE mode control	2	R/W	IDLE mode control register
29	Mode State	3	RO	Reports current mode
Exposure registers				
32	fineH	2	R/W	Fine exposure
33	fineL	8	R/W	
34	coarseH	2	R/W	Coarse exposure
35	coarseL	8	R/W	
36	analogue gain	4	R/W	Analogue gain setting

Table 7: Serial interface address map

Index	Name	Length	Type	Comments
37	clk_div	4	R/W	Clock division
44	dark offsetH	3	R/W	Dark line offset cancellation value (2's complement notation)
45	dark offsetL	8	R/W	
46	dark offset setup	3	R/W	Dark line offset cancellation enable
Video format registers - [82-98]				
82	line_lengthH	2	R/W	Line Length (pixel clocks)
83	line_lengthL	8	R/W	
87	x-offsetH	1	R/W	WOI X offset
88	x-offsetL	8	R/W	
90	y-offsetL	8	R/W	WOI Y offset
97	frame_lengthH	2	R/W	Frame length (Lines)
98	frame_lengthL	8	R/W	

4.2 Status registers

4.2.1 [0-1] - DeviceH and DeviceL

These registers provide read only information to identify the sensor type that has been coded as a 12-bit number and a 4-bit mask set revision identifier. The device identification number for VS6502 is 502 (0001 1111 0110_2). The initial mask revision identifier is 0 (0000_2).

Table 8: [0] - DeviceH

Bits	Function	Value	Comment
[7:0]	Device type identifier	1F	Most significant 8 bits of the 12 bit code identifying the chip type.

Table 9: [1] - DeviceL

Bits	Function	Value	Comment
[7:4]	Device type identifier	6	Least significant 4 bits of the 12 bit code identifying the chip type.
[3:0]	Mask set revision identifier	1	

4.2.2 [2] - Status0

Table 10: [2] - Status0

Bits	Function	Default	Comment
[7]	Video timing parameter update pending flag	0	Video timing parameters sent but not yet consumed by sensor
[4]	Odd/even frame	1	The flag will toggle state on alternate frames
[3]	Clock division update pending	0	Clock divisor sent but not yet consumed by the sensor
[2]	Gain value update pending	0	Gain value sent but not yet consumed by the sensor
[1]	Coarse exposure value update pending	0	Coarse exposure value sent but not yet consumed by the sensor
[0]	Fine exposure value update pending	0	Fine exposure value sent but not yet consumed by the sensor

4.2.3 [9-10] - Dark Average

Table 11: [9-10] - Dark_Avg

Regiter index	Bits	Function	Default	Comment
9	[2:0]	Dark average ms bits	-	The calculated pixel average over a series of dark lines. The pixel sample size from each dark line will be image size dependent up to a maximum of 256
10	[7:0]	Dark average lsb	-	

4.2.4 [14] - Frame Counter

Table 12: [14] - Frame Counter

Regiter index	Bits	Function	Default	Comment
14	[7:0]	Frame count	0	Increments by 1 each frame