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WM8734

Stereo Audio CODEC

DESCRIPTION

The WM8734 is a low power stereo CODEC ideal for DVD/RW, MP3, media centre and automotive applications

Stereo line inputs are provided, along with a mute function and programmable line level volume control.

Stereo 24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters.

Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported.

Stereo audio line level outputs are provided along with anti-thump mute and power up/down circuitry.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including level controls, mutes, de-emphasis and power management facilities. The device is available in a 20-lead SSOP package.

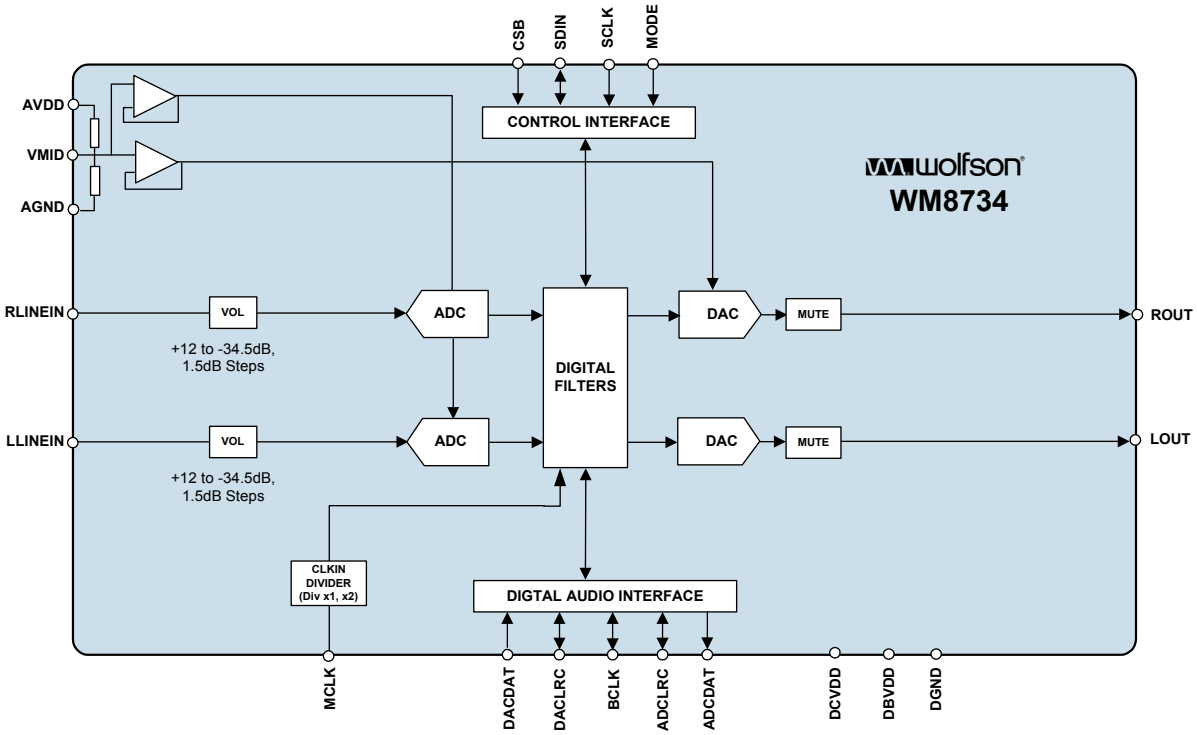
FEATURES

- Audio Performance
  - 90dB SNR ('A' weighted @ 48kHz) ADC
  - 100dB SNR ('A' weighted @ 48kHz) DAC
  - 2.7 – 3.6V Digital Supply Operation
  - 2.7 – 3.6V Analogue Supply Operation
- ADC and DAC Sampling Frequency: 8kHz – 96kHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
  - Master or Slave Clocking Mode
- Stereo Audio Inputs and Outputs
- 20-lead SSOP Package

APPLICATIONS

- CD and Minidisc Recorder
- MP3 Player / Recorder

BLOCK DIAGRAM



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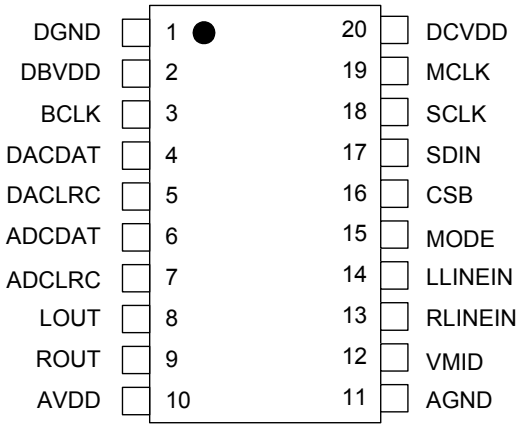
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
XWM8734EDS/V	-40 to +85°C	20-lead SSOP (Pb-free)	MSL3	260°C
XWM8734EDS/RV	-40 to +85°C	20-lead SSOP (Pb-free tape and reel)	MSL3	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DGND	Ground	Digital GND
2	DBVDD	Supply	Digital Buffers VDD
3	BCLK	Digital Input/Output	Digital Audio Bit Clock, Pull Down, (see Note 1)
4	DACDAT	Digital Input	DAC Digital Audio Data Input
5	DACLRC	Digital Input/Output	DAC Sample Rate Left/Right Clock. Pull Down (see Note 1)
6	ADCDAT	Digital Output	ADC Digital Audio Data Output
7	ADCLRC	Digital Input/Output	ADC Sample Rate Left/Right Clock, Pull Down (see Note 1)
8	LOUT	Analogue Output	Left Channel Line Output
9	ROUT	Analogue Output	Right Channel Line Output
10	AVDD	Supply	Analogue VDD
11	AGND	Ground	Analogue GND
12	VMID	Analogue Output	Mid-rail reference decoupling point
13	RLINEIN	Analogue Input	Right Channel Line Input (AC coupled)
14	LLINEIN	Analogue Input	Left Channel Line Input (AC coupled)
15	MODE	Digital Input	Control Interface Selection, Pull Up (see Note 1)
16	CSB	Digital Input	3-Wire MPU Chip Select / 2-Wire MPU interface address selection, active low, Pull up (see Note 1)
17	SDIN	Digital Input/Output	3-Wire MPU Data Input / 2-Wire MPU Data Input
18	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
19	MCLK	Digital Input	Master Clock Input (MCLK)
20	DCVDD	Supply	Digital Core VDD

Note:

1. Pull Up/Down only present when Control Register Interface ACTIVE = 0 to conserve power.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. The digital supply core voltage (DCVDD) must always be less than or equal to the analogue supply voltage (AVDD)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		2.7		3.6	V
Digital supply range (Buffer)	DBVDD		2.7		3.6	V
Analogue supply range	AVDD		2.7		3.6	V
Ground	DGND, AGND			0		V
Total analogue supply current	IAVDD	DCVDD, DBVDD, AVDD = 3.3V		16		mA
Digital supply current	IDCVDD, IDBVDD	DCVDD, DBVDD AVDD = 3.3V		8		mA
Standby Current Consumption				5		uA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DBVDD	V
Input HIGH level	V_{IH}		0.7 x DBVDD			V
Output LOW	V_{OL}				0.10 x DBVDD	V
Output HIGH	V_{OH}		0.9 x DBVDD			V
Power On Reset Threshold (DCVDD)						
DCVDD Threshold On -> Off	V_{th}			0.9		V
Hysteresis	V_{IH}			0.3		V
DCVDD Threshold Off -> On	V_{OL}			0.6		V
Analogue Reference Levels						
Reference voltage	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω
Line Input to ADC						
Input Signal Level (0dB)	V_{INLINE}			1.0 AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,2,3)	SNR	A-weighted, 0dB gain @ fs = 48kHz	85	90		dB
		A-weighted, 0dB gain @ fs = 96kHz		90		
		A-weighted, 0dB gain @ fs = 48kHz, AVDD = 2.7V		88		
Dynamic Range (Note 3)	DNR	A-weighted, -60dB full scale input	85	90		dB
Total Harmonic Distortion	THD	-1dB input, 0dB gain		-84	-74	dB
Power Supply Rejection Ratio	PSSR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		
ADC channel separation		1kHz input		90		dB
Programmable Gain		1kHz input Rsource < 50Ω	-34.5	0	+12	dB
Programmable Gain Step Size		Guaranteed Monotonic		1.5		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INLINE}	0dB gain	20k	30k		Ω
		12dB gain	10k	15k		
Input Capacitance	C_{INLINE}			10		pF

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line Output for DAC Playback Only (Load = 47kΩ. 50pF)						
0dBfs Full scale output voltage		At LINE outputs		1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,2,3)	SNR	A-weighted, @ fs = 48kHz	95	100		dB
		A-weighted @ fs = 96kHz		98		
		A-weighted, @ fs = 48kHz, AVDD = 2.7V		98		
Dynamic Range (Note 3)	DNR	A-weighted, -60dB full scale input	85	95		dB
Total Harmonic Distortion	THD	1kHz, 0dBfs		-88	-80	dB
		1kHz, -3dBfs		-92		
Power Supply Rejection Ratio	PSSR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		
DAC channel separation		1kHz, 0dB		100		dB

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with the input short circuited, measured 'A' weighted over a 20Hz to 20kHz bandwidth using an Audio analyser.
2. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
3. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attentuation (dB) – Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple – Any variation of the frequency response in the pass-band region.

POWER CONSUMPTION (EXAMPLES)

MODE DESCRIPTION	POWEROFF	OUTPD	DACPD	ADCPD	LINEINPD	CURRENT CONSUMPTION TYPICAL			
						AVDD (3.3V)	DCVDD (1.5V)	DBVDD (3.3V)	UNITS
Record and Playback	0	0	0	0	0	12.2	3.2	0.07	mA
Playback Only	0	0	0	1	1	3.3	2.3	0.07	mA
Record Only	0	1	1	0	0	9.2	2.6	0.07	mA
Standby (clock running)	0	1	1	1	1	16	77	65	μA
Standby (clock stopped)		1	1	1	1	16	0.3	0.2	μA
Power Down (clock running)	1	1	1	1	1	0.3	77	65	μA
Power Down (clock stopped)	1	1	1	1	1	0.3	0.3	0.3	μA

Notes:

1. The data presented here was measured with the audio interface in slave mode (MS = 0)
2. All figures are quiescent, with no signal.

MASTER CLOCK TIMING

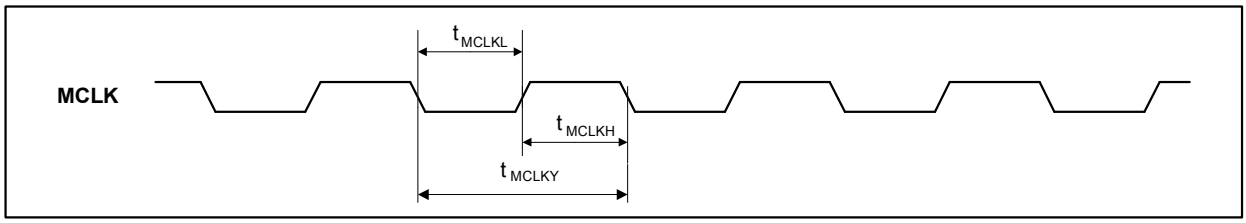


Figure 1 System Clock Timing Requirements

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK System clock pulse width high	T_{XTIH}		18			ns
MCLK System clock pulse width low	T_{XTIL}		18			ns
MCLK System clock cycle time	T_{XTIY}		54			ns
MCLK Duty cycle			40:60		60:40	

DIGITAL AUDIO INTERFACE – MASTER MODE

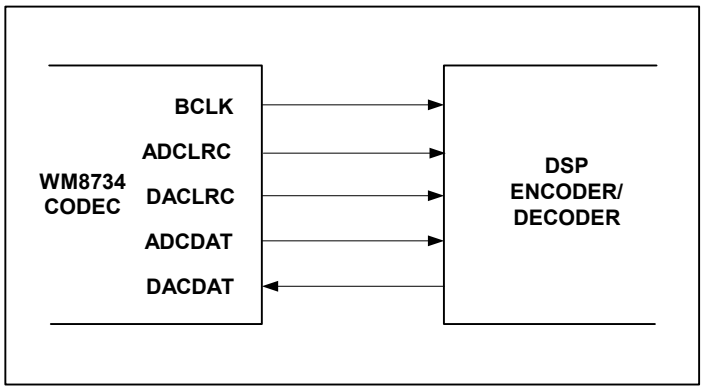


Figure 2 Master Mode Connection

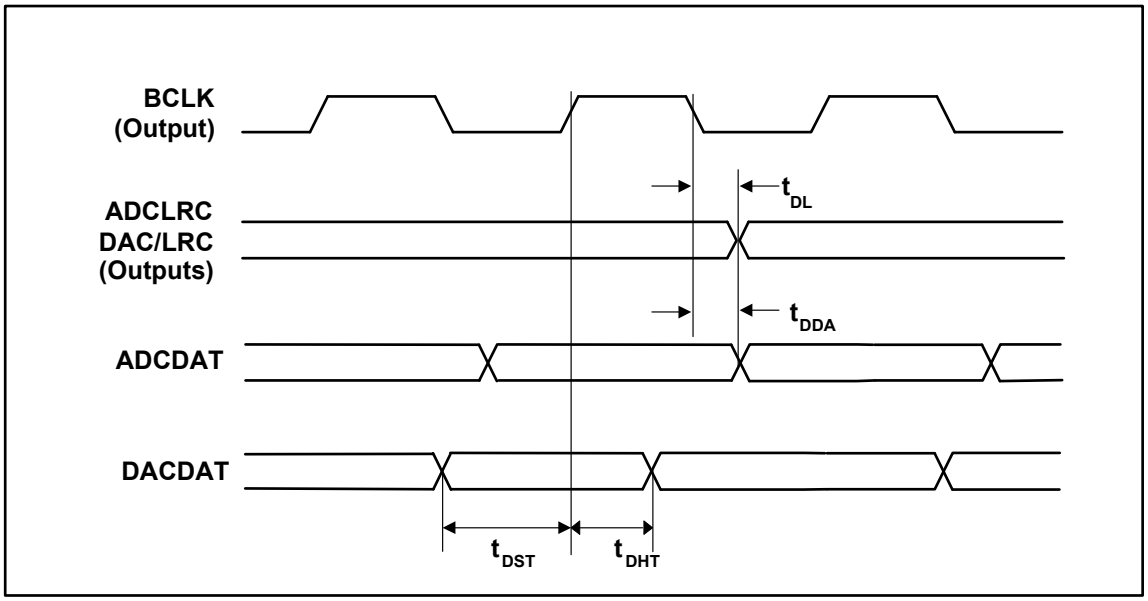


Figure 3 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCLRC/DACLRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}		0		15	ns
DACDAT setup time to BCLCK rising edge	t_{DST}		10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}		10			ns

DIGITAL AUDIO INTERFACE – SLAVE MODE

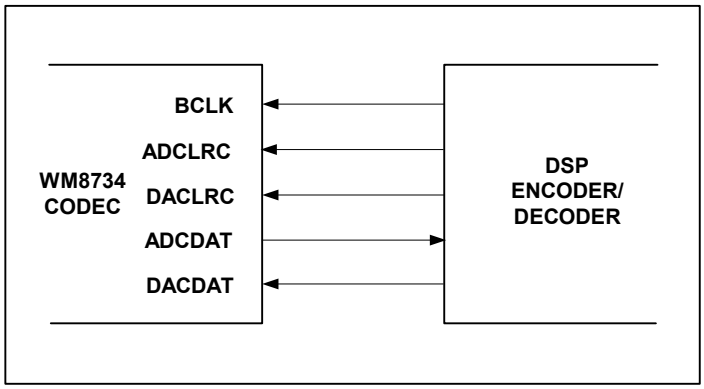


Figure 4 Slave Mode Connection

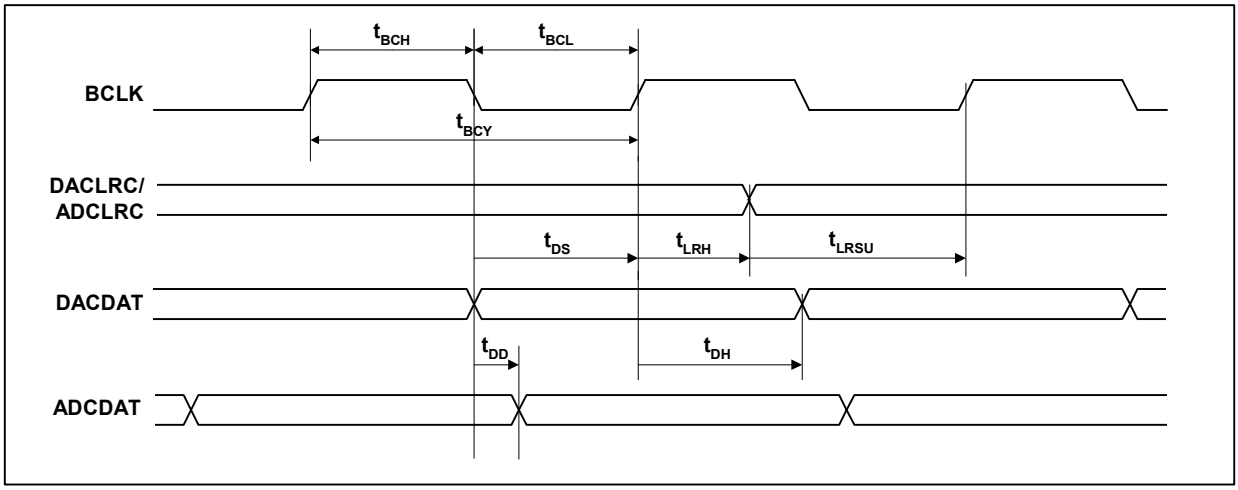


Figure 5 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
DACLRC/ADCLRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
DACLRC/ADCLRC hold time from BCLK rising edge	t_{LRH}		10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}		10			ns
DACDAT hold time from BCLK rising edge	t_{DH}		10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}		0		10	ns

MPU INTERFACE TIMING

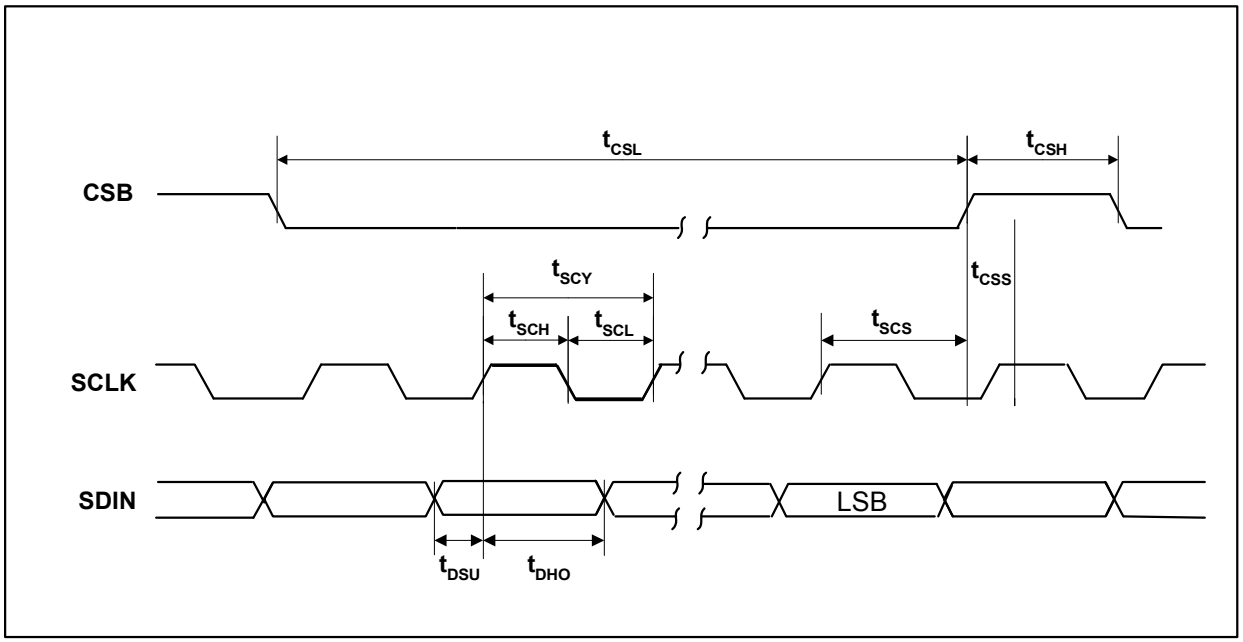


Figure 6 Program Register Input Timing – 3-Wire MPU Serial Control Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	t_{SCS}		60			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		20			ns
SCLK pulse width high	t_{SCH}		20			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
CSB pulse width low	t_{CSL}		20			ns
CSB pulse width high	t_{CSH}		20			ns
CSB rising to SCLK rising	t_{CSS}		20			ns

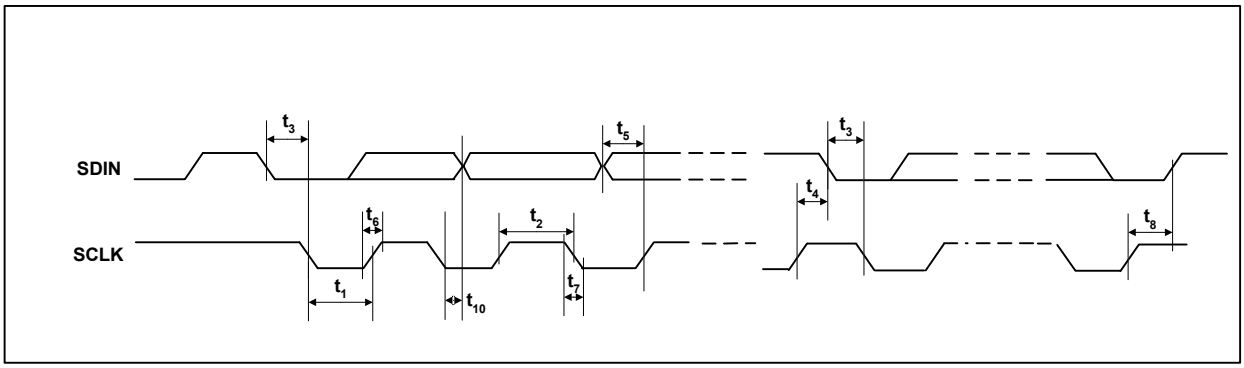


Figure 7 Program Register Input Timing – 2-Wire MPU Serial Control Mode

Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK Frequency			0		526	kHz
SCLK Low Pulsewidth	t_1		1.3			us
SCLK High Pulsewidth	t_2		600			ns
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
Data Setup Time	t_5		100			ns
SDIN, SCLK Rise Time	t_6				300	ns
SDIN, SCLK Fall Time	t_7				300	ns
Setup Time (Stop Condition)	t_8		600			ns
Data Hold Time	t_{10}				900	ns

DEVICE DESCRIPTION

The WM8734 is a high performance audio CODEC designed specifically for audio applications that require recording and playback features.

The CODEC includes line inputs to the on-board ADC, line outputs from the on-board DAC, a configurable digital audio interface and a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The CODEC includes a stereo low noise input. Line inputs have +12dB to -34dB logarithmic volume level adjustments and mute. All the required input filtering is contained within the device.

The on-board stereo analogue to digital converter (ADC) is of a high quality using a multi-bit high-order oversampling architecture delivering optimum performance with low power consumption. The output from the ADC is available on the digital audio interface. The ADC includes an optional digital high pass filter to remove unwanted dc components from the audio signal.

The on-board digital to analogue converter (DAC) accepts digital audio from the digital audio interface. Digital filter de-emphasis at 32kHz, 44.1kHz and 48kHz can be applied to the digital data under software control. The DAC employs a high quality multi-bit high-order oversampling architecture to again deliver optimum performance with low power consumption.

Special techniques allow the audio to be muted and the device safely placed into standby, sections of the device powered off and volume levels adjusted without any audible clicks, pops or zipper noises. Therefore standby and power off modes may be used dynamically under software control, whenever recording or playback is not required.

The device caters for a number of different sampling rates including industry standard 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz. The digital filters used for both record and playback are optimised for each sampling rate used.

The digitised output is available in a number of audio data formats I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified. The digital audio interface can operate in both master or slave modes.

The software control uses either a 2 or 3-wire MPU interface.

AUDIO SIGNAL PATH

LINE INPUTS

The WM8734 provides Left and Right channel line inputs (RLINEIN and LLINEIN). The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external hi-fi or audio equipment.

Both line inputs include independent programmable volume level adjustments and input mute. The scheme is illustrated in Figure 8. Passive RF and active Anti-Alias filters are also incorporated within the line inputs. These prevent high frequencies aliasing into the audio band or otherwise degrading performance.

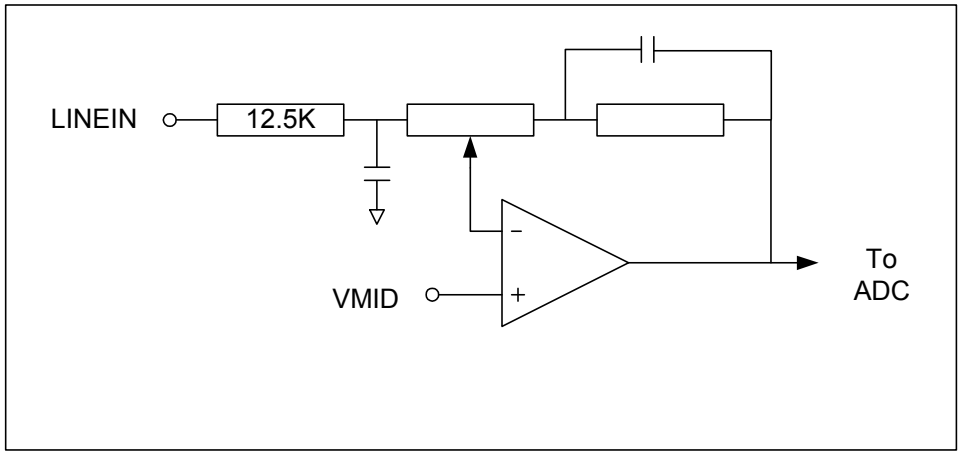


Figure 8 Line Input Schematic

The gain between the line inputs and the ADC is logarithmically adjustable from +12dB to –34.5dB in 1.5dB steps under software control. The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The gain is independently adjustable on both Right and Left Line Inputs. However, by setting the INBOTH bit whilst programming the volume control, both channels are simultaneously updated with the same value. Use of INBOTH reduces the required number of software writes required. The line inputs to the ADC can be muted in the analogue domain under software control. The software control registers are shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Left Line In	4:0	LINVOL[4:0]	10111 (0dB)	Left Channel Line Input Volume Control 11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB
	7	LINMUTE	1	Left Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[4:0] and LINMUTE to RINVOL[4:0] and RINMUTE 0 = Disable Simultaneous Load
0000001 Right Line In	4:0	RINVOL[4:0]	10111 (0dB)	Right Channel Line Input Volume Control 11111 = +12dB . .1.5dB steps down to 00000 = -34.5dB
	7	RINMUTE	1	Right Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[4:0] and RINMUTE to LINVOL[4:0] and LINMUTE 0 = Disable Simultaneous Load

Table 1 Line Input Software Control

The line inputs are biased internally through the operational amplifier to VMID. Whenever the line inputs are muted or the device placed into standby mode, the line inputs are kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

The external components required to complete the line input application is shown in the Figure 9.

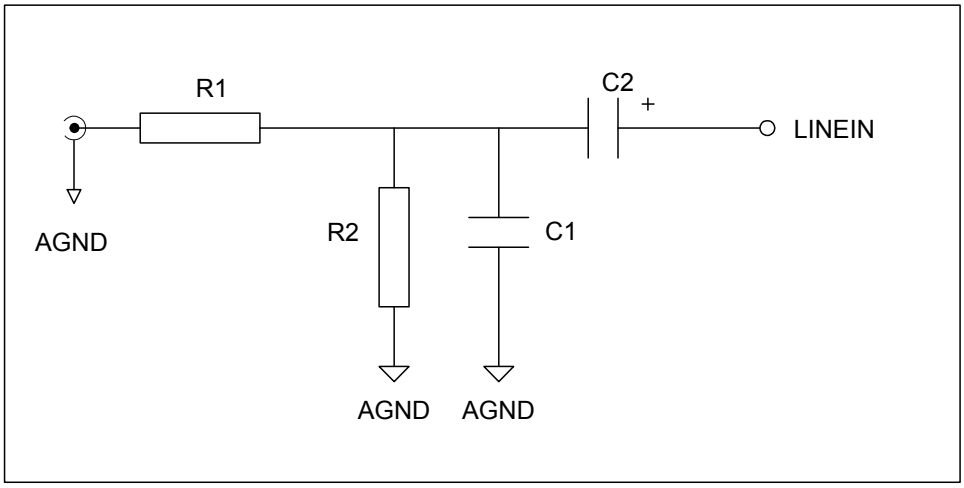


Figure 9 Line Input Application Drawing

For interfacing to a typical CD system, it is recommended that the input is scaled to ensure that there is no clipping of the signal. R1 = 5K, R2 = 5K, C1 = 47pF, C2 = 470nF (10V npo ceramic type).

R1 and R2 form a resistive divider to attenuate the 2 Vrms output from a CD player to a 1 Vrms level, so avoiding overloading the inputs. R2 also provides a discharge path for C2, thus preventing the input to C2 charging to an excessive voltage which may otherwise damage any equipment connected that is not suitably protected against high voltages. C1 forms an RF low pass filter for increasing the rejection of RF interference picked up on any cables. C2 forms a DC blocking capacitor to remove the DC path between the WM8734 and the driving audio equipment. C2 together with the input impedance of the WM8734 form a high pass filter.

ADC

The WM8734 uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated in the Figure 10.

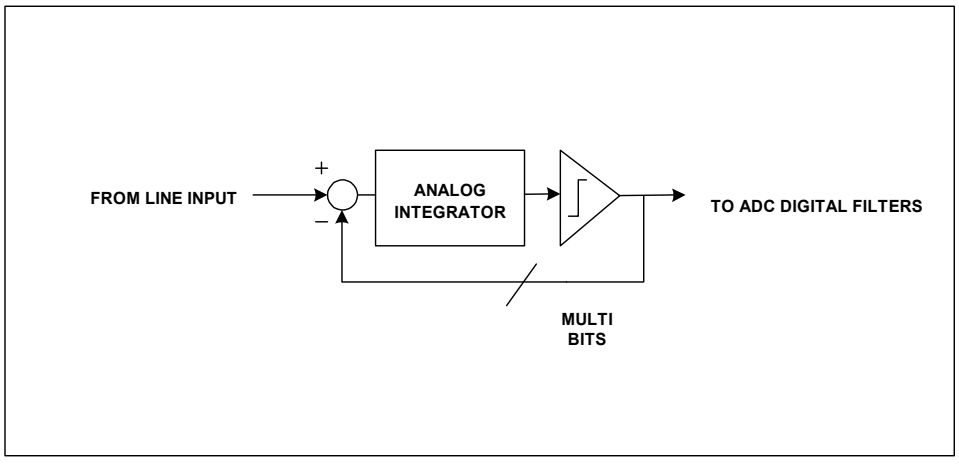


Figure 10 Multi-Bit Oversampling Sigma Delta ADC Schematic

The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The device employs a pair of ADCs. The two channels cannot be selected independently.

The digital data from the ADC is fed for signal processing to the ADC Filters.

ADC FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. Figure 11 illustrates the digital filter path.

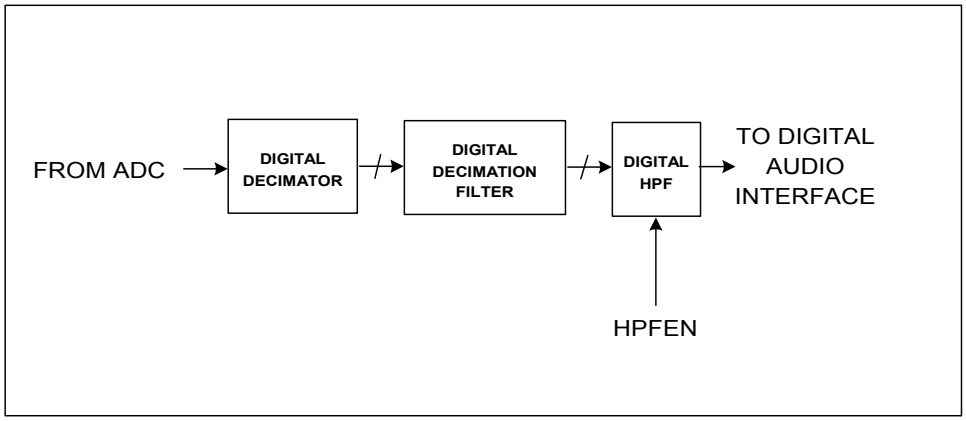


Figure 11 ADC Digital Filter

The ADC digital filters contain a digital high pass filter, selectable via software control. The high-pass filter response detailed in Digital Filter Characteristics. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the dc offset changed, the stored and subtracted value will not change unless the high-pass filter is enabled. The software control is shown in Table 2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
00000101 Digital Audio Path Control	0	ADCHPD	0	ADC High Pass Filter Enable (Digital) 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	4	HPOR	0	Store dc offset when High Pass Filter disabled 1 = store offset 0 = clear offset

Table 2 ADC Software Control

There are several types of ADC filters, frequency and phase responses of these are shown in Digital Filter Characteristics. The filter types are automatically configured depending on the sample rate chosen. Refer to the sample rate section for more details.

DAC FILTERS

The DAC filters perform true 24 bit signal processing to convert the incoming digital audio data from the digital audio interface at the specified sample rate to multi-bit oversampled data for processing by the analogue DAC. Figure 12 illustrates the DAC digital filter path.

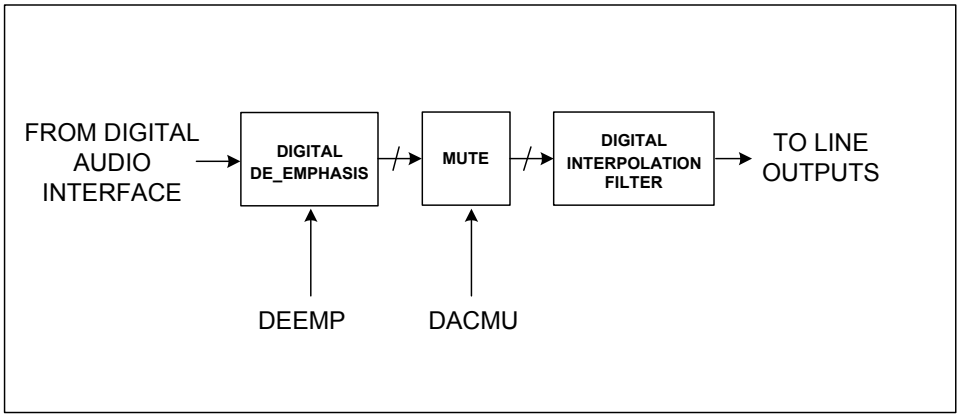


Figure 12 DAC Filter Schematic

The DAC digital filter can apply digital de-emphasis under software control, as shown in Table 3. The DAC can also perform a soft mute where the audio data is digitally brought to a mute level. This removes any abrupt step changes in the audio that might otherwise result in audible clicks in the audio outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000101 Digital Audio Path Control	2:1	DEEMP[1:0]	00	De-emphasis Control (Digital) 11 = 48kHz 10 = 44.1kHz 01 = 32kHz 00 = Disable
	3	DACMU	1	DAC Soft Mute Control (Digital) 1 = Enable soft mute 0 = Disable soft mute

Table 3 DAC Software Control

DAC

The WM8734 employs a multi-bit sigma delta oversampling digital to analogue converter. The scheme for the converter is illustrated in Figure 13.

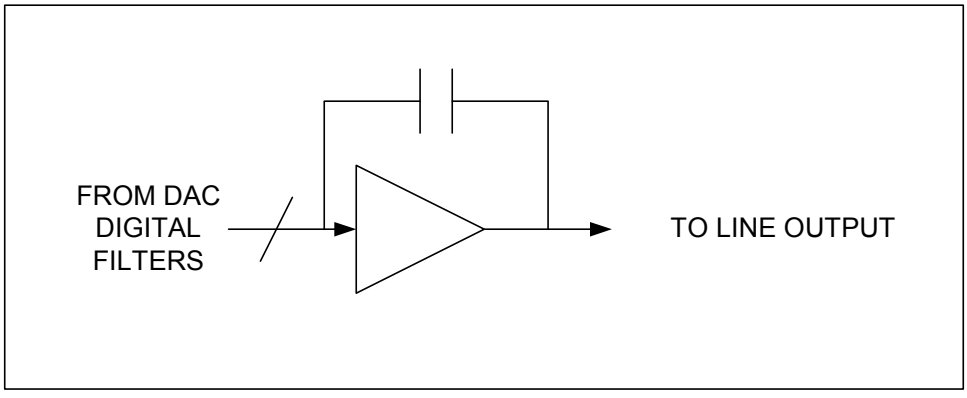


Figure 13 Multi-Bit Oversampling Sigma Delta Schematic

The DAC converts the multi-level digital audio data stream from the DAC digital filters into high quality analogue audio.

LINE OUTPUTS

The WM8734 provides two low impedance line outputs LLINEOUT and RLINEOUT, suitable for driving typical line loads of impedance 10K and capacitance 50pF. The line output is used to selectively sum the outputs from the DAC or/and the Line inputs in bypass mode.

The LLINEOUT and RLINEOUT outputs are only available at a line output level and are not level adjustable in the analogue domain, having a fixed gain of 0dB. The level is fixed such that at the DAC full scale level the output level is Vrms at AVDD = 3.3 volts. Note that the DAC full scale level tracks directly with AVDD. The scheme is shown in Figure 14. The line output includes a low order audio low pass filter for removing out-of band components from the sigma-delta DAC. Therefore no further external filtering is required in most applications.

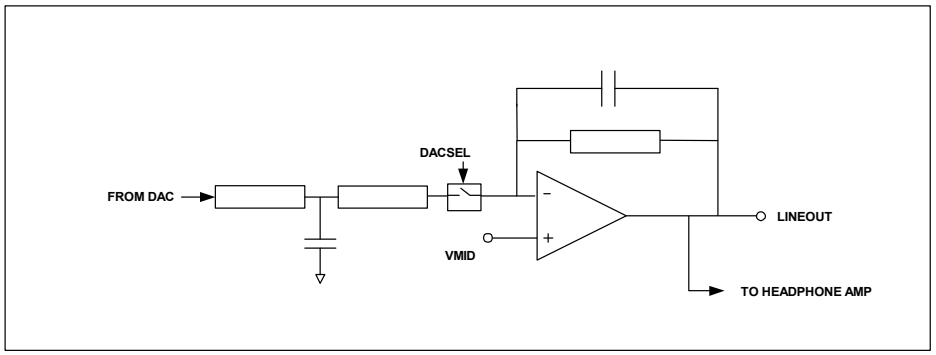


Figure 14 Line Output Schematic

The line output is muted by either muting the DAC (analogue) or Soft Muting (digital). Refer to the DAC section for more details. Whenever the DAC is muted or the device placed into standby mode the DC voltage is maintained at the line outputs to prevent any audible clicks from being present.

The software control for the line outputs is shown in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000100 Analogue Audio Path Control	4	DACSEL	0	DAC Select 1 = Select DAC 0 = Don't select DAC

Table 4 Output Software Control

The recommended external components are shown in Figure 15.

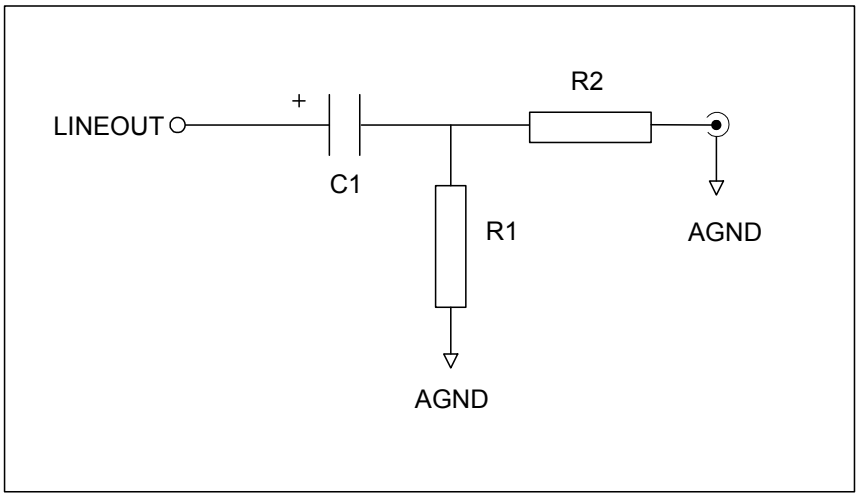


Figure 15 Line Outputs Application Drawing

Recommended values are C1 = 470nF (10V npo type), R1 = 47KΩ, R2 = 100Ω

C1 forms a DC blocking capacitor to the line outputs. R1 prevents the output voltage from drifting so protecting equipment connected to the line output. R2 forms a de-coupling resistor preventing abnormal loads from disturbing the device. Note that poor choice of dielectric material for C1 can have dramatic effects on the measured signal distortion at the output.

DEVICE OPERATION

DEVICE RESETTING

The WM8734 contains a power on reset circuit that resets the internal state of the device to a known condition. The power on reset is applied as DCVDD powers on and released only after the voltage level of DCVDD crosses a minimum turn off threshold. If DCVDD later falls below a minimum turn on threshold voltage then the power on reset is re-applied. The threshold voltages and associated hysteresis are shown in the Electrical Characteristics table.

The user also has the ability to reset the device to a known state under software control as shown in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001111 Reset Register	8:0	RESET	not reset	Reset Register Writing 00000000 to register resets device

Table 5 Software Control of Reset

When using the software reset. In 3-wire mode the reset is applied on the rising edge of CSB and released on the next rising edge of SCLK. In 2-wire mode the reset is applied for the duration of the ACK signal (approximately 1 SCLK period, refer to Figure 24).

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. To allow WM8734 to be used in a centrally clocked system, the WM8734 is capable of deriving the sample rate clock from this Master Clock (Master Mode) or receiving the sample rate clock from an external source (Slave Mode).

CORE CLOCK

The WM8734 DSP core can be clocked either by MCLK or MCLK divided by 2. This is controlled by software as shown in Table 6 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001000 Sampling Control	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divided by 2 0 = Core Clock is MCLK

Table 6 Software Control of Core Clock

Having a programmable MCLK divider allows the device to be used in applications where higher frequency master Clocks are available. For example the device can support 512fs master clocks whilst fundamentally operating in a 256fs mode.

DIGITAL AUDIO INTERFACES

WM8734 may be operated in either one of the 4 offered audio interface modes. These are:

- Right justified
- Left justified
- I^2S
- DSP mode

All four of these modes are MSB first and operate with data 16 to 32 bits, except right justified mode which does not support 32 bits.

The digital audio interface takes the data from the internal ADC digital filter and places it on the ADCDAT output. ADCDAT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. ADCLRC is an alignment clock that controls whether Left or Right channel data is present on the ADCDAT lines. ADCDAT and ADCLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. BCLK maybe an input or an output dependent on whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section.

The digital audio interface also receives the digital audio data for the internal DAC digital filters on the DACDAT input. DACDAT is the formatted digital audio data stream output to the DAC digital filters with left and right channels multiplexed together. DACLRC is an alignment clock that controls whether Left or Right channel data is present on DATDAT. DACDAT and DACLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK transition. DACDAT is always an input. BCLK and DACLRC are either outputs or inputs depending whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section

There are four digital audio interface formats accommodated by the WM8734. These are shown in the figures below. Refer to the Electrical Characteristic section for timing information.

Left Justified mode is where the MSB is available on the first rising edge of BCLK following a ADCLR or DACLRC transition.

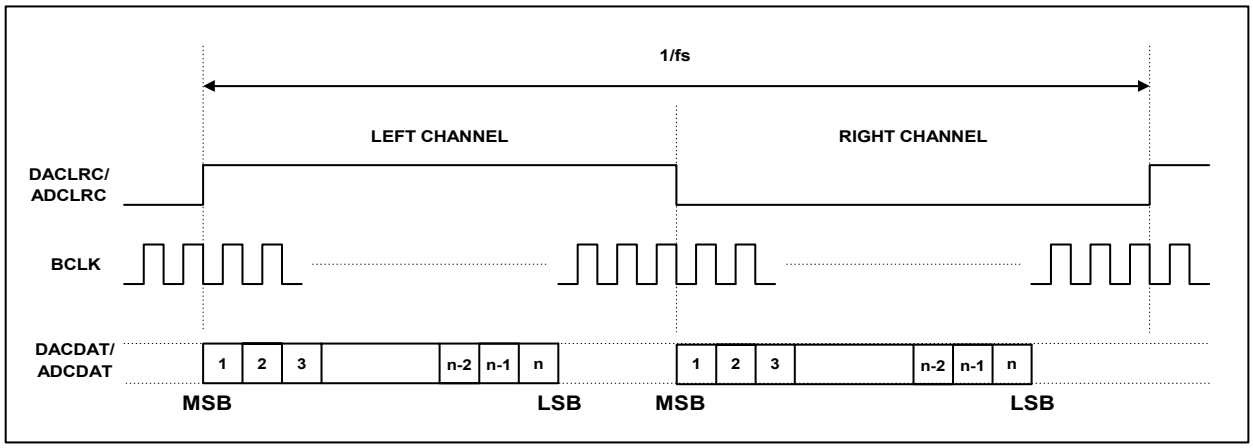


Figure 16 Left Justified Mode

I²S mode is where the MSB is available on the 2nd rising edge of BCLK following a DACLRC or ADCLRC transition.

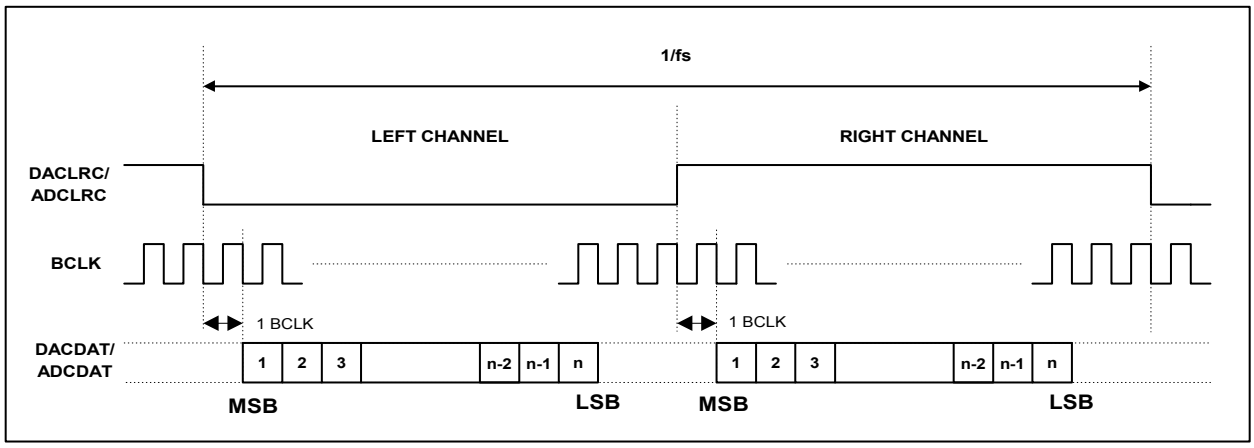


Figure 17 I²S Mode

Right Justified mode is where the LSB is available on the rising edge of BCLK preceding a DACLRC or ADCLRC transition, yet MSB is still transmitted first.

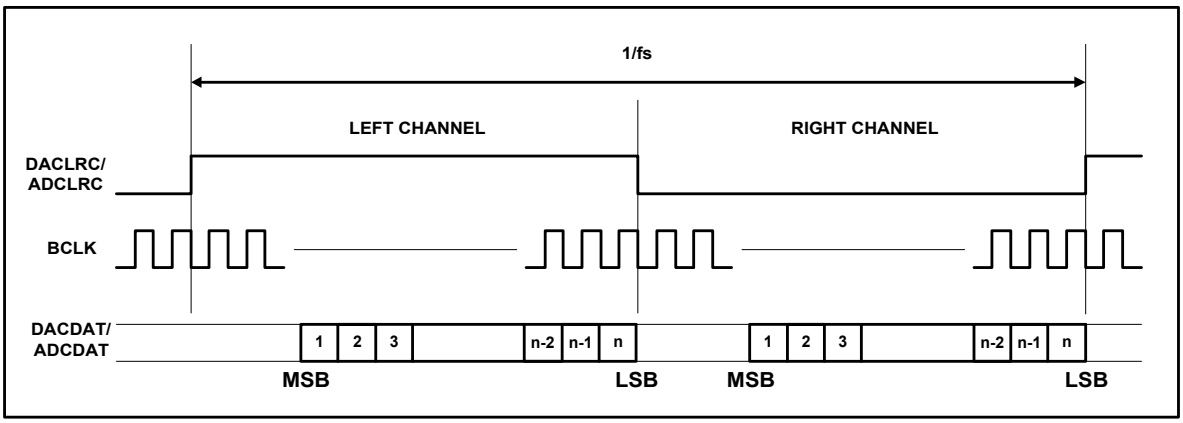


Figure 18 Right Justified Mode

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

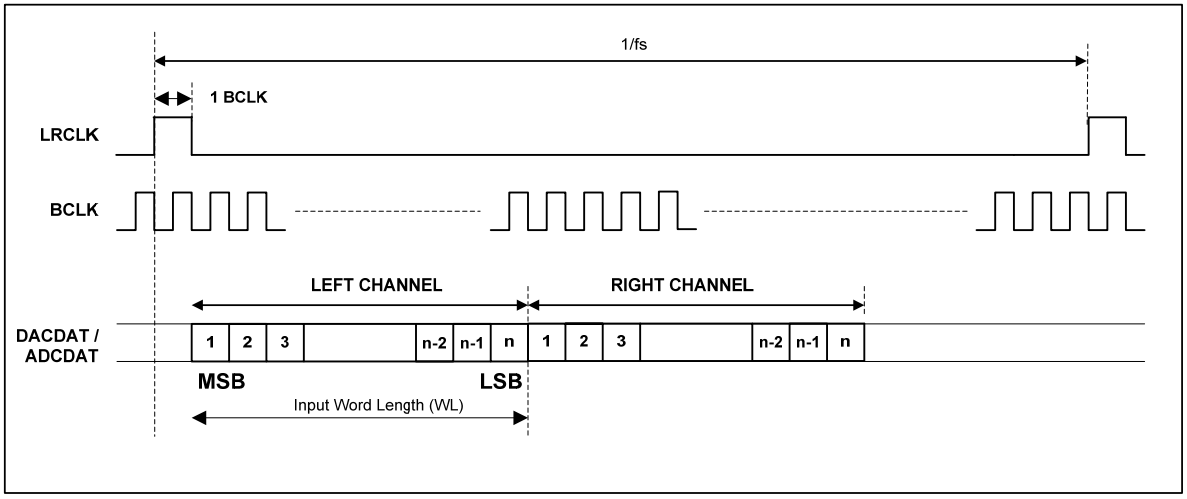


Figure 19 DSP/PCM Mode Audio Interface (mode A, LRP=1)

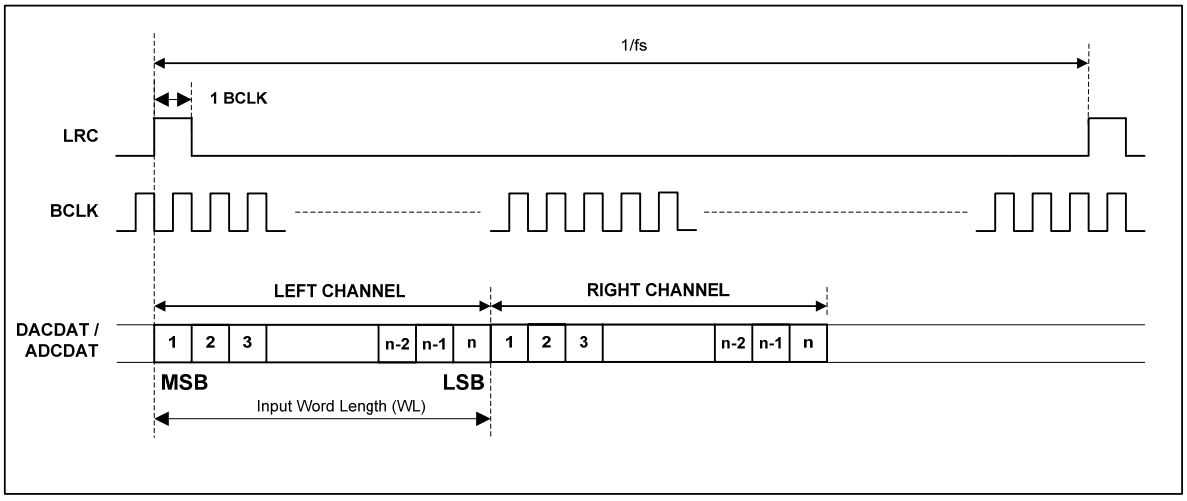


Figure 20 DSP/PCM Mode Audio Interface (mode B, LRP=0)

In all modes DACLRC and ADCLRC must always change on the falling edge of BCLK, refer to Figure 16, Figure 17, Figure 18, Figure 19 and Figure 20.

Operating the digital audio interface in DSP mode allows ease of use for supporting the various sample rates and word lengths. The only requirement is that all data is transferred within the correct number of BCLK cycles to suit the chosen word length.

In order for the digital audio interface to offer similar support in the three other modes (Left Justified, I^2S and Right Justified), the DACLRC, ADCLRC and BCLK frequencies, continuity and mark-space ratios need more careful consideration.

In Slave mode, DACLRC and ADCLRC inputs are not required to have a 50:50 mark-space ratio. BCLK input need not be continuous. It is however required that there are sufficient BCLK cycles for each DACLRC/ADCLRC transition to clock the chosen data word length.

In Master mode, DACLRC and ADCLRC will be output with a 50:50 mark-space ratio with BCLK output at 64fs.

The ADC and DAC digital audio interface modes are software configurable as indicated in Table 7. Note that dynamically changing the software format may result in erroneous operation of the interfaces and is therefore not recommended. The length of the digital audio data is programmable at 16/20/24 or 32 bits. Refer to the software control table below. The data is signed 2's complement. Both ADC and DAC are fixed at the same data length. The ADC and DAC digital filters process data using 24 bits. If the ADC is programmed to output 16 or 20 bit data then it strips the LSBs from the 24 bit data. If the ADC is programmed to output 32 bits then it packs the LSBs with zeros. If the DAC is programmed to receive 16 or 20 bit data, the WM8734 packs the LSBs with zeros. If the DAC is programmed to receive 32 bit data, then it strips the LSBs.

The DAC outputs can be swapped under software control using LRP and LRSWAP as shown in Table 7. Stereo samples are normally generated as a Left/Right sampled pair. LRSWAP reverses the order of that a Left sample goes to the right DAC output and a Right sample goes to the left DAC output. LRP swaps the phasing so that a Right/Left sampled pair is expected and preserves the correct channel phase difference.

To accommodate system timing requirements the interpretation of BCLK may be inverted, this is controlled vias the software shown in Table 6. This is especially appropriate for DSP mode.

ADCDAT lines are always outputs. They power up and return from standby low.

DACDAT is always an input. It is expected to be set low by the audio interface controller when the WM8734 is powered off or in standby.

ADCLRC, DACLRC and BCLK can be either outputs or inputs depending on whether the device is configured as a master or slave. If the device is a master then the ADCLRC, DACLRC and BCLK signals are outputs that default low. If the device is a slave then the ADCLRC, DACLRC and BCLK are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode, frame sync + 2 data packed words 10 = I^2S Format, MSB-First left-1 justified 01 = MSB-First, left justified 00 = MSB-First, right justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	4	LRP	0	DACLRC phase control (in left, right or I^2S modes) 1 = Right Channel DAC data when DACLRC high 0 = Right Channel DAC data when DACLRC low (opposite phasing in I^2S mode) or DSP mode A/B select (in DSP mode only) 1 = MSB is available on 2nd BCLK rising edge after ADCLRC/DACLRC rising edge 0 = MSB is available on 1st BCLK rising edge after ADCLRC/DACLRC rising edge
	5	LRSWAP	0	DAC Left Right Clock Swap 1 = Right Channel DAC Data Left 0 = Right Channel DAC Data Right
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	7	BCLKINV	0	Bit Clock Invert 1 = Invert BCLK 0 = Don't invert BCLK

Table 7 Digital Audio Interface Control

Note: If right justified 32 bit mode is selected then the WM8734 defaults to 24 bits.

MASTER AND SLAVE MODE OPERATION

The WM8734 can be configured as either a master or slave mode device. As a master mode device the WM8734 controls sequencing of the data and clocks on the digital audio interface. As a slave device the WM8734 responds with data to the clocks it receives over the digital audio interface. The mode is set with the MS bit of the control register as shown in Table 8.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

Table 8 Programming Master/Slave Modes

As a master mode device the WM8734 controls the sequencing of data transfer (ADCDAT, DACDAT) and output of clocks (BCLK, ADCLRC, DACLRC) over the digital audio interface. It uses the timing generated from either its on-board crystal or the MCLK input as the reference for the clock and data transitions. This is illustrated in Figure 21. ADCDAT is always an output from and DACDAT is always an input to the WM8734 independent of master or slave mode.

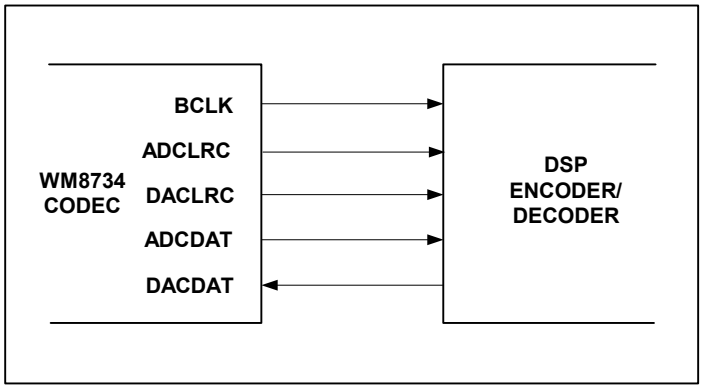


Figure 21 Master Mode

As a slave device the WM8734 sequences the data transfer (ADCDAT, DACDAT) over the digital audio interface in response to the external applied clocks (BCLK, ADCLRC, DACLRC). This is illustrated in Figure 22.

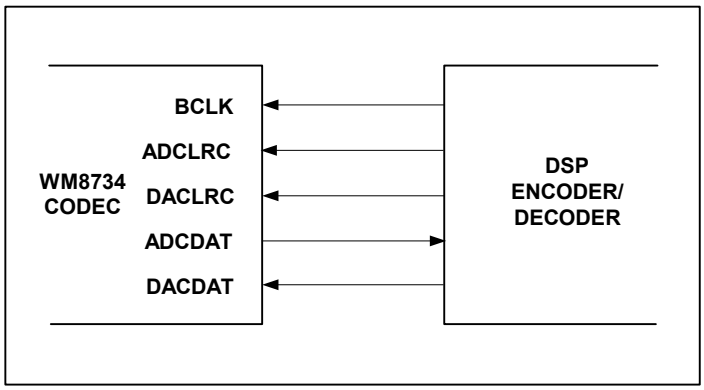


Figure 22 Slave Mode

Note that the WM8734 relies on controlled phase relationships between audio interface BCLK, DACLRC and the master MCLK. To avoid any timing hazards, refer to the timing section for detailed information.

AUDIO DATA SAMPLING RATES

The WM8734 provides for two modes of operation (normal and USB) to generate the required DAC and ADC sampling rates. Normal and USB modes are programmed under software control according to the table below.

In Normal mode, the user controls the sample rate by using an appropriate MCLK or crystal frequency and the sample rate control register setting. The WM8734 can support sample rates from 8ks/s up to 96ks/s.

In USB mode, the user must use a fixed MLCK or crystal frequency of 12MHz to generate sample rates from 8ks/s to 96ks/s. It is called USB mode since the common USB (Universal Serial Bus) clock is at 12MHz and the WM8734 can be directly used within such systems. WM8734 can generate all the normal audio sample rates from this one Master Clock frequency, removing the need for different master clocks or PLL circuits.