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Active Doubler 7.5-22.5/15.0-45.0 GHz

Rev. V1

Features

- +18 dBm Output Power
- -20 dBc Fundamental Leakage
- Lead-Free 3 mm 16-lead QFN Package
- 100% RF, DC and Output Power Testing
- RoHS* Compliant and 260°C Reflow Compatible

Description

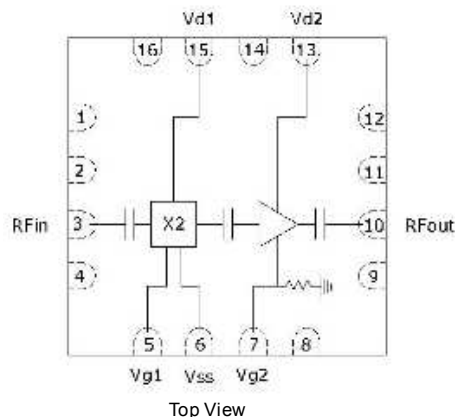
The XX1000-QT is a 7.5-22.5/15.0-45.0 GHz SMD active doubler that delivers + 18 dBm of output power. The device combines an active doubler with an output buffer amplifier that delivers constant power over a range of input powers. The device has excellent rejection of the fundamental and harmonic products and requires a single positive bias supply.

This device uses M/A-COM Technology Solutions' 0.15 GaAs pHEMT device model technology to ensure high reliability and uniformity. The device comes in a low-cost 3x3mm QFN Surface Mount Plastic Package offering excellent RF and thermal properties and is RoHS compliant. This device is well suited for Point-to-Point Radio, Microwave, LMDS, SATCOM and VSAT applications.

Ordering Information

| Part Number | Package |
|----------------|-------------------|
| XX1000-QT-0G00 | bulk quantity |
| XX1000-QT-0G0T | tape and reel |
| XX1000-QT-EV1 | evaluation module |

Functional Block Diagram



Pin Configuration¹

| Pin No. | Function | Pin No. | Function |
|---------|------------------|--------------|---------------|
| 3 | RF In | 13 | VD2 |
| 5 | VG1 | 15 | VD1 |
| 6 | VSS | 2,4,9,11 | Ground |
| 7 | VG2 ¹ | 1,8,12,14,16 | Not Connected |
| 10 | RF Out | | |

1. VG2 can be used for current regulating VD2 or VG2 can be set to GND with VD2 self-biasing at approximately 140mA.

Absolute Maximum Ratings²

| Parameter | Absolute Max. |
|----------------------------|-----------------------------------|
| Supply Voltage (Vd) | +6.0 VDC |
| Supply Voltage (Vss) | -6.0 VDC |
| Supply Current (Id) | 300 mA |
| Supply Current (Iss) | 60 mA |
| Gate Bias Voltage (Vg) | -0.4 VDC |
| Input Power (RF Pin) | +15.0 dBm |
| Storage Temperature (Tstg) | -65 °C to +165 °C |
| Operating Temperature (Ta) | -55 °C to MTTF Table ¹ |
| Channel Temperature (Tch) | MTTF Table ¹ |

2. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Electrical Specifications: 7.5-22.5 GHz Input Frequency (Ambient Temperature T=25°C)

| Parameter | Units | Min. | Typ. | Max. |
|--|-------|-------|------|-------|
| Output Frequency Range (fout) | GHz | 15.0 | - | 45.0 |
| Input Return Loss (S11) | dB | - | 15.0 | - |
| Output Return Loss (S22) | dB | - | 7.0 | - |
| Saturated Output Power (Psat) | dBm | - | +18 | - |
| RF Input Power (RF Pin) | dBm | -10.0 | - | +10.0 |
| Fundamental Leakage (fin) | dBc | - | 20 | - |
| Third Harmonic Leakage (3xfin) | dBc | - | 30 | - |
| Fourth Harmonic Leakage (4xfin) | dBc | - | 10 | - |
| Drain Bias Voltage (Vd1,2) | VDC | - | +5.0 | +5.5 |
| Gate Bias Voltage (Vg1) | VDC | -0.8 | -0.6 | -0.4 |
| Gate Bias Voltage (Vg2) | VDC | -1.2 | 0.0 | +0.1 |
| Supply Current (Id1,2) (Vd=5.0 V, Vg1=-0.6 V, Vg2=0.0 V Typical) | mA | - | 220 | 250 |
| Source Voltage (Vss) | VDC | -5.5 | -5.0 | -2.0 |
| Source Current (Iss) | mA | 25 | 50 | 60 |

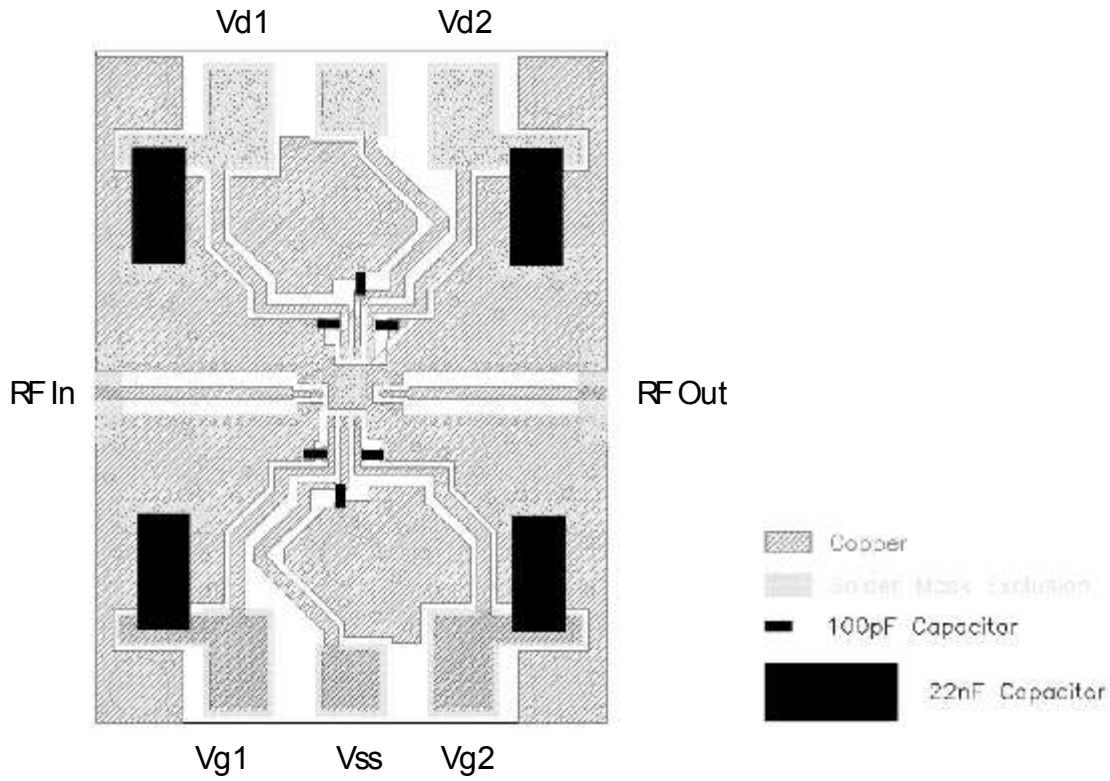
Handling Procedures

Please observe the following precautions to avoid damage:

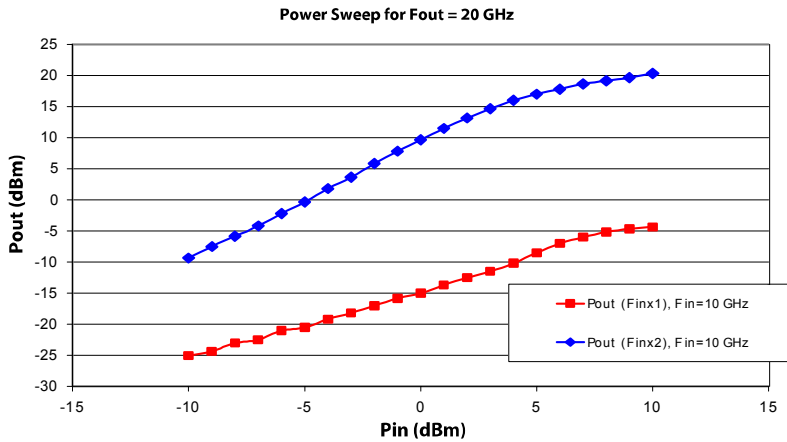
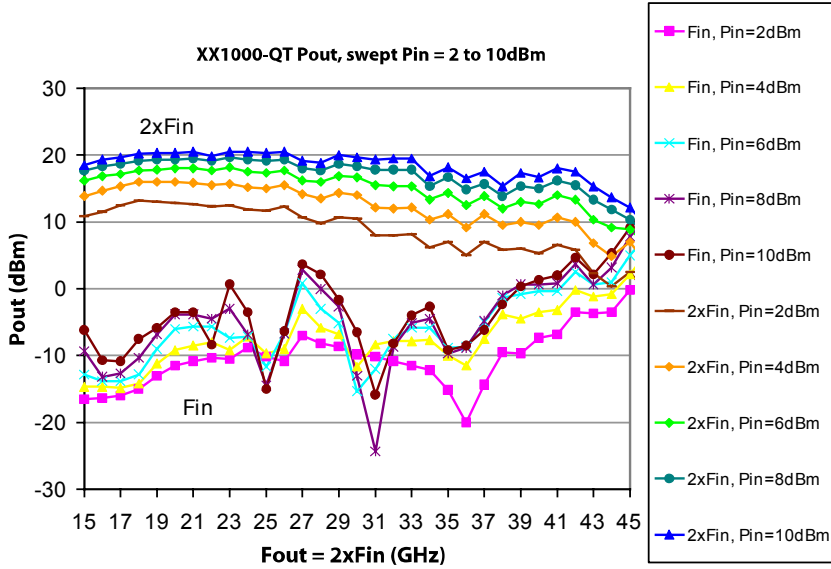
Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

PCB Layout

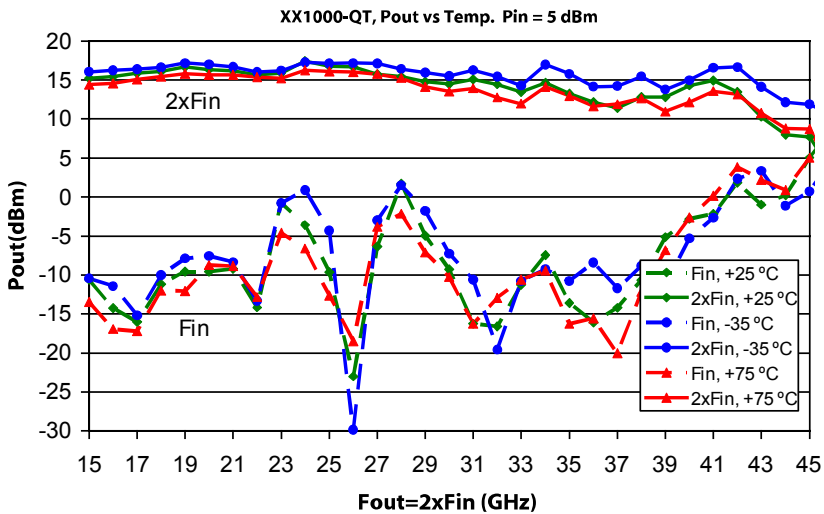
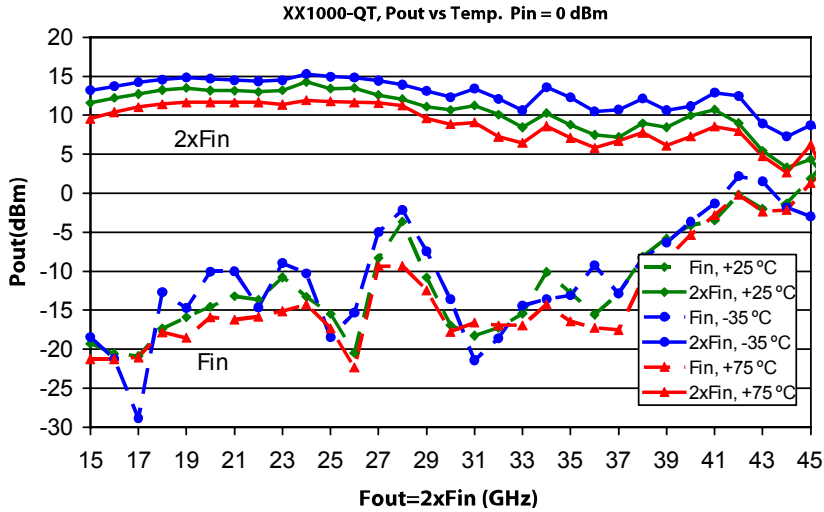


Typical Performance Curves: Nominal Bias Conditions



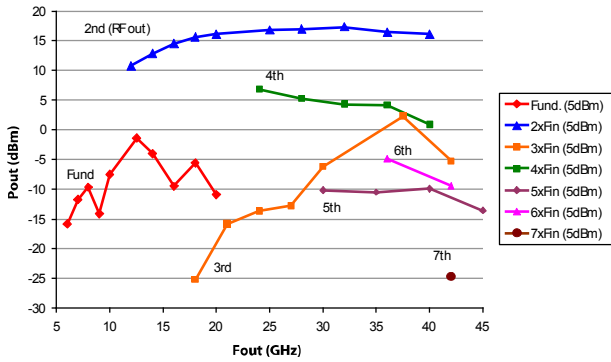
Measured results taken at room temperature in 40 GHz connectorized test fixture with no de-embedding.

Typical Performance Curves (cont.)



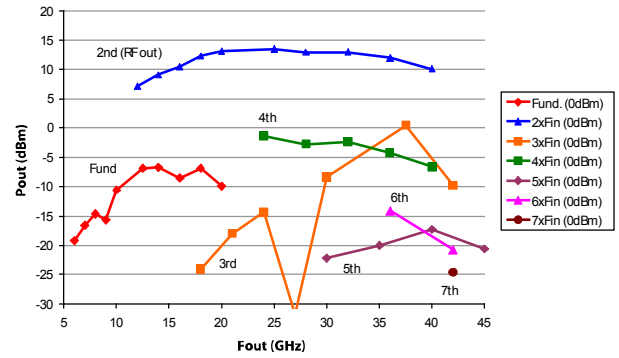
Typical Performance Curves (cont.)

Harmonic Products, Pin = +5 dBm (Fin = 6 - 20 GHz)



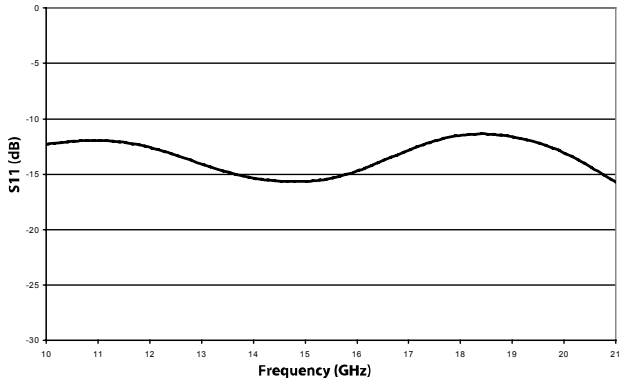
* Measured on-wafer with pre-packaging.

Harmonic Products, Pin = +0 dBm (Fin = 6 - 20 GHz)

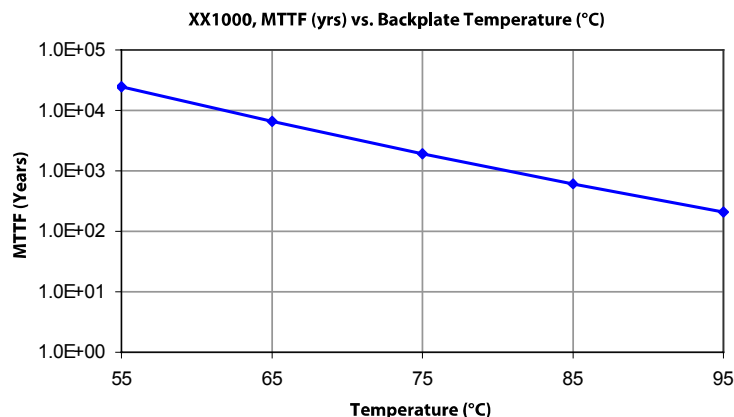


* Measured on-wafer with pre-packaging.

XX1000-QT: Input Return Loss (dB)



MTTF



MTTF is calculated from accelerated life-time data of single devices and assumes isothermal back-plate.

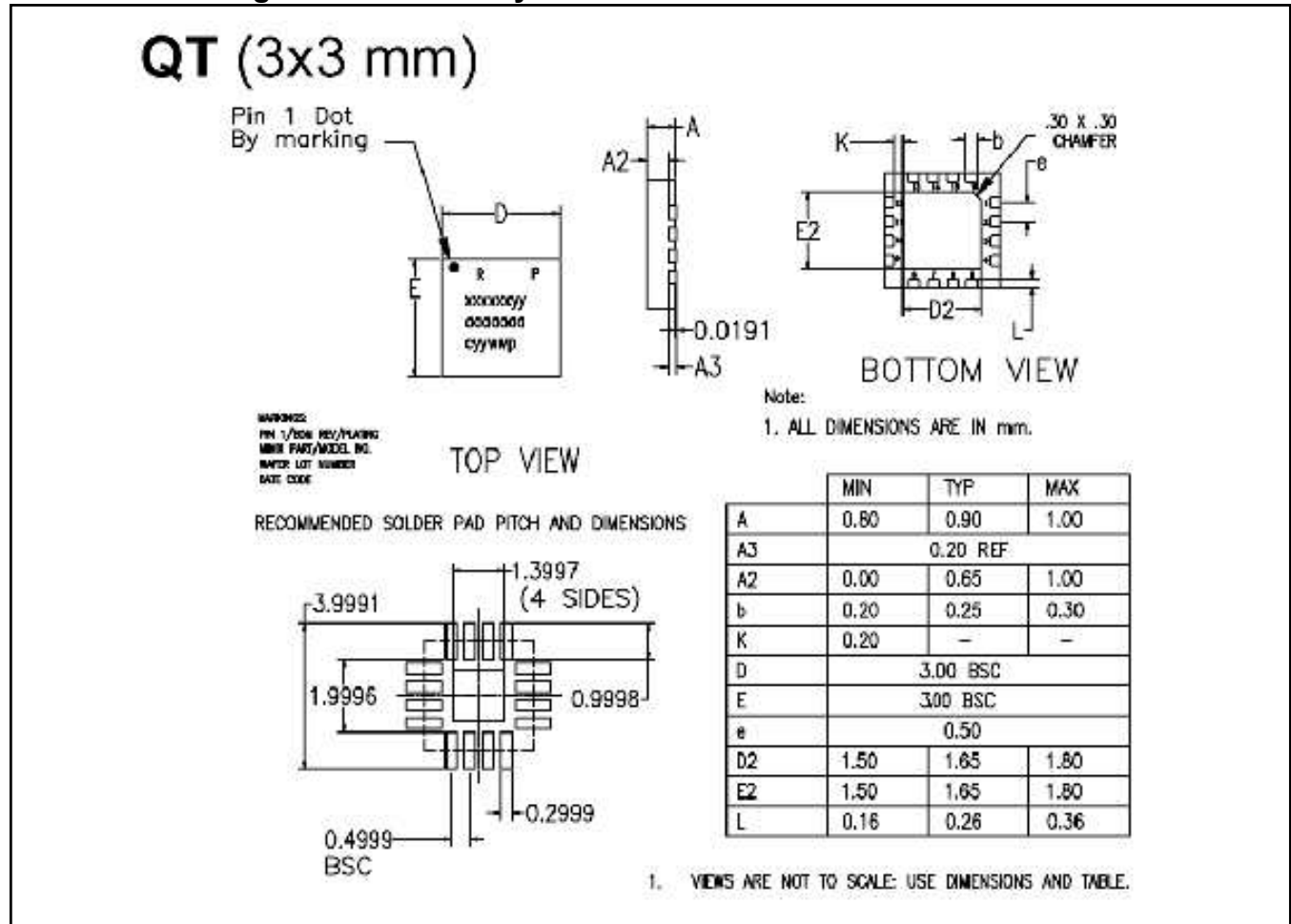
Bias Conditions: $V_{d1,2} = 5.0V$, $I_{d1,2} = 220\text{ mA}$, $V_{ss} = -5.0V$, $I_{ss} = 50\text{ mA}$

App Note [1] Biasing - It is recommended to separately bias each doubler stage with fixed voltages of $V_{d(1,2)} = 5.0V$, $V_{ss} = -5.0V$ and $V_{g1} = -0.6V$. The typical DC currents are $I_{d1} = 80\text{ mA}$, $I_{d2} = 140\text{ mA}$ and $I_{ss} = 50\text{ mA}$. V_{g2} can be used for active control biasing of V_{d2} , or it can be set to GND and V_{d2} will self bias at approximately 140mA. Maximum output power is achieved with $V_{ss} = -5.0V$ and $I_{ss} = 50\text{ mA}$ but the device will operate with reduced bias to $V_{ss} = -2.0V$ and $I_{ss} = 25\text{ mA}$. It is also recommended to use active biasing on V_{d2} with V_{g2} to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage for $V_{g2} = -0.1V$. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

Active Doubler
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Rev. V1

Lead-Free Package Dimensions/Layout



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