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Z02201

V.22BIS DATA PUMP WITH INTEGRATED AFE

Product Specification

PS000904-0107

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Document Disclaimer

Table of Contents

Features

Device	Data Pump	AFE	Speed (MHz)
Z02201	16-Bit	Integrated	12.288

- Combined data pump and Analog Front-End (AFE)
- Full duplex data modem throughput to 2400 bps
  - ITU V.22bis, V.23, V.22, V.21
  - Bell 212A and Bell 103
- FSK (V.23 1200/75 bps, V.21/Bell 103 300 bps), DPSK (V.22/Bell 212A 1200 bps), or QAM encoding (V.22bis 2400 bps)
- Automatic handshake plus full manual control over handshake timings
- Scrambler/descrambler functions plus selectable control over internal data pump functions
- Programmable Bi-Quad tone detectors for call-progress tone detection
- Adaptive equalization to compensate for a wide variety of line conditions
- Programmable transmit attenuation and selectable receive threshold
- Fully programmable call-progress detectors, signal quality detectors, tone detectors, tone generators, and transmit signal levels which aid in rapid country qualifications
- Simultaneous tone generation and detection
- Host port allows direct parallel interface to standard 8-bit microprocessors
- HDLC framing at all speeds
- On-chip peripherals
  - Full-duplex voice band AFE with 12-bit resolution
  - Synchronous Serial Interface port
  - Eye pattern interface
- Low power consumption: 50 mA typical
- 44-Pin PQFP and PLCC packages
- Single +5 VDC power supply
- 0 °C to +70 °C commercial temperature range

Note: International Telecommunications Union (ITU), formerly CCITT.

General Description

The Z02201 is a synchronous single-chip modem solution that provides a means to construct a V.22bis modem capable of 2400 bps full duplex over dial-up lines. The Z02201 is specifically designed for use in embedded modem applications where space, performance, and low power consumption are key requirements.

Operating over the Public Switched Telephone Network (PSTN), the Z02201 meets the modem standards for V.22bis, V.22, V.23, V.21, Bell 212A, and Bell 103.

A typical modem application can be made by simply adding a control microprocessor (host), phone-line interface, and DTE interface.

The Z02201 performs HDLC framing at all speeds. This capability eliminates the requirement for an external Serial Input/Output (SIO) device for Data Terminal Equipment (DTE) in products incorporating error control.

All modulation, demodulation, filtering, A/D and D/A conversion functions for transmit and receive are provided on-chip. Automatic and selectable compromise equalizers are included to optimize performance over a wide range of line types.

The Z02201 device compensates for a wide variety of adverse line conditions by using a combination of fixed link, fixed cable, and adaptive equalizers.

The Z02201 provides comprehensive selectable and programmable tone generation and detection.

All digital I/O signals are TTL compatible. The parallel interface is compatible with standard 8-bit microprocessors, allowing direct access to eight I/O registers and indirect access to the modem RAM.

The RAM access capability allows the host to retrieve diagnostic data, modem/line status and control data, and set programmable coefficients. The serial interface is used for data transfers. All control and status information is transferred by means of the parallel interface.

The Z02201 transmit drivers and receive amplifiers can be connected directly to a Data Access Arrangement (DAA) by means of a transformer. Completing this connection reduces the external circuits to a minimum.

In addition, the Z02201 offers further system level savings by providing built-in filters for both the Transmitter Analog Output and the Receiver Analog Input, thus eliminating the need for external filtering components.

The Z02201 device operates on a single +5 VDC power supply. During periods of no traffic, the host can place the modem into SLEEP mode, reducing power consumption to less than 1 percent of full load power.

Note: All signals with an overline, are active Low. For example, B/$\overline{W}$, in which WORD is active Low; or $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

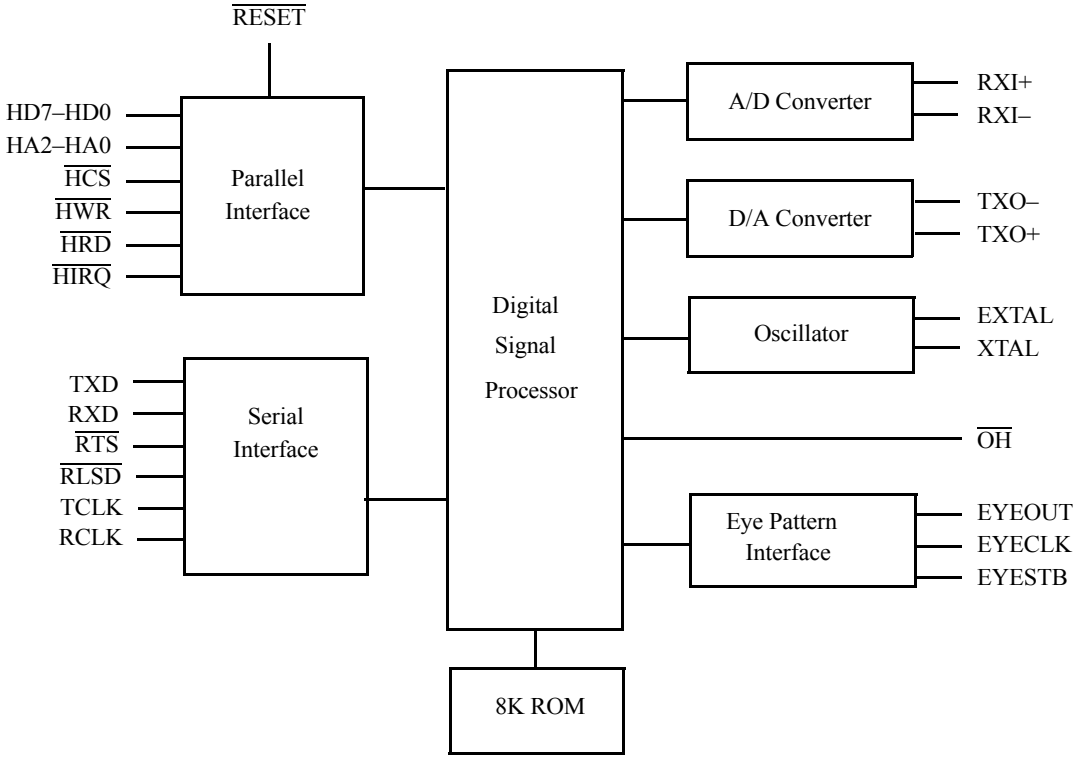

Figure 1. Z02201 Block Diagram

User Information

The ZiLOG Z02201 data pump can be selected for either parallel or serial synchronous data transfer under software control. Figure 2 indicates a block diagram of the general modem chip interface. The hardware and software configurations can be customized for a particular modem application. The parallel interface allows direct access to 7 I/O registers, indirect access to the modem RAM, and is compatible with the Z8, Z80, Z18X family, and other 8-bit microprocessors. The serial interface is used for data transfer. Controls and status information are transferred via the parallel interface. The RAM access capability allows indirect access to diagnostic data, additional status control, and programmable coefficients. The hardware and software interfaces are presented in the subsequent sections.

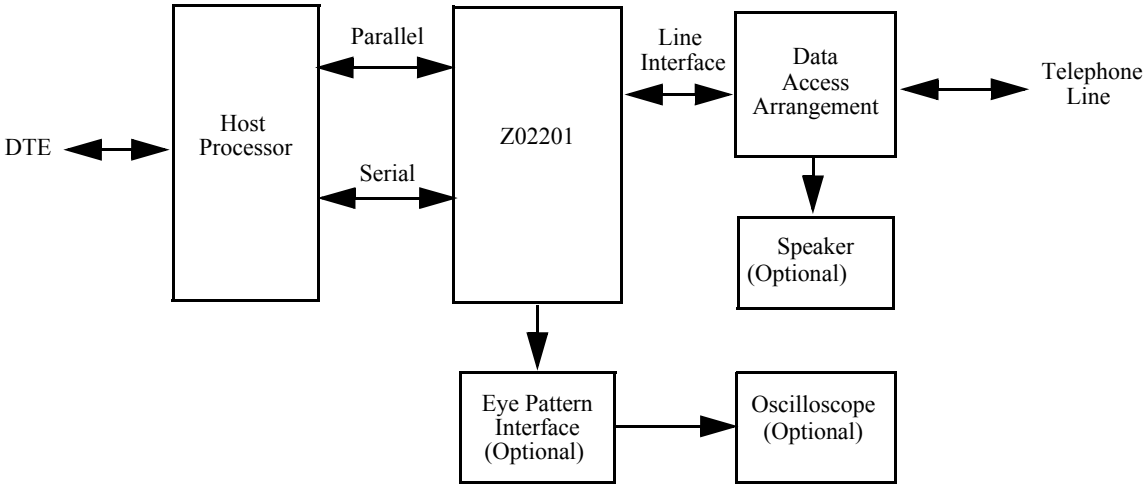

Figure 2. Z02201 System Block Diagram

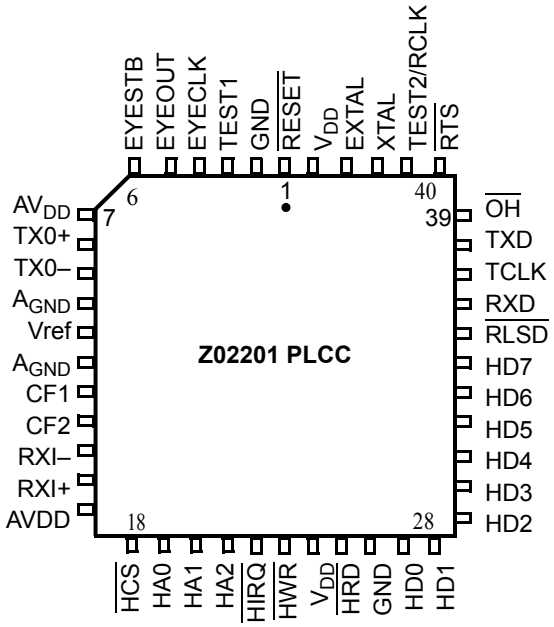

Figure 3. Z02201 44-Lead PLCC Pin Identification

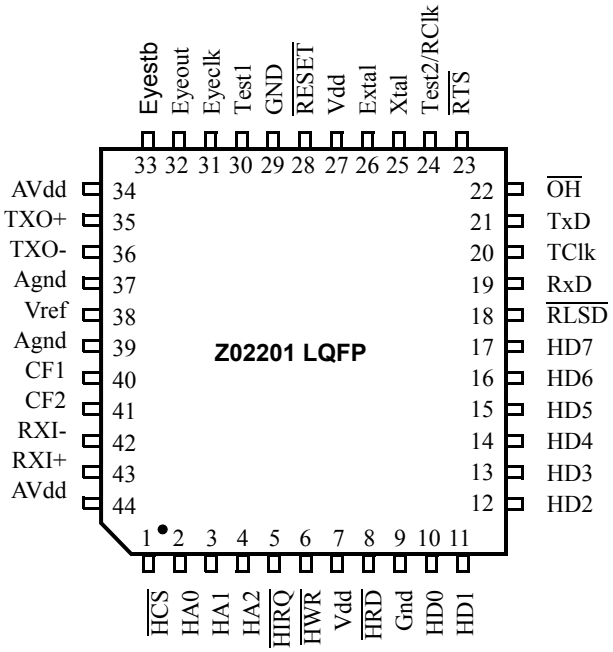

Figure 4. Z02201 44-Lead LQFP Pin Identification

Pin Description

Table 1. Z02201 Pin Assignments

PLCC Pin	LQFP Pin	Signal	Direction
1	28	RESET	
2	29	Gnd	
3	30	Test1	Input
4	31	Eyeclk	Output
5	32	Eyeout	Output
6	33	Eyestb	Output
7	34	AVdd	
8	35	TXO+	Output
9	36	TXO-	Output
10	37	Agnd	
11	38	Vref	Output
12	39	Agnd	
13	40	CF1	Input
14	41	CF2	Input
15	42	RXI-	Input
16	43	RXI+	Input
17	44	AVdd	
18	1	HCS	Input
19	2	HA0	Input
20	3	HA1	Input
21	4	HA2	Input
22	5	HIRQ	Output
23	6	HWR	Input
24	7	Vdd	
25	8	HRD	Input
26	9	Gnd	
27	10	HD0	Input/Output
28	11	HD1	Input/Output

Table 1. Z02201 Pin Assignments (Continued)

PLCC Pin	LQFP Pin	Signal	Direction
29	12	HD2	Input/Output
30	13	HD3	Input/Output
31	14	HD4	Input/Output
32	15	HD5	Input/Output
33	16	HD6	Input/Output
34	17	HD7	Input/Output
35	18	RLSD	Output
36	19	RxD	Output
37	20	TClk	Output
38	21	TxD	Input
39	22	OH	Output
40	23	RTS	Input
41	24	Test2/RClk	Input/Output
42	25	Xtal	Output
43	26	Extal	Input
44	27	Vdd	

Pin Functions

HD7–HD0 *Host Data Bus* (Bidirectional, Active High)—HD0–HD7 constitutes an 8-bit bidirectional data bus used for the transfer of control and status information.

$\overline{\text{HCS}}$ *Host Chip Select* (Input, Active Low)—When $\overline{\text{CS}}$ is Low, data transfer between the data pump and the host is enabled. Data transfers to the data pump registers are 8 bits wide.

$\overline{\text{HWR}}$ *Host Write Enable Strobe* (Input, Active Low)—The write enable strobe is an active Low signal that is used to initiate a write operation to the data pump. During a write operation, data is sent to the data pump by the host via the host data bus.

$\overline{\text{HRD}}$ *Host Read Enable Strobe* (Input, Active Low)—The read enable strobe is an active Low signal that is used to initiate a read operation from the data pump. During a read operation, data is transferred out of the data pump by the host via the host data bus.

$\overline{\text{HIRQ}}$ *Host Interrupt Request* (Output, Active Low)—The $\overline{\text{HIRQ}}$ is an open-drain output that can be tied through an external pull-up resistor to the digital power

supply V_{DD}. The $\overline{HIRQ}$ active Low data pump output can be activated when the host selects this option or requests by setting the RXIE or TXIE bits in the data pump Host Register. This pin can be connected to the host interrupt request pin to initiate host service.

$\overline{RESET}$ ***Reset*** **(Input, Active Low)—**The $\overline{RESET}$ signal places the device into its reset state.

HA2–HA0 ***Host Address*** **(Input, Active High)—**These three register select lines (pins) are used for addressing the controller-accessible internal registers of the data pump. When $\overline{HCS}$ is active, the state of the HA2–HA0 is used as the internal data pump interface register address. HA2 is the most significant bit; HA0 is the least significant bit.

$\overline{RLSD}$ ***Receive Line Signal Detect*** **(Output, Active Low)—**This pin indicates when an input signal has been detected.

RXD ***Receive Data*** **(Output)—**The data pump serial receive data is presented by the data pump to the local DTE on the RXD output.

TCLK ***Transmit Serial Data Clock*** **(Output)—**The serial data output clock is a synchronous data clock used to transfer serial data via synchronous serial interface between the data pump and the host. The clock frequencies are 2400, 1200, and 300 Hz, corresponding to the supported data bit rates.

TXD ***Transmit Data*** **(Input)—**The data pump accepts the serial transmit data from the local DTE on the TXD input when the data pump is configured to the serial transmit data mode. The serial transmit data mode is selected when the TDPM bit (bit 4) of the RAM CONTROL/DATA PUMP STATUS register (Register 6) is reset to 0.

$\overline{OH}$ ***Off Hook Relay Control*** **(Output, Active Low)—**This pin is activated to drive a relay which engages the modem with the phone line (the modem equivalent of picking up the receiver).

$\overline{RTS}$ ***Request To Send*** **(Input, Active Low)—**The logical OR of this pin and the RTSP bit (bit 3 of register 4), determines the data pump mode of operation. When the result of the logical OR of these two bits is logic 1, the data pump is in transmit mode at the selected speed, thereby placing the data pump in receive mode. In STANDBY mode, the state of this pin is insignificant.

EYECLK ***Eye Pattern Clock*** **(Output, Active High)—**Data is valid at the rising edge of the clock. The EYECLK can be used to clock an external Digital-to-Analog (D/A) converter shift register for eye pattern display.

EYEOUT ***Eye Pattern Data*** **(Output, Active High)—**This pin controls the serial 16-bit eye pattern output data. The first 8 bits is the EYEX data, and the next 8-bits are the EYEY data. This data can be used for display on an oscilloscope X and Y-axis following D/A conversion.

EYESTB ***Serial Eye Pattern Strobe*** **(Output, Active High)—**This signal is used for loading an external D/A converter.

TXO+ ***Transmit Differential Analog Output Positive*** **(Analog Output)—**The TXO+, TXO– is capable of driving a 600-ohm resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA). The TXO– and TXO+ can be configured either as a differential or single-ended output driver.

TXO– ***Transmit Differential Analog Output Negative*** **(Analog Output)—**The TXO–, TXO+ is capable of driving a 600-ohm resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA).

RXI– ***Receive Differential Analog Input Negative*** **(Analog Input)—**

RXI+ ***Receive Differential Analog Input Positive*** **(Analog Input)—**

TEST1 ***Test Pin 1*** **(Input, Active High)—**This pin is a test pin and must be tied to digital ground.

TEST2/RCLK ***Test Pin 2, Receive Data Clock*** **(Output, Active High)—**This pin is a test pin and must be tied to digital ground through a pull-down resistor. The resistor should be Low enough to ensure this pin floats below 0.8V when the part is in the $\overline{\text{RESET}}$ state. After $\overline{\text{RESET}}$, this pin becomes the Receive Data Clock Output. The resistor should be high enough such that the output can be driven to logic `1`. This pin is a synchronous data clock used to transfer serial data between the data pump and the host. The clock frequencies are 2400, 1200, and 300 Hz corresponding to the supported data bit rates.

Vref ***Reference Voltage*** **(Output, Active High—**An internally generated reference voltage.

XTAL ***Crystal*** **(Output, Active High)—**Crystal oscillator connection. This pin must be left open if an external clock is used instead of a crystal. The data pump chip can be connected to an external crystal circuit consisting of 24.576-MHz (parallel resonant) crystal, a resistor, and two capacitors.

EXTAL External Clock/ ***Crystal*** **(Input, Active High)—**Crystal oscillator connection. An external clock can be input to the Z02280 on this pin when a crystal is not used. The oscillator input is not a TTL level (see DC characteristics in Table 4).

CF1 and CF2 ***Integration Capacitor Pins 1 and 2*** **(Analog Input)—**Connect an 82pF capacitor between CF2 and CF1 to complete the internal feedback integration filter for improved Analog-to-Digital (A/D) conversion performance.

GND ***Digital ground***–0 Volts**—**

V_{DD} ***Digital Power***–5 Volts**—**

AV_{DD} ***Analog Power***–5 Volts**—**

AGND ***Analog Ground***–0 Volts**—**

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	+7.0	V
T_{OPR} (com)	Operating Temperature	0	+70	°C
T_{STG}	Storage Temperature	–65	+150	°C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The DC Parameters were tested as per Table 6. The Z02201 tester has active loads which are used to test the loading for I_{OH} and $I_{OR.}$

Available operating temperature range is: where: S = Standard Temperature Range

S = 0°C to +70°C

Voltage Supply Range:

+4.5 V ≤ V_{CC} ≤ + 5.5 V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus, and 100 pF for address and control lines.

Environmental and power requirements

The modem power and environmental requirements are indicated in Table 3 and Table 4.Table 5 provides the crystal specifications.

Table 3. Power Requirements

Voltage	Current Typical @ 25°C	Current Maximum @ 0°C
+5 V_{DC}, Operating	50 mA	<=100 mA
+5 V_{DC}, Sleep	25 µA	<=125 µA

Note: All voltages are ±5% DC and must have ripple less than 0.1V peak to peak. If switching supply is used, the frequency may be between 20 kHz and 150 kHz. No component of the switching frequency should be present outside of the supply greater than 500 µV peak.

Table 4. Environmental Requirements

Parameter	Value
Ambient Temperature Under Bias (Commercial Temp Range)	0°C to +70°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin to V_{SS}	–0.3V to +7V
Power Dissipation	250 mW
Soldering Temperature 0.5 sec	+230°C

Table 5. Z02201 Crystal Specifications

Parameter	Value
Temperature Range (Commercial)	0°C to +70°C
Nominal Frequency @ 25°C	24.576 MHz
Frequency Tolerance @ 25°C	±20 ppm
Temperature Stability @ 0°C to 70°C	±25 ppm
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF max.

Table 5. Z02201 Crystal Specifications (Continued)

Parameter	Value
Load Capacitance	32 ± 0.3 pF
Drive Level	1.0 mW max.
Aging, per Year Max.	± 5 ppm
Oscillation Mode	Fundamental
Series Resistance	60 ohms max.
Max. Frequency Variation with 28.8 or 35.2 pF load	±30 ppm

DC Characteristics

Table 6. TDC Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Test Conditions
Pin Types I and I/O: Input and Input-Output						
V_{IH}	Input High Voltage	2	–	V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	0	–	0.8	V	
I_L	Input Leakage Current	–10	–	10	µA	GND <V0<V_{DD}
Pin Types O and IO: Output and Input-Output						
V_{OH}	Output High Voltage	2.4	–	–	V	$I_{OH=}$ –200 µA
V_{OL}	Output Low Voltage	0	–	0.4	V	$I_{OI=}$ –2.2 mA
I_{OZ}	Tri-state Leakage Current	–10	–	10	µA	GND<V0<V_{DD}
Pin Types I-PU and I-PD: Input with Internal Pull-up/Pull-down Resistor						
V_{IH}	Input High Voltage	2		V_{CC} +0.3	V	$I_{OI=}$ –2.2 mA
V_{IL}	Input Low Voltage	0		0.8	V	
I_{IL}	Input Current	–10		10	µA	GND <V0<V_{DD}
Pin Type XI: Crystal Input						
V_{IH}	Input High Voltage	V_{DD} x0.8		V_{DD}	V	
V_{IL}	Input Low Voltage	0				
Pin Type O-OD: Output with Open-Drain						
V_{OL}	Output Low Voltage	0	–	0.4		I_{OI}=2.2 mA
I_{OZ}	Tri-state Leakage Current	–10	–	10	µA	GND<V0<V_{DD}
Pin Type XO: Crystal Output						
V_{OH}	Output High Voltage	V_{DD} –1		V_{DD}	V	I_{OH}=1.0 mA
V_{OL}	Output Low Voltage	0		1	V	I_{OI}=–1.0 mA
Pin Type AI: Analog Input						
V_{DC}	Input Bias Offset	V_{REF} –15	V_{REF}	V_{REF} +15	mV	
I_L	Input Current	–100	–	100	µA	
C_{IN}	Input Capacitance	–	10	–	pF	
R_{IN}	Input Resistance	–	20	–	Kohm	
Pin Type AO: Analog Output						

Table 6. TDC Pin Characteristics (Continued)

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_O	Analog Output Voltage	V_{REF} – 1.163	V_{REF}	V_{REF} +1.163	mV	
V_{OFF}	Output DC Offset	V_{REF} –40	V_{REF}	V_{REF} +40	mV	
R_O	Output Resistance	–	0.8	–	Ohm	
C_O	Output Capacitance	–	10	–	pF	
Z_I	Load Impedance	400	600	Infinite	Ohm	
Pin Type PWR: Power and Ground						
V_{DD}	Digital Supply Voltage	4.75	5	5.25	V	Voltage
GND	Digital Ground	–	–	0	–	
AV_{DD}	Analog Supply Voltage	V_{DD}	V_{DD}	V_{DD}	V	
AGND	Analog Ground	GND	GND	GND	V	
I_{DD1}	Digital Supply Current	–	45	90	mA	Operating
I_{ADD1}	Analog Supply Current	–	5	10	mA	Operating
I_{DD2}	Digital Supply Current	–	20	100	µA	Sleep Mode
I_{ADD2}	Analog Supply Current	–	5	25	µA	Sleep Mode

AC Characteristics

Timing Diagrams

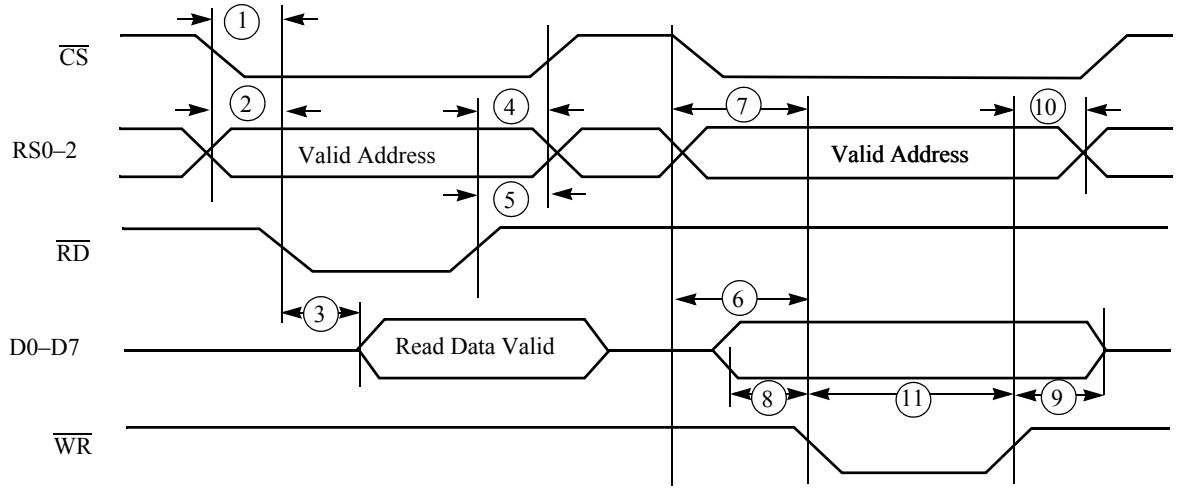

Figure 5. Microprocessor Interface Read/Write Diagram

Table 7. Microprocessor Interface Timing

Description	Parameter	Min	Typ	Max	Units
Read Timing					
HA0–2 and $\overline{HCS}$ to $\overline{HRD}$ Setup Time	1	0	–	–	ns
HA0–2 to $\overline{HRD}$ Setup Time	2	0	–	–	ns
$\overline{HRD}$ to Data Access Time	3	—	25	85	ns
$\overline{HRD}$ Data Hold	4	0	10	–	ns
HA0–2 and $\overline{HCS}$ Hold From $\overline{HRD}$	5	0	–	–	ns
Write Timing					
HA0–2 and $\overline{HCS}$ to $\overline{HWR}$ Setup Time	6	70	–	–	ns
$\overline{HCS}$ to $\overline{HWR}$ Setup Time	7	70	–	–	ns
Data to $\overline{HWR}$ Setup Time	8	0	–	–	ns
$\overline{HWR}$ Data Hold	9	10	–	–	ns
HA0–2 and $\overline{HCS}$ Hold from $\overline{HWR}$	10	10	–	–	ns

Table 7. Microprocessor Interface Timing (Continued)

Description	Parameter	Min	Typ	Max	Units
$\overline{\text{HWR}}$ Pulse Width	11	25	–	–	ns
Reset Timing					
Reset Pulse Width		1.0	–	–	µs
Reset Rise Time			–	100	ns

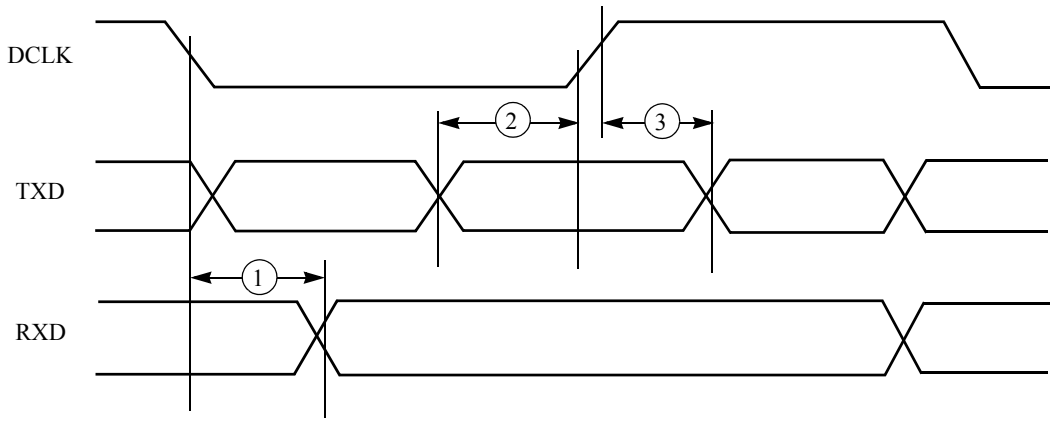

Figure 6. Serial Port Timing Diagram

Table 8. Serial Interface Timing

Description	Parameter	Min	Typ	Max	Units
RXD Data Valid Delay Time	1	–	12	–	ns
TXD Data Setup Time	2	100	–	–	ns
TXD Data Hold Time	3	100	–	–	ns

Timing Diagrams

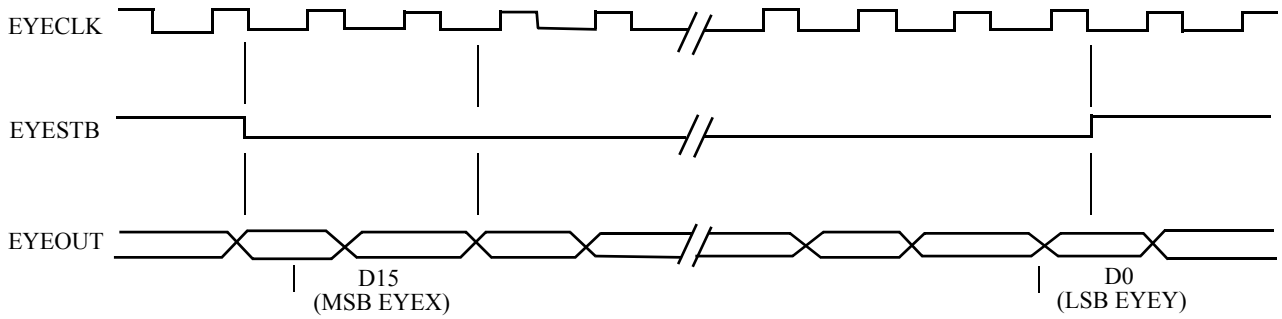

Figure 7. Eye Pattern Port Timing Diagram

Table 9. Analog Characteristics Table

Description	Parameter	Min	Typ	Max	Units
Input impedance of transformer interface	1	400	1200	–	Ohm
3 dB point of interface	2	21	26.5	32.5	kHz
External integration capacitance Type NPO (COG)	3	73	82	90	pF

Analog Inputs: Type AI

Table 10. Analog Inputs, Type AI

AC Characteristics	Sym	Min	Typ	Max	Units
Input Impedance (DC to V_{REF})	Z_{IN}	15K	25K	–	Ω
Power Supply Rejection	P_{SRRi}	40	–	–	dB
Input Current	I_i	–80	–	80	µA
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNi}	–	–	–72	dBm
Signal to Distortion	S_{TDi}	30	–	–	dB

The characteristics below are provided for information only. They are not tested

except in the functional test vectors.

Characteristics	Sym	Min	Typ	Max	Units
Input Capacitance	C_{IN}	–	10	–	pF
Input Bias	V_{DCOFF}	–	+2.5	–	V
Analog Input Voltage (Peak Differential), (23)	V_{PKI}	–2.362	–	+2.362	V
Analog Input Voltage (Per RXI+. RXI- Pin)	V_{PKIP}	–1.181	–	+1.181	V

Analog Outputs: Type A0

Table 11. Analog Inputs Type A0

AC Characteristics	Sym	Min	Typ	Max	Units
Power Supply Rejection	P_{SRRO}	40	–	–	dB
Signal to Distortion	S_{TD0}	35	–	–	dB
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNO}	–	–	–72	dBm
Out of Band Noise	N_{qo}				dBm
4–8 kHz	–	–	–20		dBm
8–12 kHz	–	–	–40		dBm
12 kHz and Above in 4 kHz Bandwidths	–	–	–55		dBm

Characteristics	Sym	Min	Typ	Max	Units
Output Impedance	Zout	–	0.80	–	Ω
Output Capacitance	Cout	–	10	–	pF
Analog Output Voltage (peak differential), (24)	Vpko	–2.375	–	+2.375	V
Load Impedance (25)	ZI	400	600	–	–

Hardware Interface Signals

The Z02201 interface consists of the Synchronous Serial Interface Port, 8-bit Host Microprocessor Interface, Eye Pattern Interface, Voice Band AFE, System Signals, and Overhead Signals. The Z02201 functional interconnect diagram is indicated in Figure 8. Any signal that is active Low is represented by a line over the signal name.

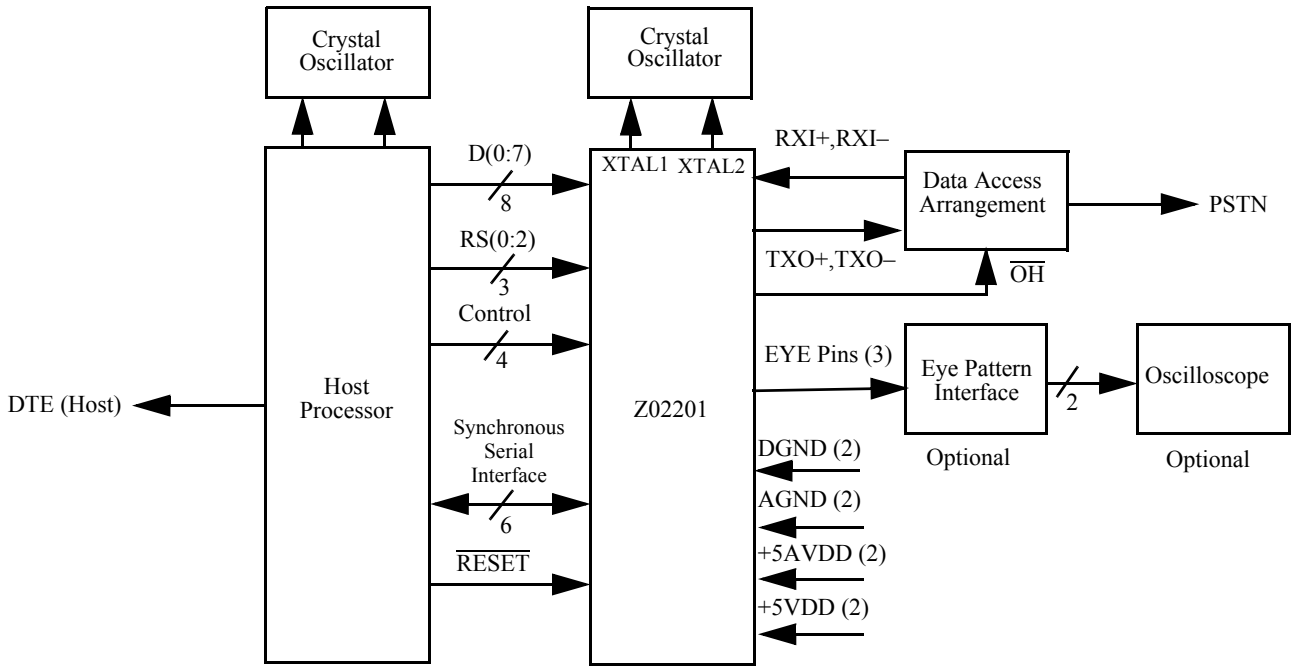

Figure 8. Modem Functional Interconnect Diagram

Synchronous Serial Interface Port

The Synchronous Serial Interface Port provides no parallel-to-serial/serial-to-parallel conversion hardware. The synchronous serial interface port consists of six signal pins as shown in Table 12.

Table 12. Synchronous Serial Interface Port

Pin	Signal Name
TxD	Transmit Data
RxD	Receive Data
RTS	Request To Send
RLSD	Receive Line Signal Detect
TCLK	Transmit Data Clock
RCLK	Receive Data Clock

Host Port Interface

The host parallel port interface consists of 15 signal pins: 8-bit bidirectional data bus pins (HD7–HD0), 3-bit Address bus (HA2–HA0), four control lines, which include the HoST READ ($\overline{\text{HRD}}$), HOST WRITE ($\overline{\text{HWR}}$), HOST CHIP SELECt ($\overline{\text{HCS}}$), and HOST INTERRUPT REQUEST ($\overline{\text{HIRQ}}$). Multiple interrupt sources are provided in the Z02201, each of which can be masked under host control.

The host parallel interface allows the host to access the data pump RAM address and data bits, transmit and receive data, control the RAM and status bits, and read data pump status bits. The host can access eye pattern functions, transmit and receive tones, and access adaptive equalizer coefficients in modem-type applications.

The host parallel interface is compatible with standard 8-bit microprocessors, which include the Z8 and Z80 bus.

Eye Pattern Interface

The eye pattern interface consists of three pins: EYE PATTERN DATA (EYEOUT), EYE PATTERN CLOCK (EYECLK), and EYE PATTERN STROBE (EYESTB). Sixteen bits of data are serially transmitted via EYEOUT, under control of EYESTB and EYE-CLK. The first byte is the X-coordinate and the second byte is Y-coordinate of the sample. The least significant bit is presented first for both the X and Y coordi-nates. A schematic of an eye pattern circuit is found in Figure 16 at the end of this specification.

The EYE PATTERN DATA, EYEOUT, outputs a serial bit stream containing data for display of the eye pattern on an oscilloscope after D/A conversion. 8 bits of the X-axis data and 8 bits of the Y-axis are output as a single 16-bit data stream with the