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Z8036/Z8536

Z-CIO and CIO Counter/Timer and Parallel I/O Unit

Product Specification

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Chapter 1
General Description

1.1 INTRODUCTION

The Z8036 Z-CIO and Z8536 CIO Counter/Timer and Parallel I/O devices are general-purpose peripheral circuits that satisfy most counter/timer and parallel I/O needs encountered in system design, and are therefore helpful in real-time situations and for interrupt control. The Z8036 Z-CIO is designed for systems using the Z-BUS or any other multiplexed Address/Data bus. The Z8536 CIO is designed for CPUs using a nonmultiplexed bus, like that of the Z80 CPU. The differences between the two devices are found in the CPU interface, pin-outs, and timing.

NOTE

All material in this manual referring to "the CIO" applies to both the Z8036 and the Z8536, unless specifically designated by reference to either Z8036 or Z8536. All references to the Z-CIO refer only to the Z8036.

1.2 FEATURES

The Z-CIO and CIO devices satisfy a wide range of applications because of their extensive list of features:

- Two independent 8-bit, double-buffered, bidirectional I/O ports, plus a 4-bit special-purpose I/O port. The I/O ports feature programmable polarity, programmable direction (Bit mode), 1's catchers, and programmable open-drain outputs.
- Four handshake modes, including 3-Wire (like the IEEE-488).
- REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer.
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- Three independent 16-bit counter/timers, each with three output duty cycles (pulsed, one-shot, and square-wave) and up to four external access lines (count input, output, gate, and trigger). The counter/timers are programmable as retriggerable or non-retriggerable.
- All registers are read/write. In the Z8036, the registers are directly addressable; in the Z8536, the registers are accessed in two steps.

1.3 OVERVIEW

The CIO (Figure 1-1) consists of a CPU interface, three I/O ports (two general-purpose 8-bit ports and one special-purpose 4-bit port), three 16-bit counter/timers, an interrupt control logic block, and an internal control logic block. A large number of programmable options allow users to tailor the configuration to suit specific applications.

1.3.1 I/O Ports

There are three I/O ports: two general-purpose 8-bit ports (which are linkable into one 16-bit port), and one special-purpose 4-bit port.

1.3.1.1 Ports A and B

The two general-purpose 8-bit I/O ports, Ports A and B (Figure 1-2), are identical, except that Port B can be programmed to provide external access to Counter/Timers 1 and 2. Either port can be programmed to be either a handshake-driven, single- or double-buffered port (input, output, or bidirectional), or a control port with the direction of each bit individually programmable.

Both ports include pattern-recognition logic, which allows interrupt generation when a specific pattern is detected. The pattern-recognition logic can be programmed to make the port function like a priority interrupt controller. Ports A and B can also be linked to form a 16-bit I/O port with handshake.

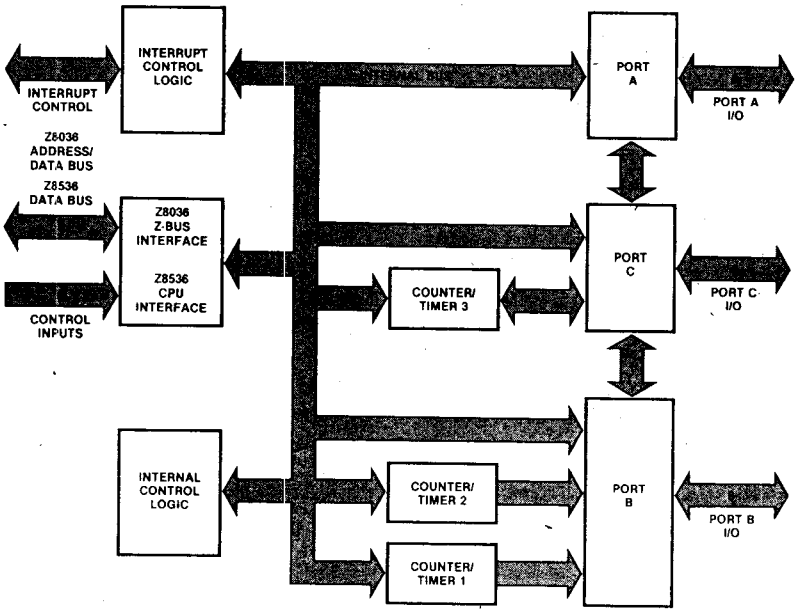

Figure 1-1. Z8036/Z8536 Z-CIO/CIO Block Diagram

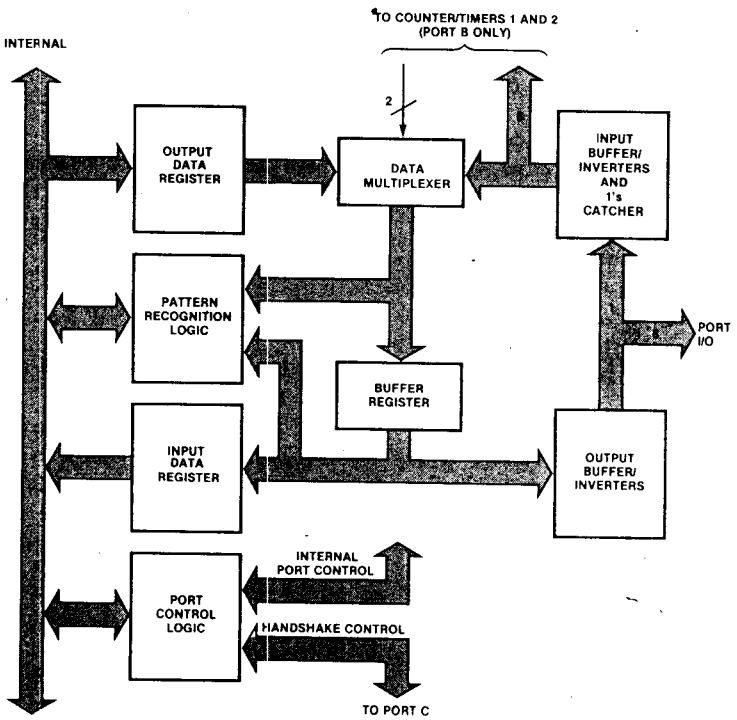

Figure 1-2. Ports A and B Block Diagram

Each port has 12 control and status registers, which control these capabilities. The data path of each port is composed of three internal registers: the Input Data register, the Output Data register, and the Buffer register. The Input Data register is accessed by writing the Port Data register; similarly, the Output Data register is accessed by reading the Port Data register. Two registers, the Mode Specification register and the Handshake Specification register, are used to define the mode of the port and to specify which type of handshake, if any, is to be used. The reference pattern for the pattern-recognition logic is specified by the contents of three registers: the Pattern Polarity register, Pattern Transition register, and Pattern Mask register. The detailed characteristics of each bit path (for example, the direction of data flow or whether a path is inverting or non-inverting) are programmed using the Data Path Polarity register, Data Direction register, and Special I/O Control register.

For each port, the primary control and status bits are grouped in a single register, the Command and Status register. After the port is configured, this is the only register that needs to be accessed frequently. To facilitate initialization, the port logic is designed so that registers associated with an unrequired capability are ignored and do not have to be programmed.

1.3.1.2 Port C

The function of the special-purpose 4-bit port, Port C (Figure 1-3), depends upon the roles of Ports A and B. Port C provides the handshake lines when required by the other two ports. A REQUEST/$\overline{\text{WAIT}}$ line can also be provided by Port C so that transfers by Ports A and B can be synchronized with DMAs or CPUs. Any bits of Port C not used as handshake lines can be used as I/O lines or as external access to Counter/Timer 3.

Since Port C's function is defined primarily by Ports A and B (besides the internal Input Data and Output Data registers, which are accessed as in Ports A and B), only the three bit path registers are needed: the Data Path Polarity register, the Data Direction register, and the Special I/O Control register.

1.3.2 Counter/Timers

The three counter/timers (Figure 1-4) are all identical. Each is composed of a 16-bit down-counter, a 16-bit Time Constant register (which holds the value loaded into the down-counter), a 16-bit Current Count register (used to read the contents of the down-counter), and two 8-bit registers for control and status (the Mode Specification and the C/T Command and Status registers).

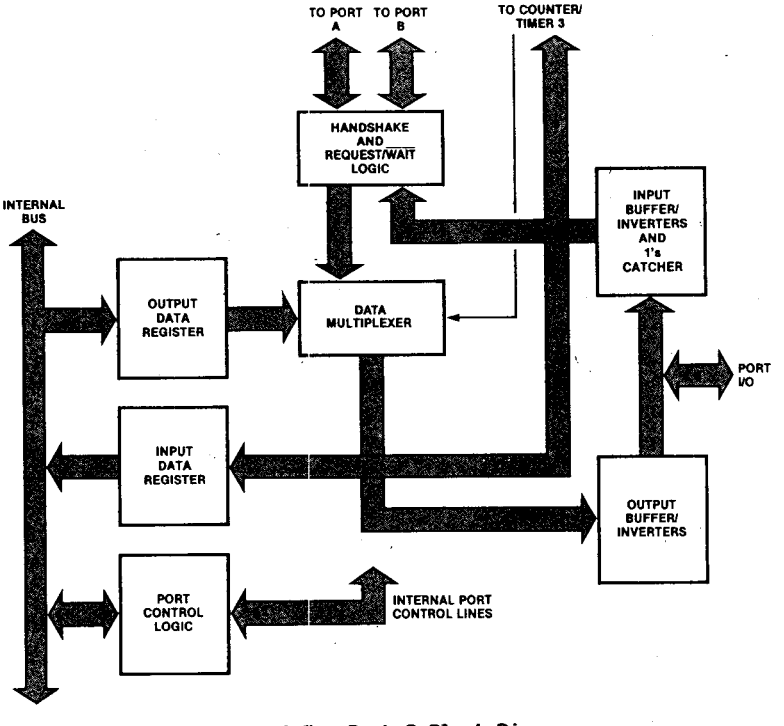

Figure 1-3. Port C Block Diagram

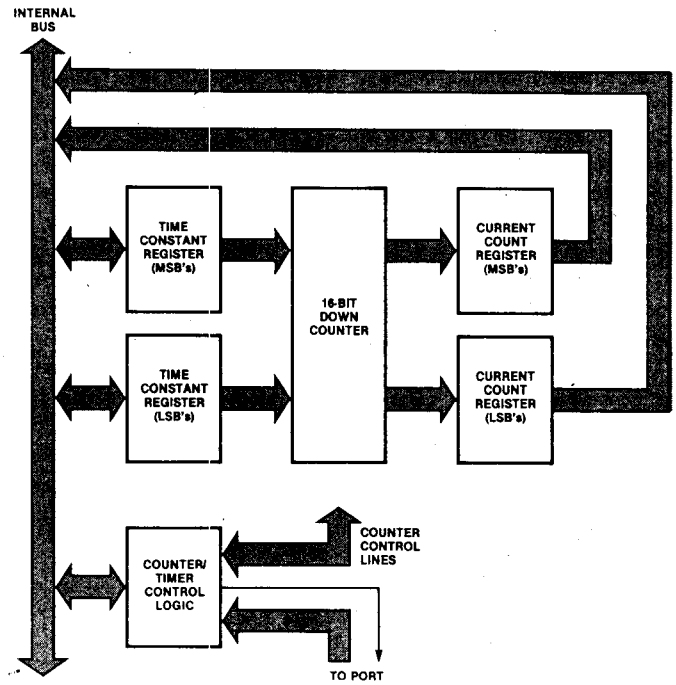

Figure 1-4. Counter/Timer Block Diagram

Up to four port pins (counter input, gate input, trigger input, and counter/timer output) can be used as dedicated external access lines for each counter/timer. Three different counter/timer output duty cycles are available: pulse, one-shot, and square-wave. The operation of the counter/timers can be programmed as either retriggerable or non-retriggerable.

1.3.3 Interrupt Control Logic

The Z8036 and Z8536 interrupt control logic provides the basis for standard Z-BUS and non-Z-BUS interrupt handling capabilities. (See Z-BUS Component Interconnect Summary, Zilog Data Book.) There are five registers (the Master Interrupt Control register, the Current Vector register, and the three Interrupt Vector registers) associated with the interrupt logic. In addition, each Port and Counter/Timer Command and Status register includes three bits associated with the interrupt logic: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE).

Chapter 2
Register Description

2.1 INTRODUCTION

This chapter provides brief descriptions of the command, status and data registers contained in the CIO. Each description includes the register address, the operation of the individual bits, and the state of the register after a reset (hardware or software).

For simplicity, the descriptions assume that the data path polarity of each bit is programmed to be non-inverting. Table 2-1 is a summary of the 48 CIO registers arranged in functional and numerical order. The binary internal addresses are the 6 bits written to an internal Pointer register as the addresses A_0-A_5. The details of the addressing schemes are described in Section 2.2 for the Z8036 and Section 2.3 for the Z8536.

For more complete discussions of the features and modes of operation of the CIO specified by these bits, refer to the appropriate chapters:

Chapter 3 Port Operation
Chapter 4 Counter/Timer Operation
Chapter 5 Interrupt Operation
Chapter 6 Initialization

Table 2-1. Z8036/Z8536 Z-CIO/CIO Register Summary

Internal Address (Binary)	Read/Write	Register Name
$A_5..A_0$		**Main Control Registers**
000000	R/W	Master Interrupt Control
000001	R/W	Master Configuration Control
000010	R/W	Port A Interrupt Vector
000011	R/W	Port B Interrupt Vector
000100	R/W	Counter/Timer Interrupt Vector
000101	R/W	Port C Data Path Polarity
000110	R/W	Port C Data Direction
000111	R/W	Port C Special I/O Control
		Most Often Accessed Registers
001000	*	Port A Command and Status
001001	*	Port B Command and Status
001010	*	Counter/Timer 1 Command and Status
001011	*	Counter/Timer 2 Command and Status
001100	*	Counter/Timer 3 Command and Status
001101	R/W	Port A Data**
001110	R/W	Port B Data**
001111	R/W	Port C Data**

Table 2-1. Z8036/Z8536 Z-CIO/CIO Register Summary--Continued

Internal Address (Binary)	Read/Write	Register Name
		Counter/Timer Related Registers
010000	R	Counter/Timer 1 Current Count MS Byte
010001	R	Counter/Timer 1 Current Count LS Byte
010010	R	Counter/Timer 2 Current Count MS Byte
010011	R	Counter/Timer 2 Current Count LS Byte
010100	R	Counter/Timer 3 Current Count MS Byte
010101	R	Counter/Timer 3 Current Count LS Byte
010110	R/W	Counter/Timer 1 Time Constant MS Byte
010111	R/W	Counter/Timer 1 Time Constant LS Byte
011000	R/W	Counter/Timer 2 Time Constant MS Byte
011001	R/W	Counter/Timer 2 Time Constant LS Byte
011010	R/W	Counter/Timer 3 Time Constant MS Byte
011011	R/W	Counter/Timer 3 Time Constant LS Byte
011100	R/W	Counter/Timer 1 Mode Specification
011101	R/W	Counter/Timer 2 Mode Specification
011110	R/W	Counter/Timer 3 Mode Specification
011111	R	Current Vector
		Port A Specification Registers
100000	R/W	Port A Mode Specification
100001	R/W	Port A Handshake Specification
100010	R/W	Port A Data Path Polarity
100011	R/W	Port A Data Direction
100100	R/W	Port A Special I/O Control
100101	R/W	Port A Pattern Polarity
100110	R/W	Port A Pattern Transition
100111	R/W	Port A Pattern Mask
		Port B Specification Registers
101000	R/W	Port B Mode Specification
101001	R/W	Port B Handshake Specification
101010	R/W	Port B Data Path Polarity
101011	R/W	Port B Data Direction
101100	R/W	Port B Special I/O Control
101101	R/W	Port B Pattern Polarity
101110	R/W	Port B Pattern Transition
101111	R/W	Port B Pattern Mask

* All bits can be read and some bits can be written.

** Also directly addressable in Z8536 using pins A_0 and A_1. (See Table 2-2 and Figures 8-1 and 8-2.)

2.2 REGISTER ADDRESSING FOR THE Z8036 (Z-CIO)

Register addressing in the Z8036 is accomplished through the use of an internal Pointer register. The Z8036 takes the contents of the multiplexed Address/Data bus and gates a subset of them into the internal Pointer register when $\overline{AS}$ is Low. The internal Pointer register identifies which register will be accessed during the subsequent part of this cycle.

The Z8036 provides two schemes for selecting the desired six of the eight address bits. The scheme to be used is determined by the Right Justify Address (RJA) bit in the Master Interrupt Control register. When RJA = 0, Address bus bits 0 and 7 are ignored, and bits 1 through 6 are decoded for the register address (A_0 derives from AD_1, A_5 derives from AD_6). When RJA = 1, address bits 0 through 5 are decoded for the register address (A_0 derives from AD_0, A_5 derives from AD_5). In the following register descriptions, only six bits are shown for addressing--they represent Address/Data bus bits 5 through 0 or 6 through 1, depending on the state of the RJA bit.

2.3 REGISTER ADDRESSING FOR THE Z8536 (CIO)

The registers in the Z8536 are accessed in a two-step sequence with pins A_0 and A_1 = 1. In the first step, a 6-bit address (the least-significant 6 bits of the Data bus) is written to an internal Pointer register. In the second step, the register identified by the Pointer register is read from or written to.

The data registers for the Z8536 Ports A, B, and C can be accessed by this sequence. The data registers can also be directly addressed by use of device pins A_0 and A_1, as shown in Table 2-2.

Table 2-2. Port Data Register Addressing for the CIO

Data Register	Address Line A_1	A_0
Port C	0	0
Port B	0	1
Port A	1	0
Control	1	1

The Z8536 contains a state machine which determines if accesses with A_0 and A_1 = 1 (see Table 2-2) are to the Pointer register or to an internal control register. (Refer to Figure 2-1 for the following discussion.) Reads in State 0 leave the state machine in State 0. Writes to the Z8536 in State 0 update the Pointer register and put the state machine into State 1. Accesses in State 1 are to the register addressed by the Pointer register, and cause the state machine to revert to State 0. State changes occur only when pin A_0 = pin A_1 = 1. Direct accesses of the data registers have no effect on state machine operation.

After any control read operation (pin A_0 = pin A_1 = 1), the state machine is in State 0 (the next control access is to the Pointer register). This can be used to force the state machine into a known state. Control reads in State 0 return the contents of the last register pointed to. Therefore, a register can be read continuously without writing to the pointer. While the Z8536 is in State 1 (next control access is to the register pointed to), many internal operations are suspended, Interrupt Pending (IP) cannot be set, and internal status is frozen. Therefore, to minimize interrupt latency and to allow continuous status updates, **the Z8536 should not be left in State 1.**

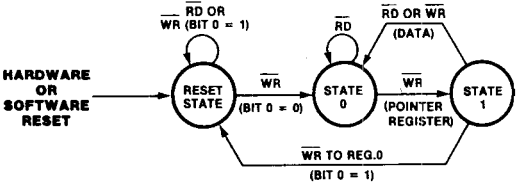

Figure 2-1. Z8536 State Machine Operation

2.4 MASTER CONTROL REGISTERS

The Master Control registers consist of the Master Interrupt Control register and Master Configuration Control register. These registers provide primary controls for the interrupt logic, port and counter/timer enable bits, port and counter/timer link bits and the RESET bit.

2.4.1 Master Interrupt Control Register

The Master Interrupt Control register contains the primary control bits for the interrupt control logic. When the device is reset all bits in all device registers are forced to 0 except RESET, which is set to 1. The RJA bit (D_1) is only

applicable to the Z8036 Z-CIO. All bits in the Master Interrupt Control register are Read/Write.

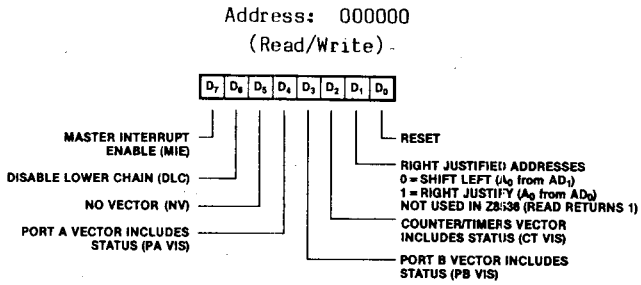

Figure 2-2. Master Interrupt Control Register.

Master Interrupt Enable--MIE (D_7). Clearing this bit to 0 inhibits the device from requesting an interrupt or responding to an Interrupt Acknowledge. Its effect is the same as pulling the Interrupt Enable In (IEI) input Low, except that the daisy-chain is left intact. A 1 in this bit allows the interrupt logic to operate normally.

The MIE bit also affects whether or not status is included when reading interrupt vectors. If MIE = 0, interrupt vector reads do not include status. If MIE = 1, vector reads always include status, independent of the state of the corresponding Vector Includes Status (VIS) bit.

Disable Lower Chain--DLC (D_6). If DLC is set to 1, the Interrupt Enable Out (IEO) output of the device is forced Low, disabling interrupts from all lower-priority devices on the daisy-chain. When DLC is 0, IEO operates normally.

No Vector--NV (D_5). When NV is set to 1, the device is inhibited from outputting an interrupt vector during an Interrupt Acknowledge cycle. This allows the vector to be provided by external hardware. It has no effect on the setting of the Interrupt Under Service (IUS) bit. If NV is written with 0, the interrupt vector is output as usual.

Port A Vector Includes Status--PA VIS (D_4). If this bit is 0 when a Port A interrupt is acknowledged, the interrupt vector that is output is the unmodified content of the Port A Interrupt Vector register. If this bit is written with a 1, the Port A base vector is modified to include status, which indicates the cause of the interrupt. Vector modification is described in Section 5.3.4. The state of this bit has no effect on the value returned when the Port A Interrupt Vector register is read. When reading the vector, the MIE bit determines if status is included in the vector, (that is, no status is included if MIE = 0).

Port B Vector Includes Status--PB VIS (D_3). This bit controls whether or not the Port B interrupt vector includes status. It operates the same way that the PA VIS bit controls the Port A interrupt vector.

Counter/Timer Vector Includes Status--CT VIS (D_2). This bit controls whether or not the base interrupt vector shared by the three counter/timers includes status. It operates the same way that the other two VIS bits (PA VIS and PB VIS) operate.

Right Justified Address--RJA (D1). (Z8036 only). When this bit is 0, the register address is shifted left one bit (see Section 2.2). Address bit A_0 is derived from Address/Data bus bit AD_1. When set to 1, the address is right justified, (for example, $A_0 = AD_0$).

The Z8536 does not use RJA--this bit is always set to 1, which causes the address to always be right-justified.

RESET--(D_0). Setting the RESET bit to 1 by a software write resets the device. The bit can also be set by a hardware reset on the Z8036 by forcing Address Strobe ($\overline{AS}$) and Data Strobe ($\overline{DS}$) Low simultaneously; or on the Z8536 by forcing Read ($\overline{RD}$) and Write ($\overline{WR}$) Low simultaneously. While RESET is 1, reads of all other registers will be 0 and writes to other registers are ignored. This bit is cleared only by writing a 0 to the RESET bit (see Sections 6.2 and 6.3).

2.4.2 Master Configuration Control Register

The Master Configuration Control register contains the control bits used to enable different sections of the device after they are initially configured, as well as the bits used to link the ports together and the timers together. All bits are cleared to 0 by resetting the device. The register is read/write.

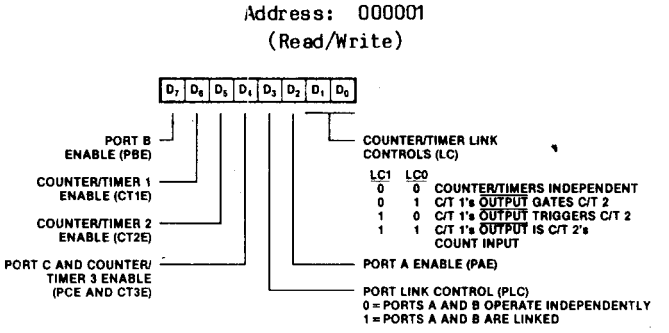

Figure 2-3. Master Configuration Control Register

Port B Enable--PBE (D_7). This bit, when set to 1, allows Port B to operate normally. When cleared to 0, it inhibits the Port B logic from issuing an interrupt request (its IP cannot be set); however, if IP was already set, clearing PBE does not clear IP. While cleared to 0, PBE inhibits READY/$\overline{WAIT}$ assertion, holds all 1's catchers in a transparent condition, and forces the Port B I/O lines into a high-impedance state. The purpose of this bit is to allow Port B to be configured initially without setting its IP erroneously or having its I/O lines go low-impedance until it is safe to do so.

Counter/Timer 1 Enable--CT1E (D_6). When cleared to 0, Counter/Timer 1 is put into an initialized state: its IP cannot be set (however, if IP was already set, clearing CT1E does not clear IP), the Count In Progress (CIP) flag is cleared, Read Counter Control (RCC) is forced to 0, and all trigger inputs are ignored. Setting CT1E to 1 allows the counter/timer to function normally.

Counter/Timer 2 Enable--CT2E (D_5). The CT2E bit performs the same function for Counter/Timer 2 that CT1E performs for Counter/Timer 1.

Port C and Counter/Timer 3 Enable--PCE and CT3E (D_4). This bit enables both Port C and Counter/Timer 3. The function is the same as D_7 (PBE) and D_6 (CT1E) for Port B and Counter/Timer 1, respectively. In addition, while this bit is cleared to 0, the handshake logic for Ports A and B is forced into an idle state and the internal Acknowledge Input ($\overline{ACKIN}$) signal is forced High. This allows the start-up of handshake operations to be precisely controlled.

Port Link Control--PLC (D_3). When PLC is set to 1, Ports A and B are linked to form a 16-bit port. In this mode, only the Port A Handshake Specification and Command and Status registers are used. Port B must be specified as a bit port and its pattern match capability must be disabled. Also, when linked, the Port B data register must be read or written before the Port A data register. A 0 in the PLC bit allows the ports to operate independently. If the ports are to be linked, this bit must be set before the ports are enabled.

Port A Enable--PAE (D_2). The Port A Enable bit performs the same function for Port A that the Port B Enable bit (D_7) performs for Port B.

Counter/Timer Link Controls--LC_1 & LC_0 (D_1 & D_0). These two bits specify if and how Counter/Timers 1 and 2 are linked. The Counter/Timers must be linked before they are enabled. The various configurations are shown in Table 2-3.

Table 2-3. Counter/Timer Link Controls

LC_1	LC_0	Configuration
0	0	Counter/Timers are independent
0	1	Counter/Timer 1's output (inverted) gates Counter/Timer 2
1	0	Counter/Timer 1's output (inverted) triggers Counter/Timer 2
1	1	Counter/Timer 1's output (inverted) is Counter/Timer 2's count input (Counter/Timer 2's External Count Enable* bit must be cleared to 0)

* (See Section 2.9.1 for description of External Count Enable bit.)

2.5 PORT SPECIFICATION REGISTERS

Each of these registers define the port operating mode, specify the type of handshake (if one is used), and contain the command and status bits used to affect data transfers of its port. There is a set of Port Specification registers for both Port A and Port B.

2.5.1 Port Mode Specification Registers

Each Port Mode Specification register contains the bits that define the operating mode of its port and specify the operation of pattern match logic of the port. A reset forces all bits to be cleared to 0. All bits are read/write.

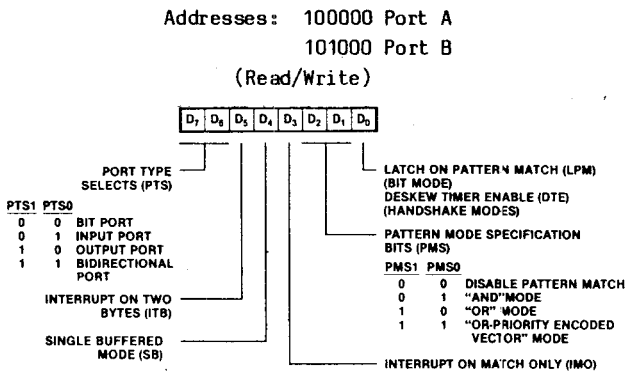

Figure 2-4. Port Mode Specification Registers

Port Type Selects--PTS_1 & PTS_0 (D_7 & D_6). The port type is specified by these two bits, as shown in Table 2-4.

Table 2-4. Port Type Selects

PTS_1	PTS_0	Port Type
0	0	Bit port (no handshake)
0	1	Input port with one of four handshakes*
1	0	Output port with one of four handshakes*
1	1	Bidirectional port with one of two handshakes**

* The four handshakes are: Interlocked, Pulsed, Strobed, or 3-wire.

** The two handshakes are: Interlocked or Strobed.

Interrupt on Two Bytes--ITB (D_5). For a port programmed with handshake, this bit indicates when an interrupt should be requested. If ITB is set to 1, IP is set when two bytes of data can be read or written. For an input port, IP is set when both the Input Data register and Buffer register are full. For an output port, IP is set when both the Output Data and Buffer register are empty. When ITB is cleared to 0, IP is set whenever a single byte of data is available to be moved (the Input Data register is full or the Output Data register is empty). This bit must always be cleared to 0 for ports specified either as bit ports, single-buffered ports (SB = 1), or bidirectional ports.

ITB also affects the operation of the Request line. When ITB = 0, the Request line will go active as soon as the device is ready for a data transfer. For input ports, the Request line will go High when the Input Data register is full. If ITB = 1, both the Buffer register and Input Data register must be full for Request to go active. For output ports with ITB = 0, the Request line will go High when the Output Data register is empty. If ITB = 1, the Request line will go High when both the Buffer register and Output Data registers are empty. In either case, the Request line will stay active as long as a byte is available to be read or written.

Single Buffer--SB (D_4). For a port programmed with handshake, this bit specifies if the port should be single- or double-buffered. When SB is cleared to 0, the port is double-buffered. When SB is set to 1 (ITB must be 0), the port is single-buffered: an input byte is loaded into both the Buffer and Input Data registers, or an output byte is loaded into both the Output Data and Buffer registers. This bit must always be cleared to 0 for bit ports.

Interrupt on Match Only--IMO (D_3). For ports with handshake (when this bit is set to 1) an interrupt will be generated only when the data moved into the Input Data register or out of the Output Data register matches the pattern specification. When cleared to 0, the port operates normally. The purpose of this bit is to allow the generation of CPU interrupts only on bytes which match the pattern specification. It is useful, for example, when the data is being moved under Direct Memory Access (DMA) control. IMO must be 0 if either SB or ITB are set to 1 or if the port is a bit port.

Pattern Mode Specification Bits--PMS_1 & PMS_0 (D_2 & D_1). These two bits define the mode of operation of the pattern match logic, as is shown in Table 2-5.

Table 2-5. Pattern Mode Specification Bits

PMS_1	PMS_0	Pattern Mode
0	0	Disable Pattern Match
0	1	AND Mode
1	0	OR Mode
1	1	OR-Priority Encoded Vector mode

The OR-Priority Encoded Vector mode must not be specified for ports configured as bit ports with the Latch on Pattern Match (LPM) bit set to 1 or for ports with handshake.

Latch On Pattern Match--LPM, or Deskew Timer Enable--DTE (D_0). The LPM/DTE bit is a dual-function bit. The LPM function is active when the port is specified in bit mode; the DTE function is active when the port is specified as an output port with handshake.

The LPM bit, when set to 1, causes the port to latch the input data present at the port when a pattern match is detected. If LPM is 0, pattern matches are still detected, but the data read back from the port follows the port pins.

The DTE bit, when set to 1, activates the deskew timer to perform delay functions as set in the Port Handshake Specification register. When cleared to 0, no delay is activated (see Section 3.4.3.2).

LPM/DTE must be cleared to 0 for input ports with handshake or for bit ports whose pattern match logic is in the OR-Priority Encoded Vector mode.

2.5.2 Port Handshake Specification Registers

Each of the Port Handshake Specification registers contain the bits that specify the type of handshake, the utilization of the REQUEST/$\overline{\text{WAIT}}$ line, and the Deskew Timer Time Constant for ports programmed with handshake. These bits are ignored if the port is a bit port. A RESET forces all bits to 0. All bits are read/write.

Addresses: 100001 Port A
101001 Port B
(Read/Write)

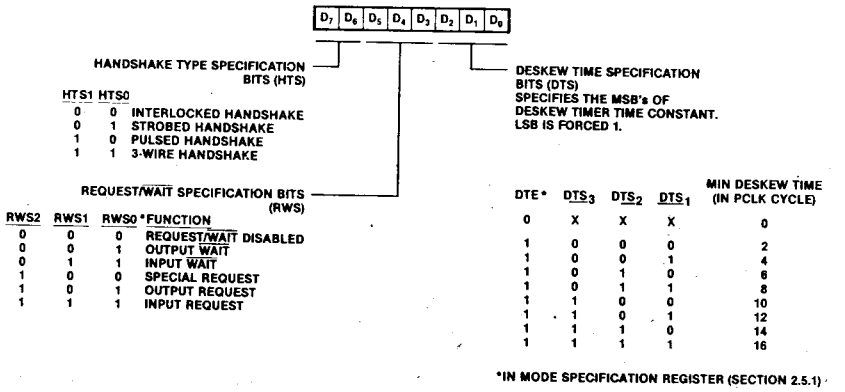

Figure 2-5. Port Handshake Specification Registers

Handshake Type Specification Bits--HTS_1 & HTS_0 (D_7 & D_6). These two bits specify the handshake type that a port with handshake will use, as is shown in Table 2-6.

Table 2-6. Handshake Type Specification Bits

HTS_1	HTS_0	Handshake Type
0	0	Interlocked Handshake
0	1	Strobed Handshake
1	0	Pulsed Handshake
1	1	3-Wire Handshake

The Pulsed Handshake and the 3-Wire Handshake must not be specified for bidirectional ports. Only one port at a time can use the Pulsed Handshake configuration. If one port uses the 3-Wire Handshake, the other port must be a bit port.

REQUEST/$\overline{WAIT}$ Specification Bits--RWS_2-RWS_0 (D_5-D_3). These three bits specify the utilization of the REQUEST/$\overline{WAIT}$ line, as is shown in Table 2-7.

Table 2-7. REQUEST/WAIT Specification Bits

RWS_2	RWS_1	RWS_0	Function
0	0	0	REQUEST/$\overline{WAIT}$ Disabled
0	0	1	Output $\overline{WAIT}$
0	1	1	Input $\overline{WAIT}$
1	0	0	Special REQUEST
1	0	1	Output REQUEST
1	1	1	Input REQUEST

If a port uses the REQUEST/$\overline{WAIT}$ capability, the other port must be programmed as a bit port, because three pins of Port C are required. (See Table 3-1.)

Deskew Time Specification Bits--DTS_3 Through DTS_1 (D_2-D_0). These three bits are the most significant bits of the Deskew Timer Time Constant. They specify the minimum amount of deskew time to be provided for output data. They define the minimum number of Peripheral Clock (PCLK) cycles of delay, 0 to 16, between the output of a new byte of data and the handshake logic indicating that new data is available ($\overline{DAV}$ falling). This logic is particularly useful in systems where large amounts of skew can exist between the data and the handshake signals or where the receiver of the data has a large set-up time requirement. The amount of deskew provided is shown in Figure 2-5.

NOTE

0 PCLK cycles deskew time is obtained by not enabling the deskew timer (DTE = 0 in the Port Mode Specification register).

2.5.3 Port Command and Status Registers

Each of these registers contain the primary command and status bits for its port. Other than the data bits themselves, these are the bits most often accessed in normal port operation. A reset forces ORE to 1 and all other bits to 0. All bits are readable and four are writeable.

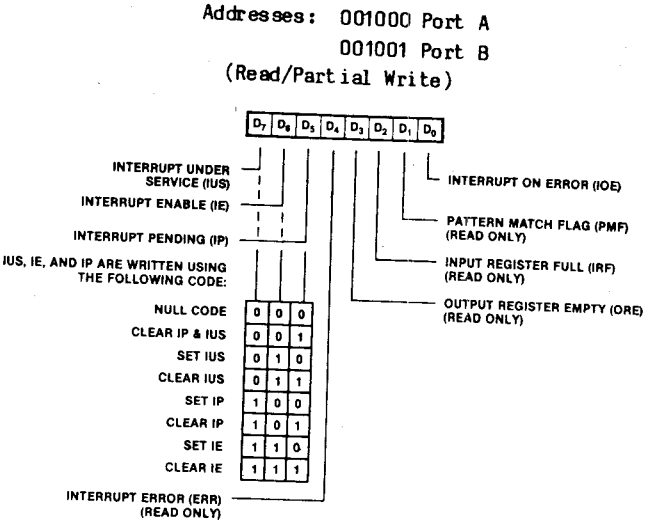

Figure 2-6. Port Command and Status Registers

Interrupt Under Service--IUS (D_7). This status bit is automatically set to 1 if its corresponding IP is the highest-priority interrupt request pending when an Interrupt Acknowledge sequence takes place. It can also be set directly by CPU command. While the IUS is set, the same and lower priority sources of interrupt are prohibited from requesting interrupts via the internal and external daisy-chains. The IUS can be cleared to 0 only by CPU command. This bit is read/write. It is changed by writing to the Command and Status register of the port using the code shown in Figure 2-6.

Interrupt Enable--IE (D_6). This bit enables or disables the port's interrupt logic. While IE is cleared to 0, the port is unable to request an interrupt or to respond to an Interrupt Acknowledge. The normal operation of IP or IUS is not affected--the IP is simply masked off from the rest of the device. A 1 in IUS still affects the interrupt daisy-chain. If IE is programmed to be 1, the interrupt logic operates normally. This bit is read/write. It is changed by writing to the Command and Status register of the port using the code shown in Figure 2-6.

Interrupt Pending--IP (D_5). IP is a status bit which, when set to 1, indicates that the port requires servicing due to a pattern match, a handshake, or an error. It is set to 1 by the port logic (or by the CPU command). If IE is also 1 and no higher-priority interrupts are under service, then the $\overline{INT}$ line is pulled Low to request an interrupt. It is cleared to 0 either automatically or by a CPU command, depending on port configuration. It is changed by writing to the Port Command and Status register using the code shown in Figure 2-6.

Interrupt Error--ERR (D_4). This status bit is automatically set to 1 along with IP when, for a bit port with pattern match enabled, a second match occurs before a previous match is acknowledged (IP is still set). If the port Interrupt On Error (IOE) bit is 0, errors are ignored and this bit is held at 0. This bit can be cleared only by clearing the corresponding IP. This bit is a read-only bit; writes to it are ignored.

Output Data Register Empty--ORE (D_3). ORE is a status bit used in conjunction with ports, specified either as output or bidirectional ports, to indicate whether or not the Output Data register is full. It is set to 1 when a byte of data is moved out of the Output Data register as part of an output handshake. The bit can only be cleared by writing to the data register. As a bit port, ORE is forced to 1 unless OR-PEV pattern match mode is specified--in which case, ORE is forced to 0. This bit is a read-only bit; writes to it are ignored. RESET empties the Output Data register, so after a RESET the ORE is set.

Input Data Register Full--IRF (D_2). IRF is a status bit used in conjunction with ports, specified either as input or bidirectional ports, to indicate whether or not the Input Data register is full. It is automatically set to 1 when a new byte of data is available to be read as the result of an input handshake. The bit can only be cleared by reading the port data register, thus "emptying" the Input Data register and forcing the bit to 0. If the port is an output port or a bit port, this bit is always forced to 0. IRF is a read-only bit; writes to it are ignored.

Pattern Match Flag--PMF (D_1). The PMF is a status bit set to 1 when a pattern match is detected. If the port is a bit port, PMF is not latched. It reflects the state of the pattern match logic just before it is read. For the Z8036, it is updated each $\overline{AS}$. For the Z8536, it is updated every second PCLK cycle while the CIO is in State 0 (See Section 2.3). For ports with handshake, the state of the PMF is updated each time a byte of data is moved into the Input Data register or out of the Output Data register. If the port pattern match logic is not enabled ($PMS_1 = PMS_0 = 0$), the PMF is forced to 0. This is a read-only bit. Writes to it are ignored.

Interrupt on Error--IOE (D_0). While IOE is cleared to 0, error conditions in bit ports using pattern-recognition logic (a second match before a previous match is acknowledged) are ignored. However, if IOE is 1, such errors will cause IP to be set and will halt normal operation of the port until the error condition is dealt with. This bit has no meaning for ports with handshake and must be cleared to 0.

2.6 BIT PATH DEFINITION REGISTERS

The Bit Path Definition registers are used to specify the details of each bit path of each port. They define:

- whether a bit path is inverting or non-inverting
- if an output is normal or open-drain
- if a bit port input has a 1's catcher inserted in its path
- which direction the data is flowing for each bit of a bit port

Each port has a set of these registers. The four most-significant bits of each register do not exist in the registers associated with Port C (writes are ignored, reads return 1s).

2.6.1 Data Path Polarity Registers

The Data Path Polarity registers each define whether the bits in its port are inverting or non-inverting on a bit-by-bit basis.

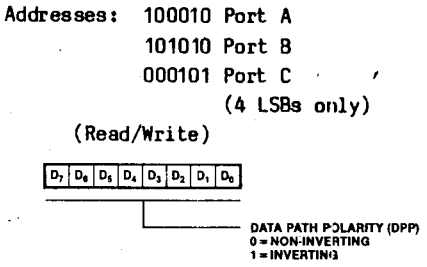

Figure 2-7. Data Path Polarity Registers

A 0 in a particular bit position of this register specifies the corresponding bit path of the port as non-inverting (that is, a High level at the port pin is 1). If a bit in this register is written with 1, the data path is programmed inverting (that is, a Low level at the pin is 1). A reset clears all bits to 0 (the port is non-inverting). The bits are read/write.

2.6.2 Data Direction Registers

Each of the Data Direction registers define the direction of data flow for the individual bits of its port if configured as a bit port. The state of this register is ignored for ports with handshake.

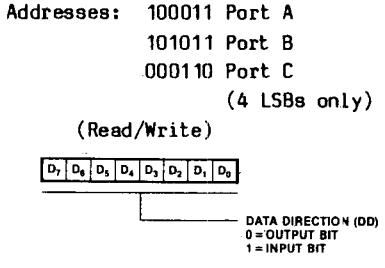

Figure 2-8. Data Direction Registers

A 0 in a bit position of this register specifies the corresponding bit of the port as an output bit, while a 1 specifies it as an input. The value programmed in this register for Ports A and B is overridden if the port is one with handshake.

An input bit specification is overridden for bits in Port C used as outputs for handshake signals or a REQUEST/$\overline{\text{WAIT}}$ line. Bits used as handshake inputs must be specified as inputs.

A reset forces all bits in these registers to 0. All bits are read/write.

2.6.3 Special I/O Control Registers

Each of the Special I/O Control registers is a dual-function register which specifies special characteristics about its port's data path. Its exact function depends on the direction of data flow defined for the path.

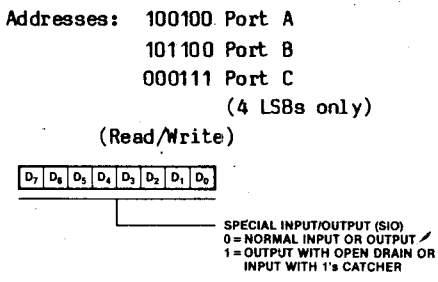

Figure 2-9. Special I/O Control Registers

If a bit is an input bit, a 1 in this register's corresponding bit position invokes a 1's catcher. A 1's catcher functions by automatically latching a 1 if its input goes to 1. It is cleared only by writing a 0 to the Input Data register. A 1's catcher is inserted into the input path after the bit's invert/non-invert logic. If the bit is programmed 0, it is a normal input bit. The 1's catcher is available only for input bit port bits.

If a bit is an output bit, a 0 in the corresponding bit position of this register specifies the output as a normal output with both a pull-up and a pull-down transistor. A 1 in this register defines the output as open-drain; no pull-up transistor is provided. The value programmed in this register applies to all output modes, independent of utilization.

A reset forces all bits to 0. All bits are read/write.

2.7 PATTERN DEFINITION REGISTERS

These registers collectively specify the match pattern for the port. As the registers must be taken together to define the pattern, they are described differently than the previous registers.

Addresses: 100101 Port A
101101 Port B
(Read/Write)

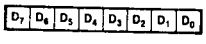

Figure 2-10. Pattern Polarity Registers

Addresses: 100110 Port A
101110 Port B
(Read/Write)

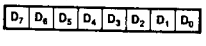

Figure 2-11. Pattern Transition Registers

Addresses: 100111 Port A
101111 Port B
(Read/Write)

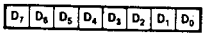

Figure 2-12. Pattern Mask Registers

A reset forces all of these registers to 0. All are read/write.

The pattern specification for each bit is defined as shown in Table 2-8.

The pattern specified by the Pattern Definition registers is a logical (not a physical) specification--this concept is important in understanding the interaction between the pattern match logic and the invert/non-invert logic. An example which shows the logical (as opposed to physical) nature of the specification is: a High level (V_{CC}) on an input pin programmed as inverting matches a 0 specification. Similarly, an output written with a 1 matches a 1 specification even if it is programmed inverting and the output pin is at a Low voltage level.

If the port is programmed as a port with handshake, or if the pattern match mode is OR-Priority Encoded Vector, the transition detection patterns should not be specified (PTn should be set to 0). If the AND mode is specified, no more than one bit should be specified to detect transitions.

2.8 PORT DATA REGISTERS

Ports A and B each have a data path that is composed of three registers: an Input Data register, an Output Data register, and a Buffer register (See Figure 1-2). Output data written to the data register is stored in the Output Data register. Reading the data register returns the contents of the Input Data register. The Buffer register is used to buffer the input and output data if the port is configured as a port with handshake. If so enabled, it is used by the bit port to latch data when a pattern match is detected.

Addresses: 001101 Port A
001110 Port B
(Read/Write)

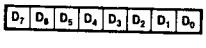

Figure 2-13. Port A and B Data Registers

Table 2-8. Pattern Specification Definition

Pattern Mask Register$_n$	Pattern Transition Register$_n$	Pattern Polarity Register$_n$	Pattern Specification
0	0	0	Bit Masked Off (X)
0	1	0	Any Transition (⇕)
1	0	0	Zero (0)
1	0	1	One (1)
1	1	0	One to Zero Transition (↓)
1	1	1	Zero to One Transition (↑)

The individual bits of the port data registers map directly onto the port I/O pins (bit 0 of the Port A Data register corresponds to the PA_0 pin, etc.).

The Port C Data register consists of two registers: an Input Data register and an Output Data register (see Figure 1-3). Output data written to the data register is stored in the Output Data register. Reading the data register returns the contents of the Input Data register. Because Port C is only four bits wide, the four least-significant bits of an 8-bit register are used for the Port C Data register. The four most-significant bits are used as a write protect mask for the four least-significant bits (bit D_7 is the write protect mask for bit D_3, etc.), as shown in Figure 2-14. Writing a 0 to the write protect mask bit enables writing to the corresponding bit in Port C. Writing a 1 inhibits writing the corresponding bit in Port C. Reading Port C always returns 1's in the upper four bits.

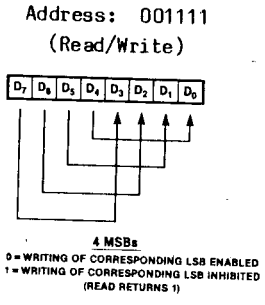

Figure 2-14. Port C Data Register

Details of the operation of these registers in the various configurations are given in Chapter 3. The data registers in the Z8536 can also be directly accessed by pin A_0 and pin A_1 (see Table 2-2).

NOTE

A reset does not effect the contents of the data registers.

2.9 COUNTER/TIMER CONTROL REGISTERS

Each counter/timer has a set of Counter/Timer Control registers, which perform several functions for the counter/timers:

- specify the mode of operation
- monitor the status
- provide control
- allow access to the down-counter so that it can be preset and read

2.9.1 Counter/Timer Mode Specification Registers

Each Counter/Timer Mode Specification register contains the bits that define its counter/timer's mode of operation and specify the external control and status lines to provide for it. A reset forces all bits to 0. All bits are read/write.

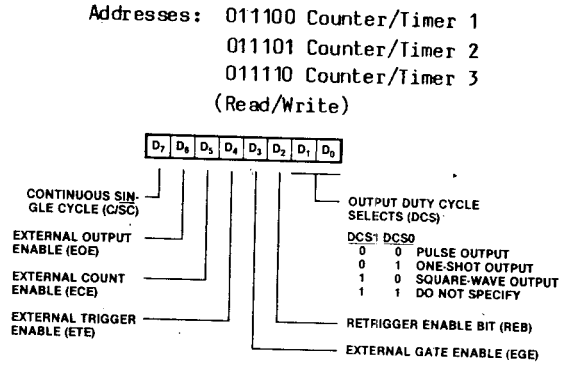

Figure 2-15. Counter/Timer Mode Specification Registers

Continuous/Single Cycle--C/$\overline{SC}$ (D_7). If C/$\overline{SC}$ is set to 1, then each time the down-counter reaches the count of 1, the time constant value is reloaded (on the next count) and the countdown sequence is repeated. If C/$\overline{SC}$ is 0 when the count of 1 is encountered (and, for square-wave outputs, if the output is a 1), the counter is allowed to count down to 0 and the countdown sequence is terminated.

External Output Enable--EOE (D_6). By programming this bit to be 1, the output of the counter/timer is provided on the I/O line of the port associated with that particular counter/timer (see Table 4-1). This bit should not be set to 1 unless the corresponding bit is available, (it is not being used as part of an input, output, or bidirectional port, or it is not being used as a handshake or REQUEST/WAIT line). The bit must be programmed to be an output bit in the Data Direction register of its port.

External Count Enable--ECE (D_5). When ECE is set to 1, the counter/timer is put into the counter mode. The I/O line of the port associated with the counter/timer (Table 4-1) is used as an external counter input. On each rising edge of the count input (when the data path is specified non-inverting), the down-counter is decremented. The bit must be available and it must be specified to be an input. (Even if the port bit is programmed as an output bit, the port pin [if enabled] is used as the counter/timer input, allowing the CPU to write this input directly.)

External Trigger Enable--ETE (D_4). When ETE is set to 1, the I/O line of the port associated with the counter/timer (see Table 4-1) is used as a trigger input to the counter/timer. A rising edge (when the data path is specified non-inverting) on this line will cause the down-counter to be loaded. To guarantee that the counter/timer will be triggered on a particular rising edge of the clocking signal (PCLK/2 or counter input), the trigger rising edge must satisfy a setup time to the preceding falling edge of the clocking signal. As in the external count input, the bit of the port must be available for use by the counter/timer, and must be programmed as an input bit. (Even if the port bit is programmed as an output bit, the port pin is used as the counter/timer input [if enabled], allowing the CPU to write this input directly.)

External Gate Enable--EGE (D_3). By setting EGE to 1, the I/O line of the port associated with the counter/timer (see Table 4-1) is used as an external gate input to the counter/timer. If the external gate input is a 0 (assuming the data path is programmed non-inverting), the countdown sequence is suspended; forcing it to a 1 enables the countdown sequence to continue. To guarantee the enabling or disabling of the counter/timer for a particular rising edge of the clocking signal (PCLK/2 or counter input), the gate input must satisfy a setup time to the preceeding falling edge of the clocking signal. Like external trigger input, the bit must be available and it must be programmed to be an input. (Even if the port bit is programmed as an output bit, the port pin is used as the counter/timer input if enabled. This allows the CPU to write this input directly.)

Retrigger Enable Bit--REB (D_2). If REB is set to 0, triggers (internal or external) which occur during a countdown sequence are ignored. If REB is 1, each trigger causes the time constant value to be reloaded and a new countdown sequence to be initiated. When a counter/timer is programmed in square-wave mode, a retrigger will cause the Time Constant value to be reloaded and the new countdown will start on the first half of the square-wave cycle.

Output Duty Cycle Selects--DCS_1 & DCS_0 (D_1 & D_0). These two bits select the output duty cycle according to the information indicated in Table 2-9.

Table 2-9. Output Duty Cycle Selects

DCS_1	DCS_0	Output Duty Cycle
0	0	Pulse Output
0	1	One-Shot Output
1	0	Square Wave Output
1	1	- DO NOT USE -

(See Section 4.2.5 for a description of each output duty cycle type.)

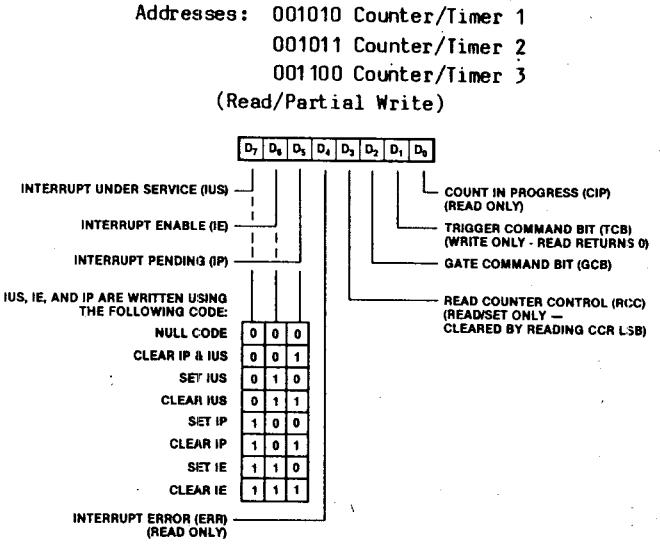

Figure 2-16. Counter/Timer Command and Status Registers

2.9.2 Counter/Timer Command and Status Registers

Each Counter/Timer Command and Status register contains the primary command and status bits for its counter/timer and (in most cases) will be the register most often accessed. A reset forces all bits to 0. The detailed bit descriptions will discuss whether or not a bit can be read or written.

Interrupt Under Service--IUS (D_7). The operation is the same as the port IUS bit.

This status bit is automatically set to 1 if its corresponding IP is the highest-priority interrupt request pending when an Interrupt Acknowledge sequence takes place. It can also be set directly by CPU command. As long as it is set, the same and lower-priority sources of interrupt are inhibited from requesting interrupts via the internal and external daisy-chains. It can be cleared only by CPU command. This bit is read/write. It is changed by writing to the Counter/Timer Command and Status register of the port using the code shown in Figure 2-16.

Interrupt Enable--IE (D_6). The operation is the same as the port IE bit.

This bit enables or disables the counter/timer's interrupt logic. When IE is cleared to 0, the counter/timer is unable to request an interrupt or to respond to an Interrupt Acknowledge. It does not affect the normal operation of IP or IUS, but simply masks IP off from the rest of the device. A 1 in IUS still affects the interrupt daisy-chain. If IE is programmed to be 1, the interrupt logic operates normally. This bit is read/write. It is changed by writing to the Counter/Timer Command and Status register of the port using the code shown in Figure 2-16.

Interrupt Pending--IP (D_5). The operation is similar to the port IP bit.

IP is a status bit which, when set to 1, indicates that the counter/timer requires servicing. It is automatically set to 1 each time the counter/timer reaches its terminal count (or by the CPU command). If IE is also 1 and no higher-priority interrupts are under service, then the $\overline{INT}$ line is pulled Low to request an interrupt. This bit is read/write. It is changed by writing to the Counter/Timer Command and Status register using the code shown in Figure 2-16.

Interrupt Error--ERR (D_4). This status bit is set along with IP to indicate that an error has occurred. An error occurs for a counter/timer whenever terminal count is reached and IP is still set from a previous terminal count. ERR can be cleared only by having software clear the IP it corresponds to. ERR is a read-only bit.

Read Counter Control--RCC (D_3). RCC is a command bit that enables the counter/timer to be read reliably while it is in a countdown sequence. Writing a 1 to RCC causes the contents of the Counter/Timer Current Count register (CCR), which normally follows the down-counter, to be frozen