



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





*Z86017/Z16017*

*PCMCIA Interface Solution*

**Product Specification**

*PS012002-1201*

## **Z86017/Z16017 PCMCIA Interface Solution Reference Manual**



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact

### **ZiLOG Worldwide Headquarters**

910 E. Hamilton Avenue  
Campbell, CA 95008  
Telephone: 408.558.8500  
Fax: 408.558.8300  
[www.ZiLOG.com](http://www.ZiLOG.com)

Windows is a registered trademark of Microsoft Corporation.

### **Document Disclaimer**

© 2001 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Except with the express written approval ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses or other rights are conveyed, implicitly or otherwise, by this document under any intellectual property rights.



# *Preface*

Thank you for your interest in Zilog's PCMCIA interface solution. This Reference Manual describes the programming and operation of the Z86017 and Z16017 PCMCIA adapter chips.

This Reference Manual is organized in the following way:

- **PCMCIA Interface Overview**  
This chapter is an introductory section that provides an overview of the architecture of the device.
- **Addressing Modes**  
This chapter describes the addressing modes supported by the Z86017/Z16017 architecture to ensure PCMCIA compatibility.
- **Programming Internal Registers**  
This chapter describes the serial interface modes.
- **Configuration Registers**  
This chapter describes the functions of the Z86017/Z16017 internal registers.
- **Appendix A**  
This appendix gives an overview of the Z86017/Z16017 multifunction pins.
- **Appendix B**  
This appendix provides Absolute Maximum Ratings, DC Electrical Characteristics, and Timing Specifications related to the Z86017/Z1601.
- **Appendix C**  
This appendix provides various Z86017/Z16017 timing diagrams.

# Z86017/Z16017 PCMCIA Interface Solution Product Specification



iv

- **Appendix D**  
This appendix provides part numbers and ordering information.
- **Appendix E**  
This appendix provides a description of the Z8601700ZCO PCMCIA Interface Development Kit.



# *Table of Contents*

<b>Preface</b> .....	<b>iii</b>
<b>Table of Contents</b> .....	<b>v</b>
<b>List of Figures</b> .....	<b>vii</b>
<b>List of Tables</b> .....	<b>xi</b>
<b>PCMCIA Interface Overview</b> .....	<b>1</b>
Features .....	1
General Description .....	2
Pin Description .....	12
Pin Identification .....	14
Pin Functions .....	18
PCMCIA Signals .....	18
Peripheral or ATA/IDE Signals .....	21
Serial Interface Signals .....	24
Peripheral Control Signals .....	25
<b>Addressing Modes</b> .....	<b>27</b>
<b>Programming Internal Registers</b> .....	<b>33</b>
Introduction .....	33
EEPROM Register .....	36
Word-to-Byte Operation .....	76
<b>Configuration Registers</b> .....	<b>79</b>



# Z86017/Z16017 PCMCIA Interface Solution Product Specification



vi

Introduction .....	79
Configuration Registers .....	80
<b>Appendix A: Multifunction Pins .....</b>	<b>87</b>
Overview of Multifunction Pins .....	87
<b>Appendix B: Electrical Characteristics and Timing .....</b>	<b>93</b>
internal attribute memory timing .....	96
017 Device Slew Delay .....	108
<b>Appendix C: Timing Examples .....</b>	<b>113</b>
<b>Appendix D: Packaging and Ordering Information .....</b>	<b>117</b>
20 Mhz PCMCIA Adapter Chips .....	117
Package .....	117
Temperature .....	117
Speed .....	117
Environmental .....	117
Package Dimensions .....	119
<b>Appendix E: PCMCIA Interface Development Kit .....</b>	<b>121</b>
General Description .....	121
Z86017 Specifications .....	121
Power Requirements: .....	121
Dimensions .....	121
Kit Contents .....	122
Evaluation Board .....	122
ZPCMCIA0ZDP PCMCIA Extender Card .....	122



# *List of Figures*

<b>Preface</b> .....	<b>iii</b>
<b>Table of Contents</b> .....	<b>v</b>
<b>List of Figures</b> .....	<b>vii</b>
<b>List of Tables</b> .....	<b>xi</b>
<b>PCMCIA Interface Overview</b> .....	<b>1</b>
Figure 1. ZX6017 Functional Block Diagram .....	3
Figure 2. Serial Port Master Mode Control .....	5
Figure 3. Serial Port Slave Mode Control .....	7
Figure 4. EEPROM Programming Through the PCMCIA Interface .....	8
Figure 5. Connection Block Diagram .....	9
Figure 6. Serial Interface Diagram .....	10
Figure 7. Attribute and Configuration Memory Diagram .....	11
Figure 8. ZX6017 100-Pin VQFP Pin Configuration .....	12
Figure 9. Z86M17 and Z16M17 (Mirror Image) 100-Pin VQFP Pin Configuration .....	13
<b>Addressing Modes</b> .....	<b>27</b>
<b>Programming Internal Registers</b> .....	<b>33</b>
Figure 10. Word-to-Byte Timing .....	76
Figure 11. Word-to-Byte Mode Data Path .....	77
<b>Configuration Registers</b> .....	<b>79</b>





<b>Appendix A: Multifunction Pins</b> .....	<b>87</b>
Figure 12. Z16017BA PC_RDY/ $\overline{\text{BSY}}$ / $\overline{\text{IREQ}}$ /HINT Pin .....	87
Figure 13. Z86017BA PC_WP//IOIS16//IOIS16 Pin .....	88
Figure 14. Z16017BA PC_WP//IOIS16//IOIS16 Pin .....	89
Figure 15. Z86017BA (Overview of Internal Structure) .....	90
Figure 16. Z16017BA (Overview of Internal Structure) .....	91
<b>Appendix B: Electrical Characteristics and Timing</b> .....	<b>93</b>
Figure 17. PCMCIA Read Memory Timing, No Wait States .....	97
Figure 18. PCMCIA Read Memory Timing, Wait State Enabled ...	98
Figure 19. PCMCIA Write Memory Timing, No Wait States .....	101
Figure 20. PCMCIA Write Memory Timing, Wait State Enabled ..	102
Figure 21. I/O Read Timing .....	104
Figure 22. I/O Write Timing .....	106
Figure 23. Skew Timing Between PCMCIA and ATA/IDE or Peripheral Bus .....	107
Figure 24. 017 Slew Delay Derating Curve (Typical) .....	108
Figure 25. FMaster Mode Read EEPROM Timing .....	110
Figure 26. Slave Interface Timing (Read) .....	111
<b>Appendix C: Timing Examples</b> .....	<b>113</b>
Figure 27. Z16017BA Reset Timing PCMCIA Mode .....	113
Figure 28. PCMCIA ATA/IDE 16-Bit I/O Write (Register 24 = 01, Internal IOIS 16 is selected) .....	114
Figure 29. PCMCIA ATA / IDE 8-Bit Long Read (Reading 512-byte data plus 6-byte ECC) .....	115
<b>Appendix D: Packaging and Ordering Information</b> .....	<b>117</b>
Figure 30. Example Package Name .....	118
Figure 31. 100-Lead VQFP Package Diagram .....	119



**Appendix E: PCMCIA Interface Development Kit .....121**

**Z86017/Z16017 PCMCIA Interface Solution  
Product Specification**



**x**



# *List of Tables*

<b>Preface</b> .....	<b>iii</b>
<b>Table of Contents</b> .....	<b>v</b>
<b>List of Figures</b> .....	<b>vii</b>
<b>List of Tables</b> .....	<b>xi</b>
<b>PCMCIA Interface Overview</b> .....	<b>1</b>
Table 1. Device Features .....	1
Table 2. Power Connections .....	2
Table 3. 100-Pin VQFP Pin Identification .....	14
<b>Addressing Modes</b> .....	<b>27</b>
Table 4. ZX6017 Addressing Modes .....	27
Table 5. Programming PCMCIA_ATA ZX6017 Configuration Registers .....	29
Table 6. PCMCIA Common Memory Mode .....	30
Table 7. PCMCIA I/O Mode .....	31
Table 8. PCMCIA_ATA Memory Mapped Access .....	31
Table 9. PCMCIA_ATA I/O Mapped Access .....	32
<b>Programming Internal Registers</b> .....	<b>33</b>
Table 10. ZX6017 Card Configuration Registers .....	33
Table 11. Interface Configuration Register: Address 00h .....	36
Table 12. Master Clock .....	38
Table 13. Interrupt Enable Register: Address 01h .....	39

# Z86017/Z16017 PCMCIA Interface Solution

## Product Specification



Table 14.	Interface Configuration Register 1: Address 02h . . . . .	41
Table 15.	PCMCIA PDIAG Pin Functions . . . . .	42
Table 16.	PCMCIA DASP Pin Functions . . . . .	43
Table 17.	Host Chip Select Designations . . . . .	44
Table 18.	Audio Pin Configurations . . . . .	44
Table 19.	Interface Configuration Register 2: Address 03h . . . . .	45
Table 20.	Interface Configuration Register 3: Address 04h . . . . .	46
Table 21.	ATA Register Selection Designations . . . . .	47
Table 22.	Reset Conditions . . . . .	47
Table 23.	PCMCIA CCR Base Address Register: Address 05h . . . . .	48
Table 24.	CCR Location Examples, Register 5 . . . . .	49
Table 25.	PCMCIA Interrupt Status Register: Address 06h . . . . .	50
Table 26.	PCMCIA Exception Status Register: Address 07h . . . . .	51
Table 27.	ATA Sample Mode Bit . . . . .	52
Table 28.	Attribute Memory Address Register: Address 08h . . . . .	52
Table 29.	Attribute Memory Data Register: Address 09h . . . . .	53
Table 30.	Window 1 Control Register: Address 10h . . . . .	54
Table 31.	Window 1 Start Address LSB: Address 11h . . . . .	55
Table 32.	Window 1 Start/Range Address MSB: Address 12h . . . . .	55
Table 33.	Window 1 Range Address LSB: Address 13h . . . . .	56
Table 34.	Window 2 Control Register: Address 14h . . . . .	56
Table 35.	Window 2 Start Address LSB: Address 15h . . . . .	57
Table 36.	Window 2 Start/Range Address MSB: Address 16h . . . . .	58
Table 37.	Window 2 Range Address LSB: Address 17h . . . . .	58
Table 38.	Window 3 Control Register: Address 18h . . . . .	59
Table 39.	Window 3 Start Address LSB: Address 19h . . . . .	60
Table 40.	Window 3 Start/Range Address MSB: Address 1Ah . . . . .	60
Table 41.	Window 3 Range Address LSB: Address 1Bh . . . . .	61



Table 42.	EEPROM Valid flag Byte Register: Address 1Eh . . . . .	61
Table 43.	EEPROM Address/Status CCR5 Back Door: Address 20h	61
Table 44.	EEPROM Data CCR6 Back Door: Address 21h . . . . .	62
Table 45.	EEPROM Command CCR7 Back Door: Address 22h . . .	62
Table 46.	Revision Control Register: Address 23h . . . . .	63
Table 47.	Revision Number Register: Address 24h . . . . .	63
Table 48.	Bus Control 1 Register: Address 26h . . . . .	64
Table 49.	IOIS16 Address Control Register: Address 27h . . . . .	66
Table 50.	16-Bit_Control . . . . .	67
Table 51.	8-Bit_CTRL . . . . .	67
Table 52.	Power Management Timer Count Value: Address 2Ah . .	68
Table 53.	Power Management control Register: Address 2Bh . . . . .	69
Table 54.	Interface Configuration Register 4: Address 2Ch . . . . .	70
Table 55.	Power Management Clock Select . . . . .	71
Table 56.	Configuration Index Compare Register 1: Address 2Dh .	72
Table 57.	Configuration Index Compare Register 2: Address 2Eh .	72
Table 58.	Bus Control Register: Address 2Fh . . . . .	74
Table 59.	Strobe Width and Access Delay . . . . .	75
Table 60.	PCMICA Host Read and Write Address Examples, . . . . .	78

**Configuration Registers . . . . .79**

Table 61.	PCMCIA Address xx0h to xx8h, Configuration Register De- code . . . . .	79
Table 62.	ZiLOG EEPROM Programming Extensions . . . . .	80
Table 63.	PCMCIA Configuration Option Register CCR0: Address 0Ah . . . . .	80
Table 64.	PCMCIA Card Status Register CCR1: Address 0Bh . . . . .	81
Table 65.	PCMCIA Pin Replacement Register CCR2: Address 0Ch .	82
Table 66.	PCMCIA socket and Copy Register CCR3: Address 0Dh .	83



Table 67.	PCMCIA I/O Event Indication CCR4: Address 1Fh . . . . .	84
<b>Appendix A: Multifunction Pins . . . . .</b>		<b>87</b>
<b>Appendix B: Electrical Characteristics and Timing . . . . .</b>		<b>93</b>
Table 68.	Absolute Maximum Ratings . . . . .	93
Table 69.	DC Electrical Characteristics . . . . .	94
Table 70.	Internal Attribute Memory Timing . . . . .	96
Table 71.	PCMCIA Memory Write Timing . . . . .	99
Table 72.	I/O Read Timing Specification . . . . .	103
Table 73.	I/O Write Timing Specification . . . . .	105
Table 74.	Skew Timing Between PCMCIA And ATA/IDE or Peripheral Bus . . . . .	106
Table 75.	Serial Interface Timing . . . . .	109
<b>Appendix C: Timing Examples . . . . .</b>		<b>113</b>
<b>Appendix D: Packaging and Ordering Information . . . . .</b>		<b>117</b>
<b>Appendix E: PCMCIA Interface Development Kit . . . . .</b>		<b>121</b>





# *PCMCIA Interface Overview*

## FEATURES

**Table 1. Device Features**

Device	RAM (Bytes)	Speed	Package
Z86017	256	20	100-Pin VQFP
Z86M17 <sup>1</sup>	256	20	100-Pin VQFP
Z16017	256	20	100-Pin VQFP
Z16M17 <sup>1</sup>	256	20	100-Pin VQFP

NOTES:

1. Mirror Image Bond-Out Options

- PCMCIA Configuration Registers
- Sequencer for programming attribute memory using EEPROM content, MASTER mode
- Serial Peripheral Interface (SPI) circuitry allows control through the local microprocessor, SLAVE mode
- PCMCIA to I/O peripheral
- PCMCIA to ATA/IDE translation
- ATA/IDE to ATA/IDE mapping, PASSHROUGH mode
- Operates from a 3.0V to 5.5V power supply
- Conforms to PCMCIA standards
- Low power dissipation
- Mirror image bond-out option (Z86M17/Z16M17)
- On-chip generation of IOIS16 in I/O mode (Z16017)



## General Description

The Z86017/Z16017 (ZX6017) are general-purpose PCMCIA adapter chips used on the card side of the interface. For increased versatility, “mirror image” bond-out versions, the Z86M17 and Z16M17, are also available. These chips are easily configured to allow access to all types of memory or I/O-mapping peripherals, such as Ethernet controllers, Universal Asynchronous Receiver/Transmitters (UART), modems, rotating disk memory, and so on. The ZX6017 can be used in a stand-alone configuration without the use of a local processor when all necessary data for Attribute Memory, Card Configuration Registers (CCR), Memory/I/O maps, and so on, are being provided by a local serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The ZX6017 can also be configured by a local microprocessor, when one is being used on the card.

Throughout this document, references to the ZX6017 device applies equally to the Z86017 and Z16017, unless otherwise specified.

► **Note:** All Signals with an overline ( $\bar{\quad}$ ) are active Low, that is,  $B/\bar{W}$  (WORD is active Low);  $\bar{B}/W$  (BYTE is active Low, only).

Power connections follow conventional descriptions below:

**Table 2. Power Connections**

Connection	Circuit	Device
Power	$V_{CC}$	$V_{DD}$
Ground	GND	$V_{SS}$

The ZX6017 can be programmed by one of two ways: an external 256 byte serial EEPROM can be connected to the serial port interface, or a microprocessor can be connected to this port to provide a higher level of control. [Figure 1](#) depicts the functional block diagram for the ZX6017.

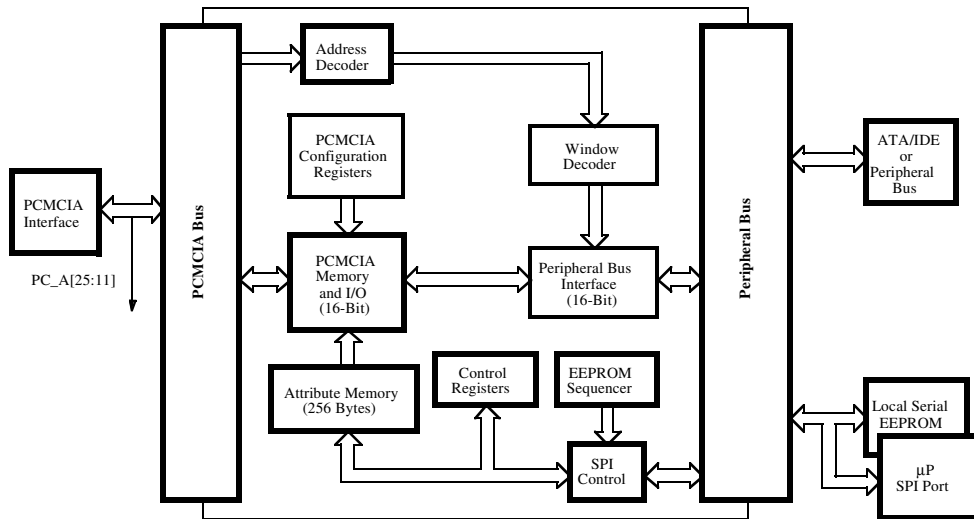


Figure 1. ZX6017 Functional Block Diagram

## Power-On Reset

The ZX6017 defaults to the Memory Only interface as outlined in the PCMCIA specification upon deassertion of Power-On Reset ( $\overline{\text{POR}}$ ). The hardware sets Busy on the PC\_RDY/BSY pin and then addresses the EE\_MASTER pin. If the EE\_MASTER pin is unconnected or pulled High, the ZX6017 serial interface defaults to the Master mode and an external EEPROM is required. If this pin is pulled Low, the SLAVE mode is selected and an external microprocessor is required to configure the ZX6017 through the serial interface pins.

Next, the hardware addresses the  $\overline{\text{PC\_ATA}}/\text{HOE}$  pin. If the  $\overline{\text{PC\_ATA}}/\text{HOE}$  pin is held Low for 40 clocks (PC\_MCLK\_IN) after POR deassertion, the ZX6017 is enabled for ATA/IDE to ATA/IDE PASSTHROUGH mode. The PASSTHROUGH mode is for systems that



use the physical PCMCIA 68-pin connector but do not support PCMCIA protocol. If this pin is held High ( $\overline{PC\_ATA/HOE}$ ), the device is placed into the PCMCIA mode. The override bits in register 00H determine what mode(s) the user can support.

### **Serial Port Operation (Master) Mode**

After the ZX6017 determines that an external EEPROM is present (see [Figure 2](#)), the Ready/Busy pin on the PCMCIA interface is set to Busy. The ZX6017 internal sequencer starts up and reads EEPROM address 1eh. If EEPROM address 1Eh is loaded with a 1Ch then the EEPROM's data is considered to be valid. After that, the internal sequencer resets its address counter back to zero. Data from EEPROM's addresses [00-2F] is read out and put into the on-board registers of the ZX6017. The EEPROM sequencer then reads EEPROM addresses 30h to FFh and each byte is moved into the ZX6017 on-board attribute memory addresses 00-CFh. After loading the registers and attribute memory, the sequencer completes by clearing the Ready/Busy pin on the PCMCIA interface indicating 1 "Ready." If EEPROM address 1Eh does not contain 1Ch, then the sequencer stops. The PCMCIA Ready/Busy pin stays in the Busy state, the on-board registers of the ZX6017 remain in their default state, and attribute memory data is unknown. The user can program the off-board EEPROM through the PCMCIA interface by means of three special registers and ignore Busy.

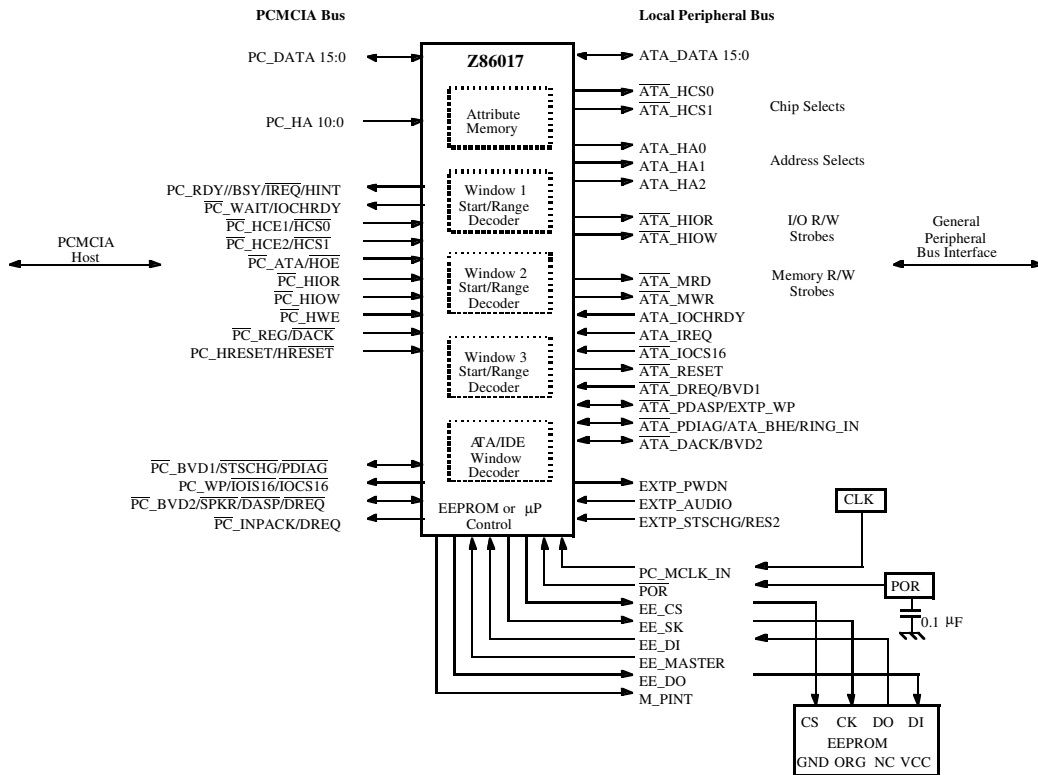


Figure 2. Serial Port Master Mode Control

## Serial Port Operation (SLAVE) Mode

When the ZX6017 is placed in serial port SLAVE mode (EE\_Master signal grounded on POR), the EEPROM sequencer is disabled and the user must provide external hardware (microprocessor) with serial interface to program CCRs and attribute memory. Additionally, if the



POR signal is deasserted, the user must provide a clock source on the PC\_MCLK\_IN pin in the range of 1-20MHz.

The external hardware can program the on-board registers and the attribute memory by selecting the ZX6017 and pulling the EE\_CS pin High. The external hardware must set up the data to be sent to the ZX6017 on the EE\_DI pin and strobe the EE\_SK pin. The first byte of data is the address selected by the user, the second byte is the command byte and the third byte is the data. The external hardware must provide 24 clocks in order to read or write to a location in the ZX6017 (see [Figure 26](#), Slave Interface Timing, in Appendix B).

To program the on-board attribute memory, the user must first write to it. Accomplish this programming by writing the address location of the attribute memory to be written (or read) in the attribute RAM data address register at location 08h. When this step has been accomplished, the user then writes (or reads) the attribute RAM data register 09h with the data to be read or written at that location.

► **Note:** The attribute RAM address register auto-increments after reading or writing to the attribute RAM data register.

[Figure 3](#) demonstrates programming the ZX6017 in SLAVE Mode. The external user's hardware writes to register 00 and selects the clock divide by and the override mode (if needed). The READY/ $\overline{\text{BUSY}}$  pin remains set to 0 to indicate BUSY, and a local  $\mu\text{P}$  interrupt polarity is selected.

The user programs registers 01-05, followed by registers 0Ah-2Fh. The user writes to the attribute memory by setting the address in the address register 08h and in the loop on data register 09h with the user's attribute memory data. The user completes the operation by writing back to register 00 to clear the READY/ $\overline{\text{READY}}$  status.

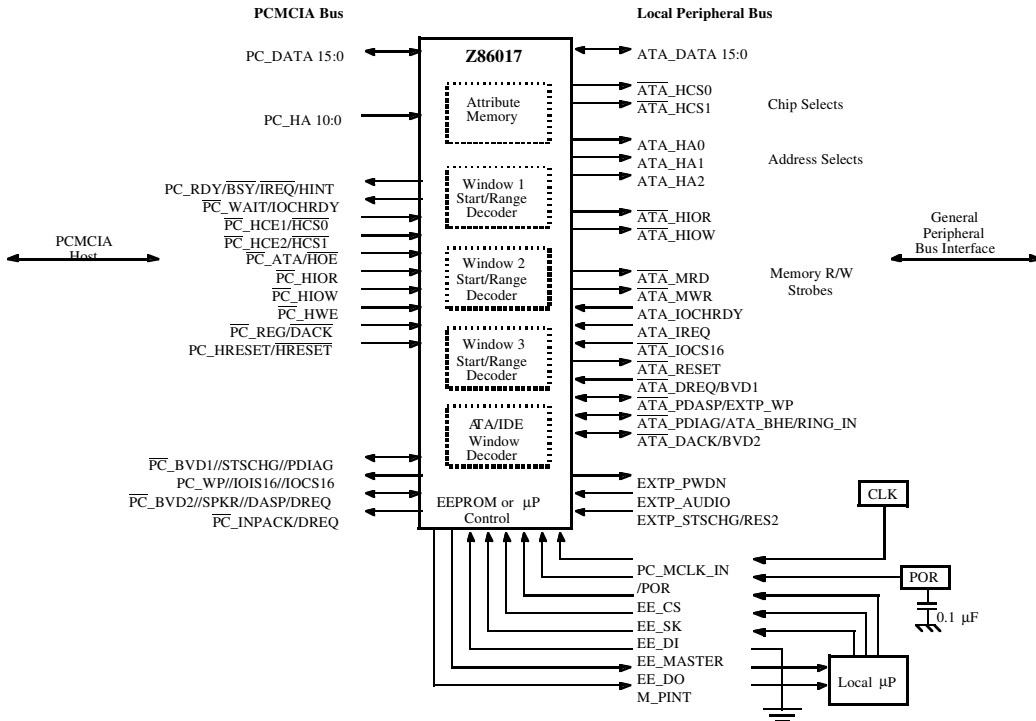


Figure 3. Serial Port Slave Mode Control

## EEPROM Programming Through the PCMCIA Interface

The ZX6017 can program the serial EEPROM through the PCMCIA interface. EEPROM programming is accomplished by means of three special registers that are accessed identically to the CCR registers as defined by the PCMCIA specification (Figure 4). These registers are fixed at addresses 7F0, 7F2, and 7F4. The software reads and writes each byte of the EEPROM through these registers and configures the

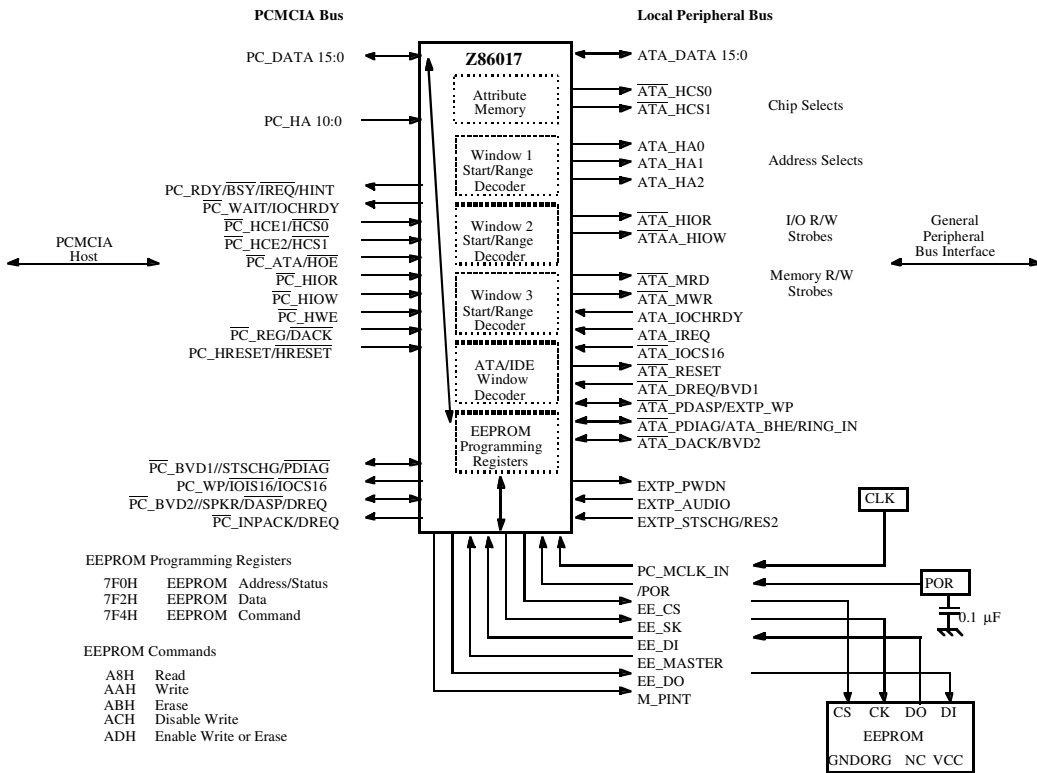


# Z86017/Z16017 PCMCIA Interface Solution Product Specification



ZX6017 device. After the host writes new values to the EEPROM through these registers, the new values are loaded into the ZX6017 at Power-On Reset ( $\overline{\text{POR}}$ ).

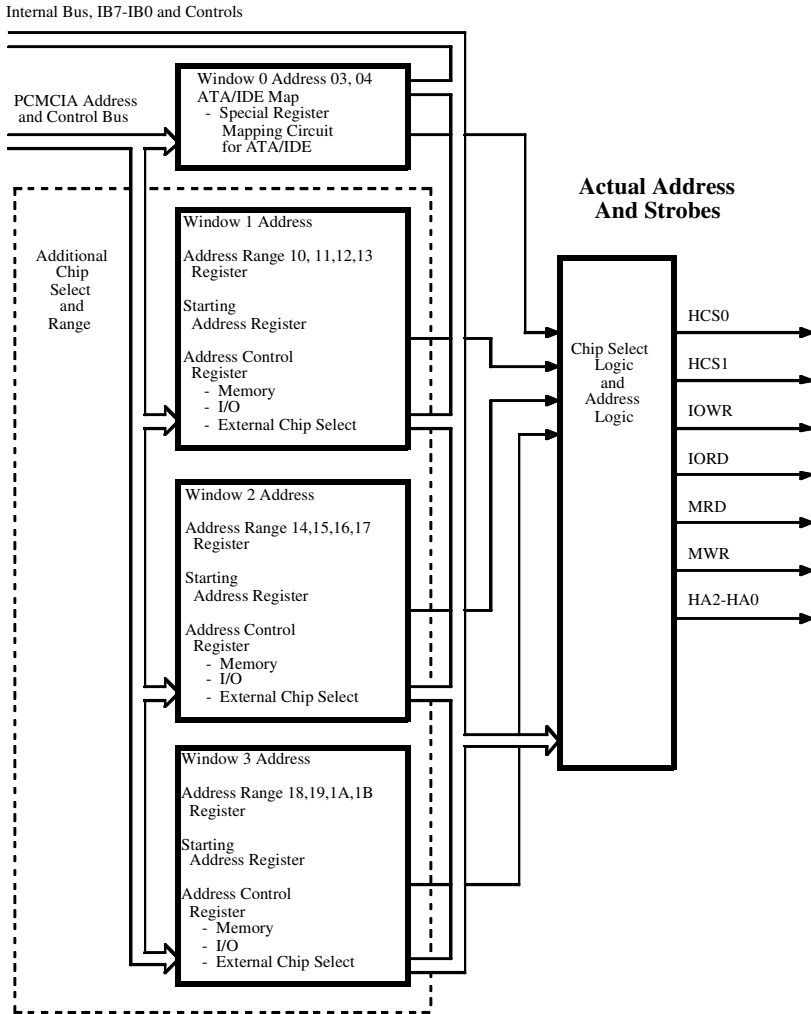
► **Note:** The values written register 05h offset the CCR registers and the three special EEPROM programming registers on the next POR.



**Figure 4. EEPROM Programming Through the PCMCIA Interface**



**Address Mapping Circuit**



**Figure 5. Connection Block Diagram**

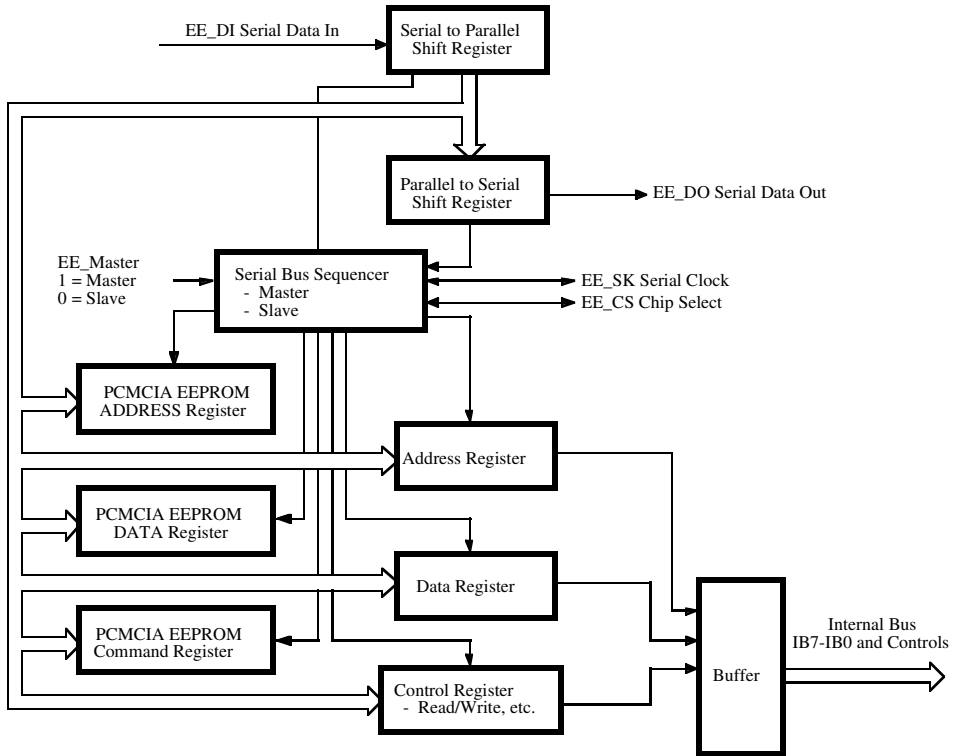


Figure 6. Serial Interface Diagram

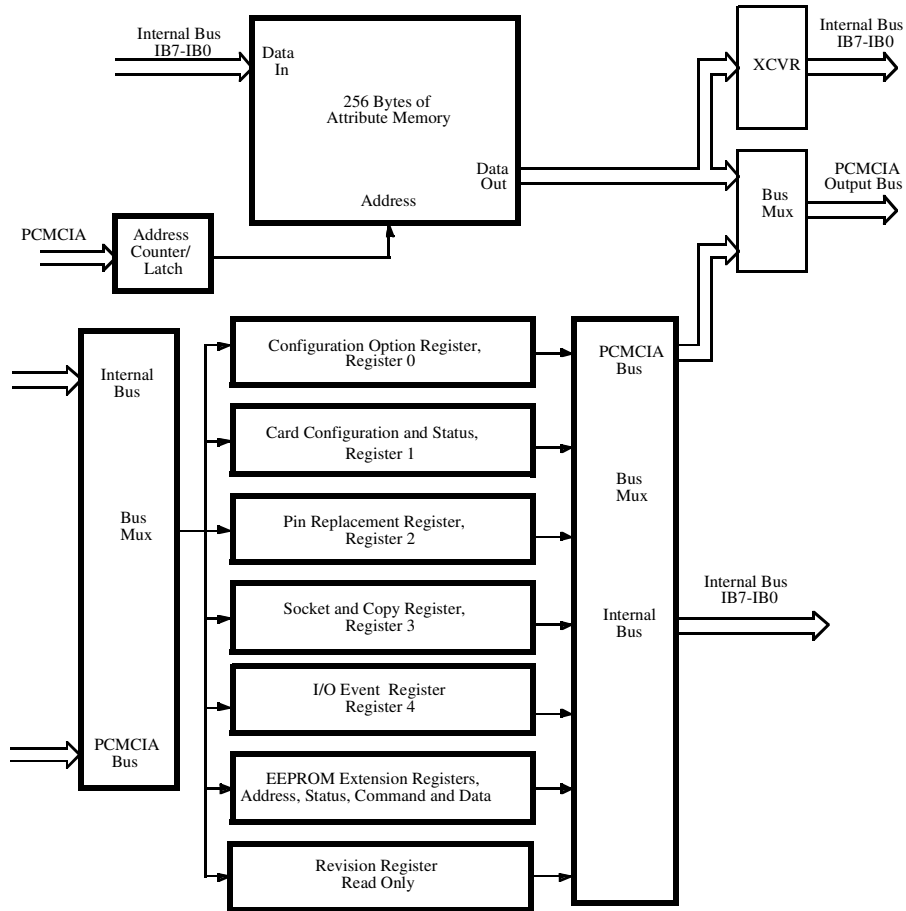


Figure 7. Attribute and Configuration Memory Diagram