Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Z86017/Z16017

PCMCIA Interface Solution

Reference Manual

RM001103-0901

ZiLOG Worldwide Headquarters • 910 E. Hamilton Avenue • Campbell, CA 95008
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

Z86017/Z16017 PCMCIA Interface Solution
Reference Manual

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact

ZiLOG Worldwide Headquarters
910 E. Hamilton Avenue
Campbell, CA 95008
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

RM001103-0901

Preface

Thank you for your interest in Zilog's PCMCIA interface solution. This Reference Manual describes the programming and operation of the Z86017 and Z16017 PCMCIA adapter chips.

This Reference Manual is organized in the following way:

- **PCMCIA Interface Overview**
  This chapter is an introductory section that provides an overview of the architecture of the device.
- **Addressing Modes**
  This chapter describes the addressing modes supported by the Z86017/Z16017 architecture to ensure PCMCIA compatibility.
- **Programming Internal Registers**
  This chapter describes the serial interface modes.
- **Configuration Registers**
  This chapter describes the functions of the Z86017/Z16017 internal registers.
- **Appendix** A
  This appendix gives an overview of the Z86017/Z16017 multifunction pins.
- **Appendix B**
  This appendix provides Absolute Maximum Ratings, DC Electrical Characteristics, and Timing Specifications related to the Z86017/ Z1601.
- **Appendix C**
  This appendix provides various Z86017/Z16017 timing diagrams.

- **Appendix D**
  This appendix provides part numbers and ordering information.
- **Appendix E**
  This appendix provides a description of the Z8601700ZCO PCMCIA Interface Development Kit.

Table of Contents

List of Figures

List of Tables

PCMCIA Interface Overview

FEATURES

Table 1. Device Features

Device	RAM (Bytes)	Speed	Package
Z86017	256	20	100-Pin VQFP
Z86M17[1]	256	20	100-Pin VQFP
Z16017	256	20	100-Pin VQFP
Z16M17[1]	256	20	100-Pin VQFP

NOTES:
1.Mirror Image Bond-Out Options

- PCMCIA Configuration Registers
- Sequencer for programming attribute memory using EEPROM content, MASTER mode
- Serial Peripheral Interface (SPI) circuitry allows control through the local microprocessor, SLAVE mode
- PCMCIA to I/O peripheral
- PCMCIA to ATA/IDE translation
- ATA/IDE to ATA/IDE mapping, PASSHROUGH mode
- Operates from a 3.0V to 5.5V power supply
- Conforms to PCMCIA standards
- Low power dissipation
- Mirror image bond-out option (Z86M17/Z16M17)
- On-chip generation of IOIS16 in I/O mode (Z16017)

General Description

The Z86017/Z16017 (ZX6017) are general-purpose PCMCIA adapter chips used on the card side of the interface. For increased versatility, “mirror image” bond-out versions, the Z86M17 and Z16M17, are also available. These chips are easily configured to allow access to all types of memory or I/O-mapping peripherals, such as Ethernet controllers, Universal Asynchronous Receiver/Transmitters (UART), modems, rotating disk memory, and so on. The ZX6017 can be used in a stand-alone configuration without the use of a local processor when all necessary data for Attribute Memory, Card Configuration Registers (CCR), Memory/I/O maps, and so on, are being provided by a local serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The ZX6017 can also be configured by a local microprocessor, when one is being used on the card.

Throughout this document, references to the ZX6017 device applies equally to the Z86017 and Z16017, unless otherwise specified.

Note: All Signals with an overline ($\overline{\ }$) are active Low, that is, B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

The ZX6017 can be programmed by one of two ways: an external 256 byte serial EEPROM can be connected to the serial port interface, or a microprocessor can be connected to this port to provide a higher level of control. Figure 1 depicts the functional block diagram for the ZX6017.

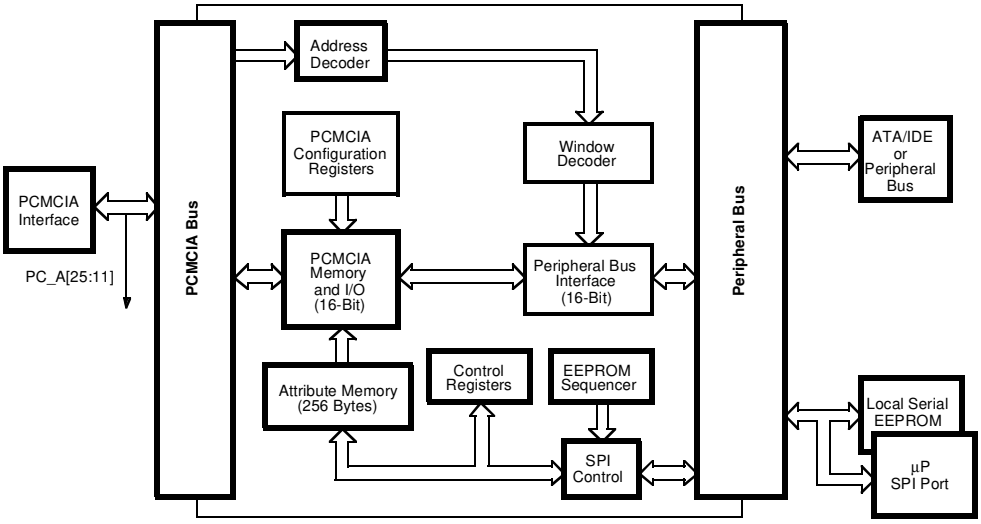

Figure 1. ZX6017 Functional Block Diagram

Power-On Reset

The ZX6017 defaults to the Memory Only interface as outlined in the PCMCIA specification upon deassertion of Power-On Reset (/$\overline{\text{POR}}$). The hardware sets Busy on the PC_RDY/$\overline{\text{BSY}}$ pin and then addresses the EE_MASTER pin. If the EE_MASTER pin is unconnected or pulled High, the ZX6017 serial interface defaults to the Master mode and an external EEPROM is required. If this pin is pulled Low, the SLAVE mode is selected and an external microprocessor is required to configure the ZX6017 through the serial interface pins.

Next, the hardware addresses the $\overline{\text{PC}}$_ATA//HOE pin. If the $\overline{\text{PC}}$_ATA/$\overline{\text{HOE}}$ pin is held Low for 40 clocks (PC_MCLK_IN) after POR deassertion, the ZX6017 is enabled for ATA/IDE to ATA/IDE PASSTHROUGH mode. The PASSTHROUGH mode is for systems that

use the physical PCMCIA 68-pin connector but do not support PCMCIA protocol. If this pin is held High ($\overline{PC}$_ATA/$\overline{HOE}$), the device is placed into the PCMCIA mode. The override bits in register 00H determine what mode(s) the user can support.

Serial Port Operation (Master) Mode

After the ZX6017 determines that an external EEPROM is present (see Figure 2), the Ready/Busy pin on the PCMCIA interface is set to Busy. The ZX6017 internal sequencer starts up and reads EEPROM address 1eh. If EEPROM address 1Eh is loaded with a 1Ch then the EEPROM's data is considered to be valid. After that, the internal sequencer resets its address counter back to zero. Data from EEPROM's addresses [00-2F] is read out and put into the on-board registers of the ZX6017. The EEPROM sequencer then reads EEPROM addresses 30h to FFh and each byte is moved into the ZX6017 on-board attribute memory addresses 00-CFh. After loading the registers and attribute memory, the sequencer completes by clearing the Ready/Busy pin on the PCMCIA interface indicating 1 "Ready." If EEPROM address 1Eh does not contain 1Ch, then the sequencer stops. The PCMCIA Ready/Busy pin stays in the Busy state, the on-board registers of the ZX6017 remain in their default state, and attribute memory data is unknown. The user can program the off-board EEPROM through the PCMCIA interface by means of three special registers and ignore Busy.

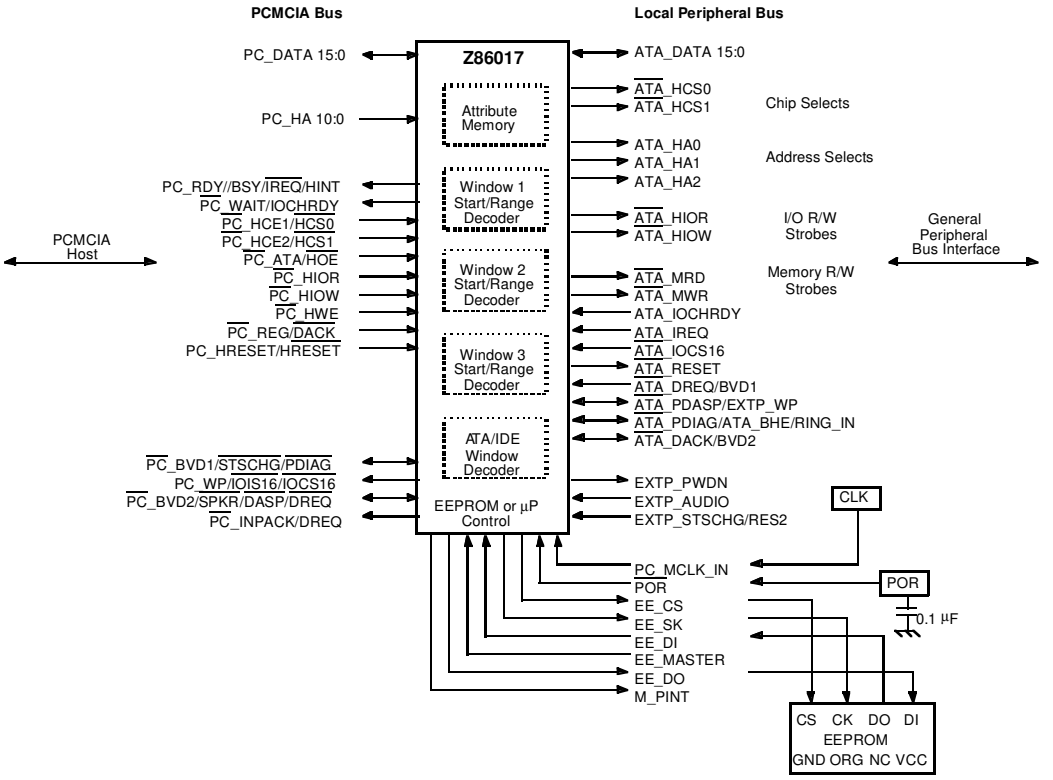

Figure 2. Serial Port Master Mode Control

Serial Port Operation (SLAVE) Mode

When the ZX6017 is placed in serial port SLAVE mode (EE_Master signal grounded on POR), the EEPROM sequencer is disabled and the user must provide external hardware (microprocessor) with serial interface to program CCRs and attribute memory. Additionally, if the

POR signal is deasserted, the user must provide a clock source on the PC_MCLK_IN pin in the range of 1-20MHz.

The external hardware can program the on-board registers and the attribute memory by selecting the ZX6017 and pulling the EE_CS pin High. The external hardware must set up the data to be sent to the ZX6017 on the EE_DI pin and strobe the EE_SK pin. The first byte of data is the address selected by the user, the second byte is the command byte and the third byte is the data. The external hardware must provide 24 clocks in order to read or write to a location in the ZX6017 (see Figure 26, Slave Interface Timing, in Appendix B).

To program the on-board attribute memory, the user must first write to it. Accomplish this programming by writing the address location of the attribute memory to be written (or read) in the attribute RAM data address register at location 08h. When this step has been accomplished, the user then writes (or reads) the attribute RAM data register 09h with the data to be read or written at that location.

Note: The attribute RAM address register auto-incriments after reading or writing to the attribute RAM data register.

Figure 3 demonstrates programming the ZX6017 in SLAVE Mode. The external user's hardware writes to register 00 and selects the clock divide by and the override mode (if needed). The READY/$\overline{\text{BUSY}}$ pin remains set to 0 to indicate BUSY, and a local µP interrupt polarity is selected.

The user programs registers 01-05, followed by registers 0Ah-2Fh. The user writes to the attribute memory by setting the address in the address register 08h and in the loop on data register 09h with the user's attribute memory data. The user completes the operation by writing back to register 00 to clear the READY/$\overline{\text{READY}}$ status.

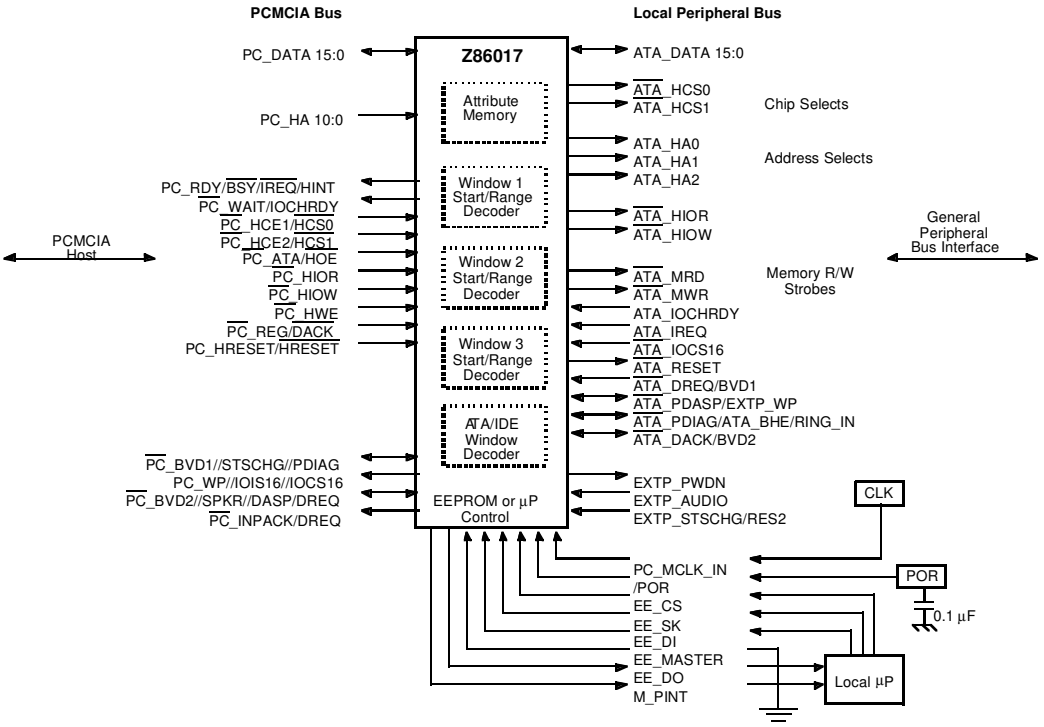

Figure 3. Serial Port Slave Mode Control

EEPROM Programming Through the PCMCIA Interface

The ZX6017 can program the serial EEPROM through the PCMCIA interface. EEPROM programming is accomplished by means of three special registers that are accessed identically to the CCR registers as defined by the PCMCIA specification (Figure 4). These registers are fixed at addresses 7F0, 7F2, and 7F4. The host software reads and writes each byte of the EEPROM through these registers and configures the

ZX6017 device. After the host writes new values to the EEPROM through these registers, the new values are loaded into the ZX6017 at Power-On Reset ($\overline{POR}$).

Note: The values written register 05h offset the CCR registers and the three special EEPROM programming registers on the next POR.

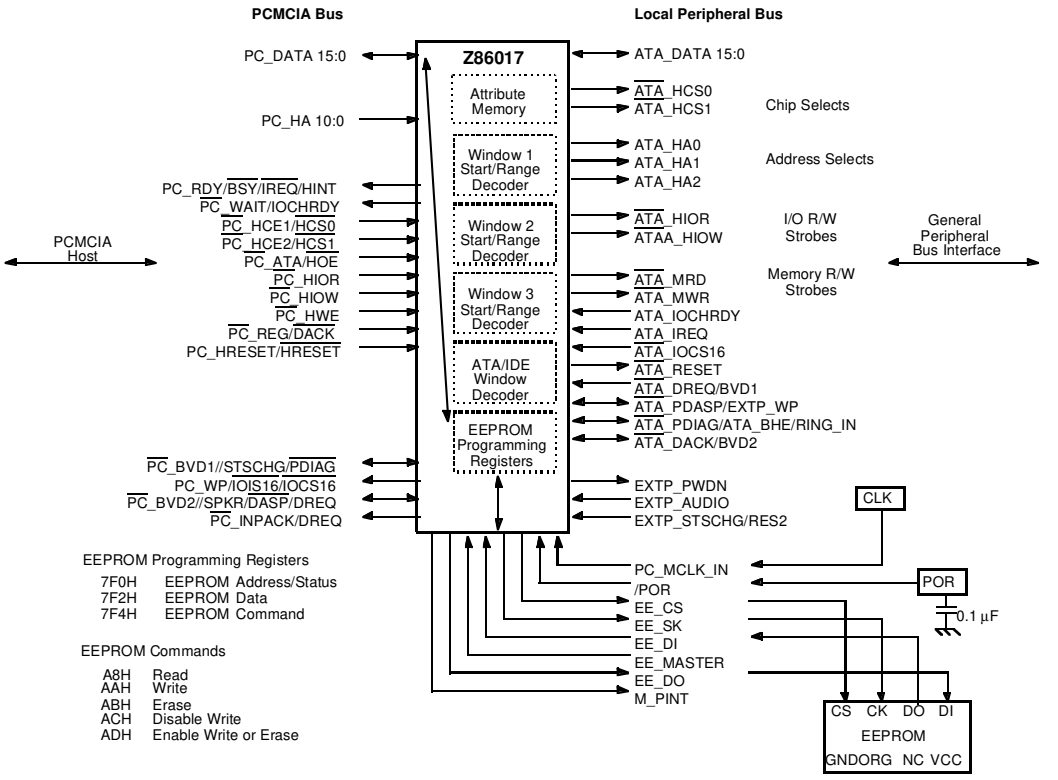

Figure 4. EEPROM Programming Through the PCMCIA Interface

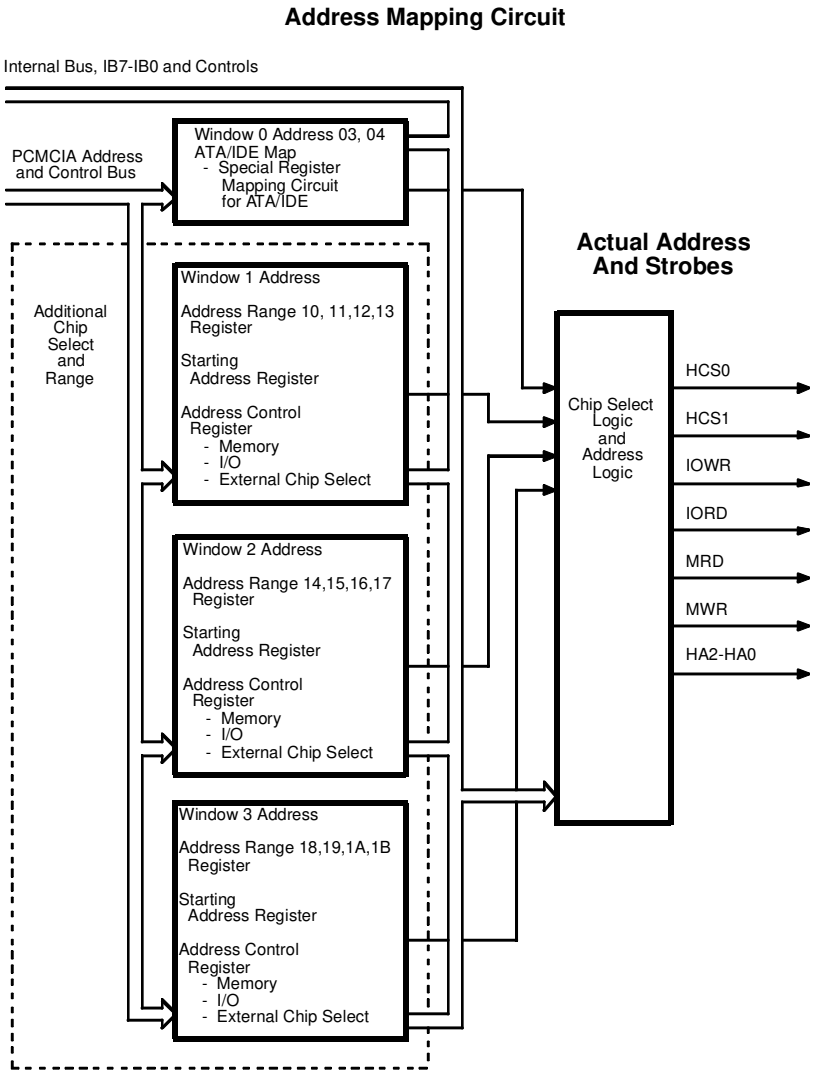

Figure 5. Connection Block Diagram

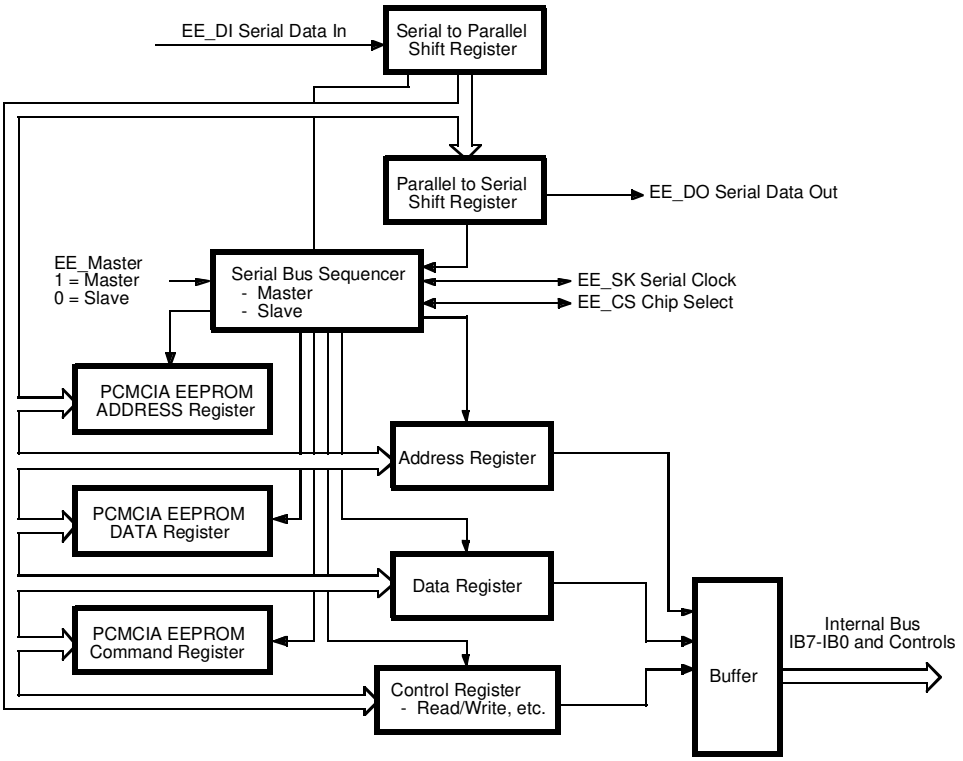

Figure 6. Serial Interface Diagram

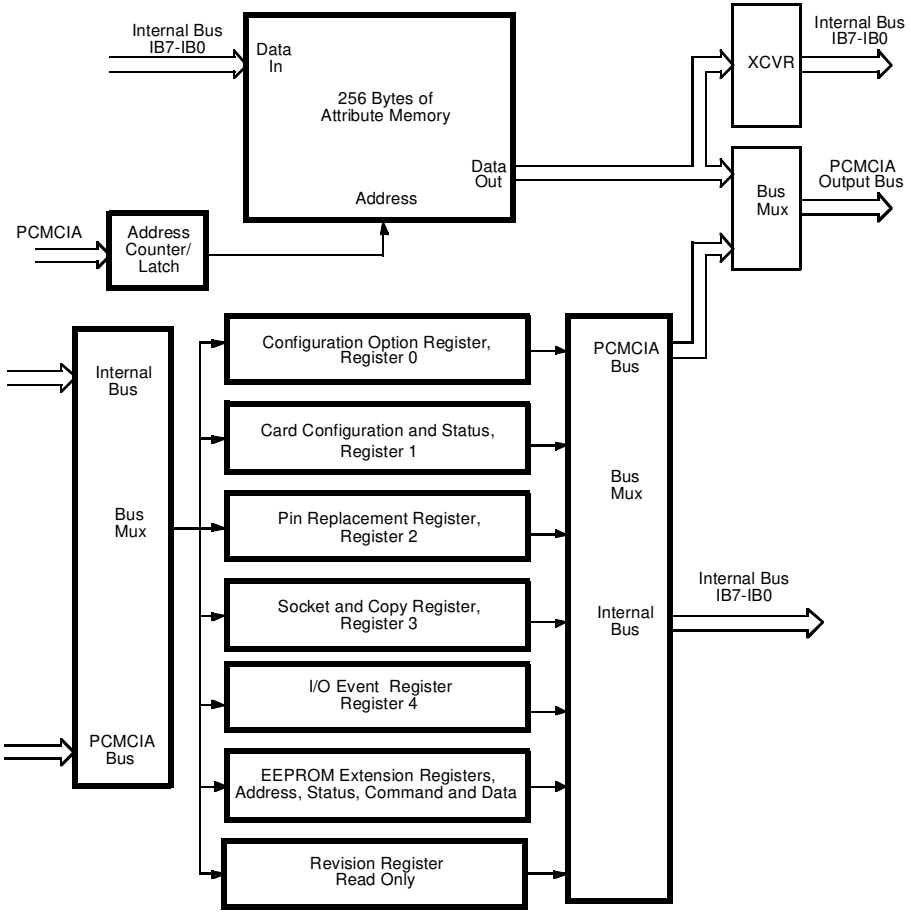

Figure 7. Attribute and Configuration Memory Diagram

PIN DESCRIPTION

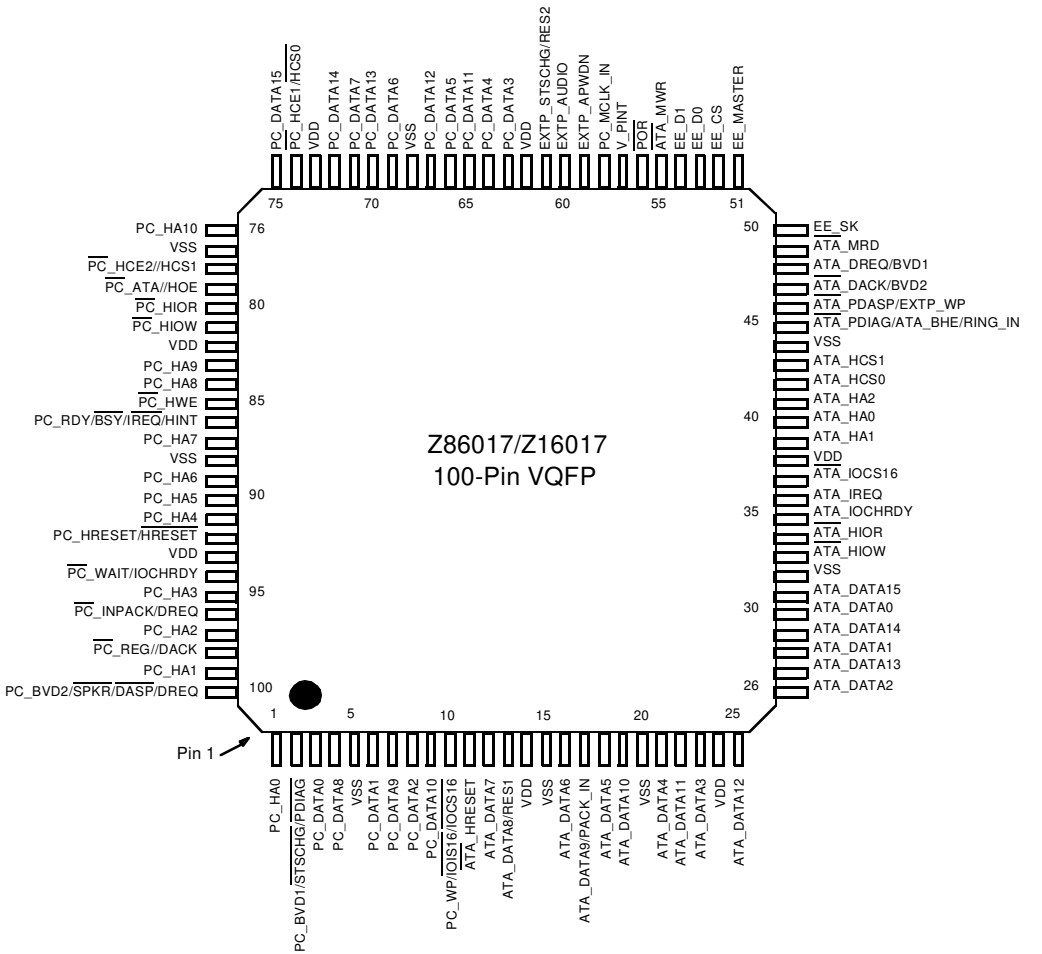

Figure 8. ZX6017 100-Pin VQFP Pin Configuration

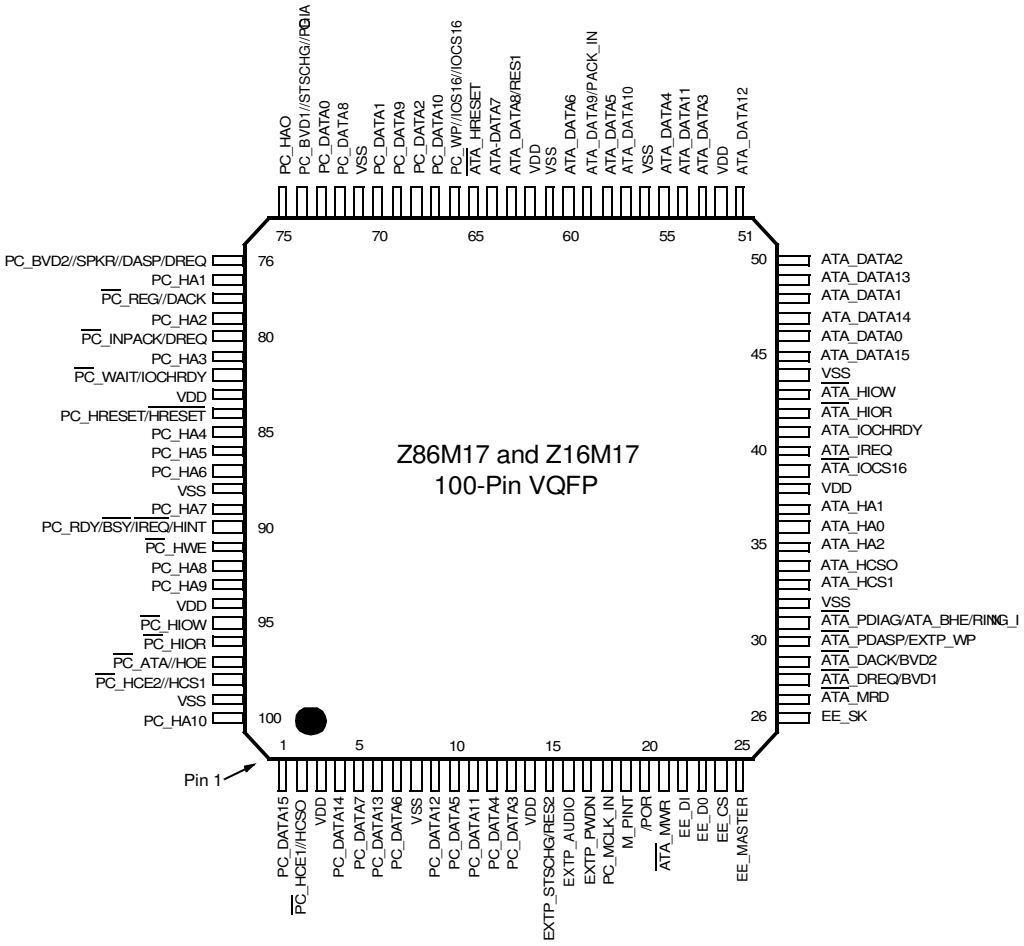

Figure 9. Z86M17 and Z16M17 (Mirror Image) 100-Pin VQFP Pin Configuration