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Z16C30

CMOS USC Universal Serial Controller

Product Specification

DS007902-0708

PRELIMINARY

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
July 2008	02	Updated as per latest template and style guide.	All
Jan 2000	01	Original issue	

Table of Contents

Architectural Overview

Features

The key features of Zilog's Z16C30 device include:

- Two Independent 0-to-10 Mbps Full-Duplex Channels, each with Two Baud Rate Generators and One digital phase-locked loop (DPLL) for Clock Recovery
- 32-byte Data FIFO's for each Receiver and Transmitter
- 110 ns Bus Cycle Time, 16-bit Data Bus Bandwidth
- Multi-Protocol Operation under Program Control with Independent Mode Selection for Receiver and Transmitter
- Async Mode with 1 to 8 Bits/Character, 1/16 to 2 Stop Bits/Character in 1/16-bit Increments, Programmable Clock Factor, Break Detect and Generation, Odd, Even, Mark, Space or no Parity and Framing Error Detection, Supports One Address/Data Bit and MIL STD 1553B Protocols
- Byte Oriented Synchronous Mode with One to Eight Bits/Character, Programmable Idle Line Condition, Optional Receive Sync Stripping; Optional Preamble Transmission, 16- or 32-bit CRC, and Transmit-to-Receive Slaving (for X.21)
- Bisync Mode with 2- to 16-bit Programmable Sync Character, Programmable Idle Line Condition, Optional Receive Sync Stripping, Optional Preamble Transmission, 16- or 32-bit CRC
- Transparent Bisync Mode with EBCDIC or ASCII Character Code, Automatic CRC Handling, Programmable Idle Line Condition, Optional Preamble Transmission, Automatic Recognition of DLE, SYN, SOH, ITX, ETX, ETB, EOT, ENQ, and ITB
- External Character Sync Mode for Receive
- HDLC/SDLC Mode with Eight-Bit Address Compare, Extended Address Field Option, 16- or 32-bit CRC, Programmable Idle Line Condition, Optional Preamble Transmission and Loop Mode
- DMA Interface with Separate Request and Acknowledge for Each Receiver and Transmitter
- Channel Load Command for DMA Controlled Initialization
- Flexible Bus Interface for Direct Connection to Most Microprocessors, User Programmable for 8 or 16 Bits Wide, Directly Supports 680X0 Family or 8X86 Family Bus Interfaces
- Low Power CMOS
- 68-Pin PLCC/100-Pin VQFP Packages

General Description

Zilog's Z16C30 USC Universal Serial Controller is a dual-channel multi-protocol data communications peripheral designed for use with any conventional multiplexed or non-multiplexed bus. The USC functions as a serial-to-parallel, parallel-to-serial converter/controller and may be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including two baud rate generators per channel, one digital phase-locked loop (DPLL) per channel, character counters for both receive and transmit in each channel and 32-byte data FIFO's for each receiver and transmitter (Figure 1 on page 3).

Zilog now offers a high speed version of the USC with improved bus bandwidth. CPU bus accesses have been shortened from 160 ns per access to 110 ns per access. The USC has a transmit and receive clock range of up to 10 MHz (20 MHz when using the DPLL, BRG, or CTR) and data transfer rates as high as 10 Mbits/sec full duplex.

The USC handles asynchronous formats, synchronous byte-oriented formats such as BISYNC, and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The device can generate and check CRC in any synchronous mode and can be programmed to check data integrity in various modes. The USC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O (GPIO). The same is true for most of the other pins in each channel.

Interrupts are supported with a daisy-chain hierarchy, with the two channels having completely separate interrupt structures.

High-speed data transfers through DMA are supported by a Request/Acknowledge signal pair for each receiver and transmitter. The device supports automatic status transfer through DMA and also allows device initialization under DMA control.

Note: *When written to, all reserved bits must be programmed to 0.*

To aid in efficiently programming the USC, support tools are available. The Technical Manual describes in detail all features presented in this Product Specification and gives programming sequence hints. The Programmer's Assistant is a MS-DOS disk-based programming initialization tool to be used in conjunction with the Technical Manual. There are also available assorted application notes and development boards to assist in the hardware/software development.

All Signals with an overline, are active Low. For example: B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow these conventional descriptions:

Table 1. Power connection conventions

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

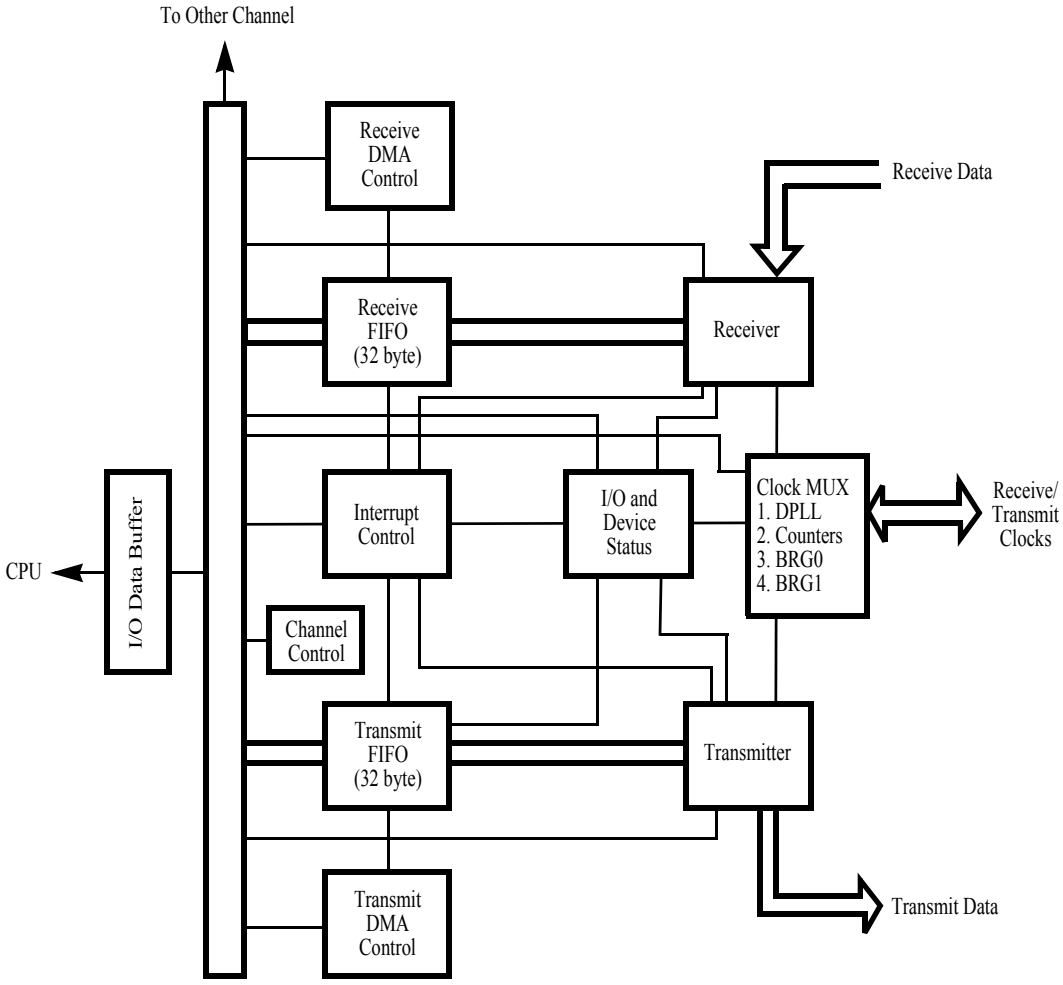


Figure 1. Z16C30 Block Diagram

Pin Description

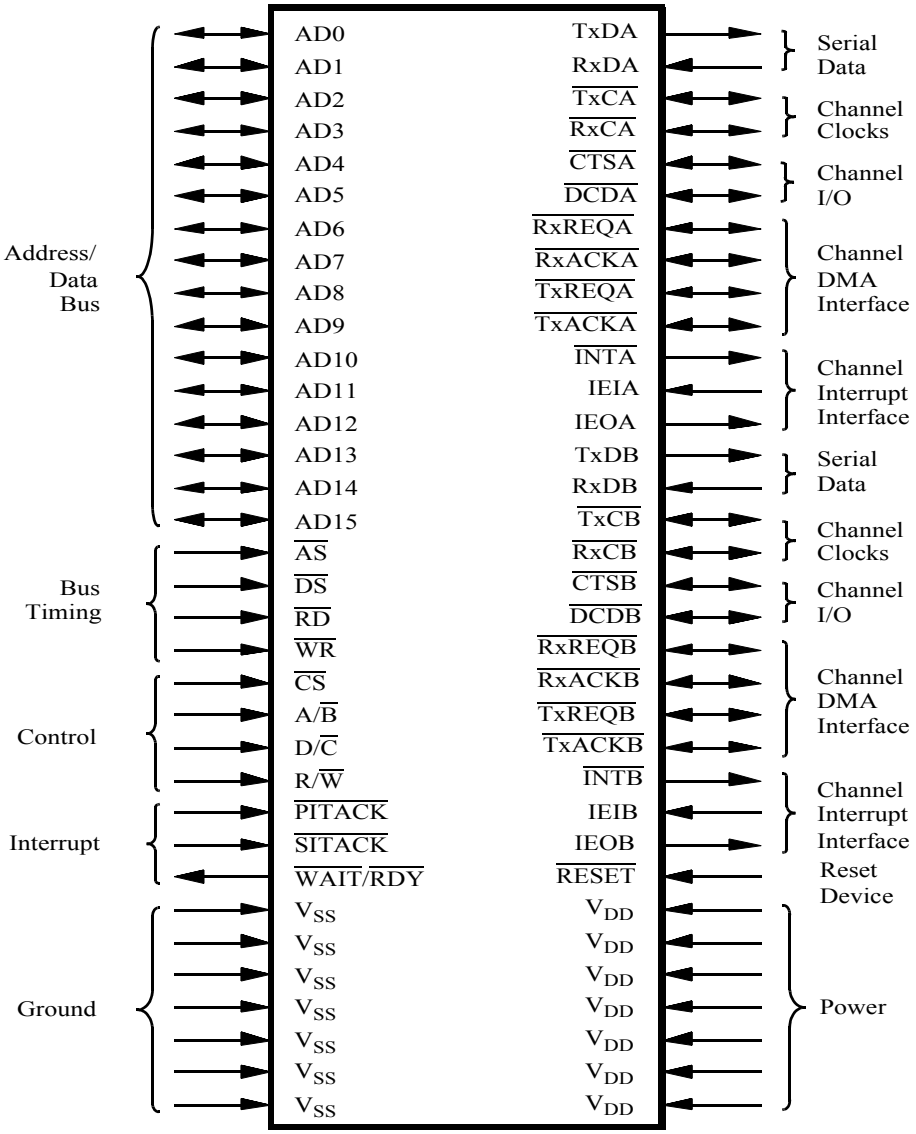


Figure 2. Z16C30 Pin Functions

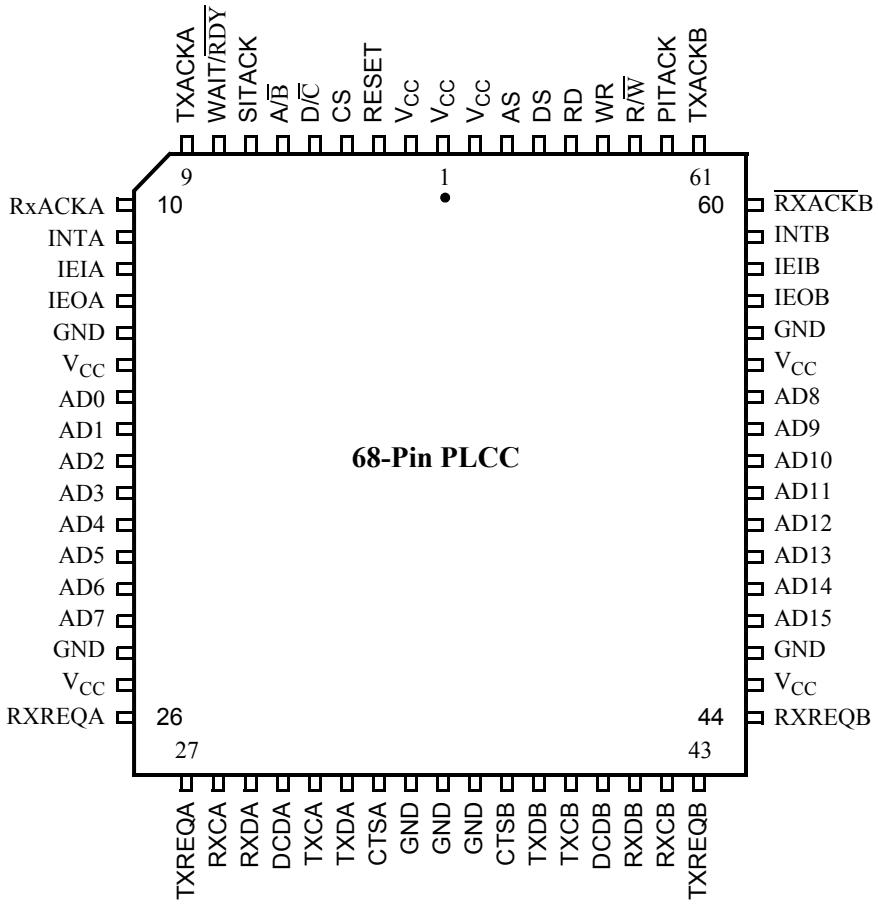


Figure 3. Z16C30 68-Pin PLCC Pin Assignments

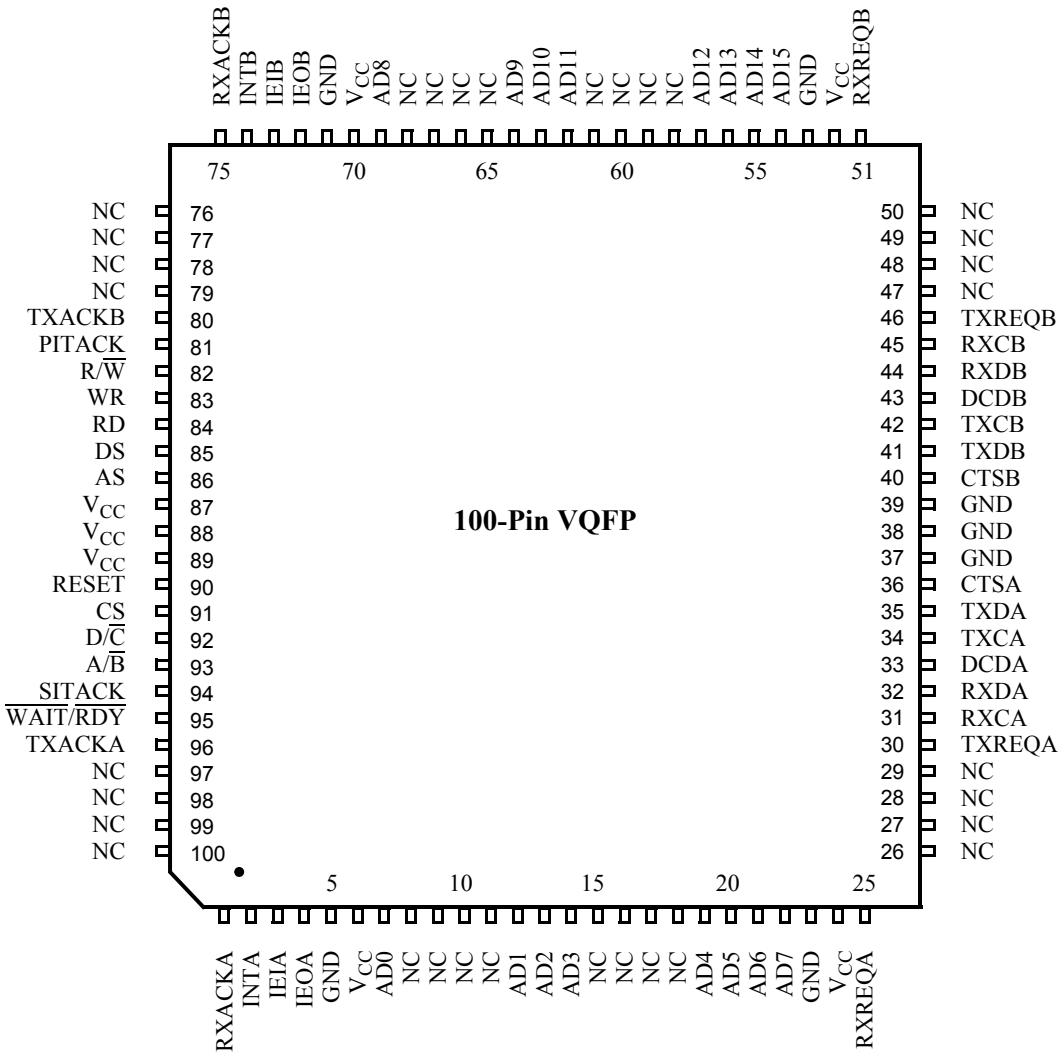


Figure 4. 100-Pin VQFP Pin Assignments

The Z16C30 contains 13 pins per channel for channel I/O, 16 pins for address and data, 12 pins for CPU handshake, and 14 pins for power and ground.

Three separate bus interface types are available for the device. The Bus Configuration Register (BCR) and external connections to the AD bus control selection of the bus type. A 16-bit bus is selected by setting BCR bit 2 to a 1. The 8-bit bus is selected by setting BCR bit 2 to 0 and tying AD15–AD8 to V_{SS}.

The 8-bit bus with separate address is selected by setting BCR bit 2 to 0 and, during the BCR write, forcing AD15 to a 1 and forcing AD14–AD8 to 0.

The multiplexed bus is selected for the USC if there is an Address Strobe prior to or during the transaction which writes the BCR. If no Address Strobe is present prior to or during the transaction which writes the BCR, a nonmultiplexed bus is selected (see Figure 29 on page 49).

Pin Functions

$\overline{\text{RESET}}$ Reset (input, active Low)—This signal resets the device to a known state. The first write to the USC after a reset accesses the BCR to select additional bus options for the device.

$\overline{\text{AS}}$ Address Strobe (input, active Low)—This signal is used in the multiplexed bus modes to latch the address on the AD lines. The $\overline{\text{AS}}$ signal is not used in the nonmultiplexed bus modes and should be tied to V_{DD}.

$\overline{\text{DS}}$ Data Strobe (input, active Low)—This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle. $\overline{\text{DS}}$ also strobes data into the device on the state of R/$\overline{\text{W}}$.

$\overline{\text{RD}}$ Read Strobe (input, active Low)—This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle.

$\overline{\text{WR}}$ Write Strobe (input, active Low)—This signal strobes data into the device during a write.

R/$\overline{\text{W}}$ Read/Write (input)—This signal determines the direction of data transfer for a read or write cycle in conjunction with $\overline{\text{DS}}$.

$\overline{\text{CS}}$ Chip Select (input, active Low)—This signal selects the device for access and must be asserted for read and write cycles, but is ignored during interrupt acknowledge and fly-by DMA transfers. In the case of a multiplexed bus interface, $\overline{\text{CS}}$ is latched by the rising edge of $\overline{\text{AS}}$.

A/$\overline{\text{B}}$ Channel A/Channel B Select (input)—This signal selects between the two channels in the device. High selects channel A and Low selects channel B. This signal is sampled and the result is latched during the BCR (Bus Configuration Register) write. It programs the sense of the $\overline{\text{WAIT}}$/$\overline{\text{RDY}}$ signal appropriate for different bus interfaces.

D/$\overline{\text{C}}$ Data/Control Select (input)—This signal, when High, provides for direct access to the RDR and TDR. In the case of a multiplexed bus interface, D/$\overline{\text{C}}$ High overrides the address provided to the device.

$\overline{\text{SITACK}}$ Status Interrupt Acknowledge (input, active Low)—This signal is a status signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle. This signal is compatible with 680X0 family microprocessors.

$\overline{\text{PITACK}}$ Pulsed Interrupt Acknowledge (input, active Low)—This signal is a strobe signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle. $\overline{\text{PITACK}}$ may be programmed to accept a single pulse or double pulse acknowledge type. This programming is done in the BCR. With the double pulse type selected, the first $\overline{\text{PITACK}}$ is recognized but no action takes place. The interrupt vector is returned on the second pulse if the no vector option is not selected. The double pulse type is compatible with 8X86 family microprocessors.

$\overline{\text{WAIT}}$/$\overline{\text{RDY}}$ Wait/Data Ready (output, active Low)—This signal serves to indicate when the data is available during a read cycle, when the device is ready to receive data during a write cycle, and when a valid vector is available during an interrupt acknowledge cycle. It may be programmed to function either as a Wait signal or a Ready signal using the state of the A/$\overline{\text{B}}$ pin during the BCR write. When A/$\overline{\text{B}}$ is High during the BCR write, this signal functions as a wait output and thus supports the READY function of 8X86 family microprocessors. When A/$\overline{\text{B}}$ is Low during the BCR write, this signal functions as a ready output and thus supports the DTACK function of 680X0 family microprocessors.

AD15–AD0 Address/Data Bus (bidirectional, active High, tri-state)—The AD signals carry addresses to, and data to and from, the device. When the 16-bit nonmultiplexed bus is selected, AD15–AD0 carry data to and from the device. Addresses are provided using a pointer within the device that is loaded with the desired register address. When selecting the 8-bit nonmultiplexed bus (without separate address) only AD7–AD0 are used to transfer data. The pointer is used for addressing, with AD15–AD8 unused. When selecting the 8-bit nonmultiplexed bus (with separate address), AD7–AD0 are used to transfer data with AD15–AD8 used as address bus. When the 16-bit multiplexed bus is selected, addresses are latched from AD7–AD0 and data transfers are sixteen bits wide. When selecting the 8-bit multiplexed bus (without separate address) only AD7–AD0 are used to transfer addresses and data, with AD15–AD8 unused. When the 8-bit multiplexed bus with separate address is selected, only AD7–AD0 are used to transfer data, while AD15–AD8 are used as an address bus.

$\overline{\text{INTA}}$, $\overline{\text{INTB}}$ Interrupt Request (outputs, active Low)—These signals indicate that the channel has an interrupt condition pending and is requesting service. These outputs are NOT open-drain.

IEIA, IEIB Interrupt Enable In (inputs, active High)—The IEI signal for each channel is used with the accompanying IEO signal to form an interrupt daisy chain. An active IEI indicates that no device having higher priority is requesting or servicing an interrupt.

IEOA, IEOB Interrupt Enable Out (outputs, active High)—The IEO signal for each channel is used with the accompanying IEI signal to form an interrupt daisy chain. IEO is Low if IEI is Low, an interrupt is under service in the channel, or an interrupt is pending during an interrupt acknowledge cycle.

$\overline{\text{TxACKA}}$, $\overline{\text{TxACKB}}$ Transmit Acknowledge (inputs or outputs, active Low)—The primary function of these signals is to perform fly-by DMA transfers to the transmit FIFOs. They may also be used as bit inputs or outputs.

$\overline{\text{RxACKA}}$, $\overline{\text{RxACKB}}$ Receive Acknowledge (inputs or outputs, active Low)—The primary function of these signals is to perform fly-by DMA transfers from the receive FIFOs. They may also be used as bit inputs or outputs.

TxDA, TxDB Transmit Data (outputs, active High, tri-state)—These signals carry the serial transmit data for each channel.

RxDA, RxDB Receive Data (inputs, active High)—These signals carry the serial receive data for each channel.

$\overline{\text{TxCA}}$, $\overline{\text{TxCB}}$ Transmit Clock (inputs or outputs, active Low)—These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various transmitter signals or internal clock signals.

$\overline{\text{RxCA}}$, $\overline{\text{RxCB}}$ Receive Clock (inputs or outputs, active Low)—These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various receiver signals or internal clock signals.

$\overline{\text{TxREQA}}$, $\overline{\text{TxREQB}}$ Transmit Request (inputs or outputs, active Low)—The primary function of these signals is to request DMA transfers to the transmit FIFOs. They may also be used as simple inputs or outputs.

$\overline{\text{RxREQA}}$, $\overline{\text{RxREQB}}$ Receive Request (inputs or outputs, active Low)—The primary function of these signals is to request DMA transfers from the receive FIFOs. They may also be used as simple inputs or outputs.

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$ Clear To Send (inputs or outputs, active Low)—These signals are used as enables for the respective transmitters. They may also be programmed to generate interrupts on either transition or used as simple inputs or outputs.

$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$ Data Carrier Detect (inputs or outputs, active Low)—These signals are used as enables for the respective receivers. They may also be programmed to generate interrupts on either transition or used as simple inputs or outputs.

Electrical Characteristics

Table 2. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

*Voltage on all pins with respect to GND.
†See Ordering Information on page 97.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The DC Characteristics and Capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5 on page 11). Standard conditions are as follows:

- +4.5 V < V_{CC} < +5.5 V
- GND = 0 V
- T_A as specified in Ordering Information on page 97

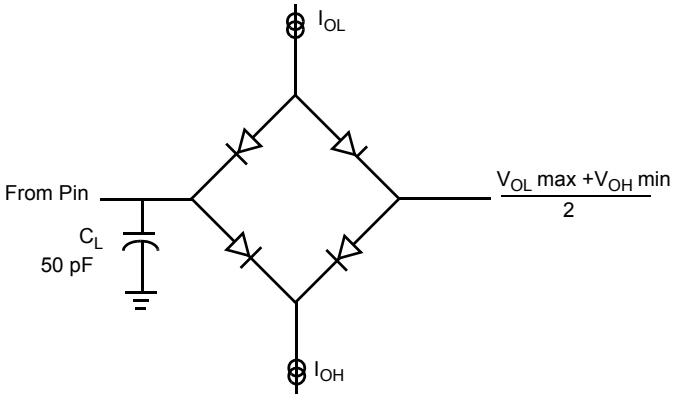


Figure 5. Test Load Diagram

Capacitance

Table 3. Capacitance

Symbol	Parameter	Min	Max	Unit	Condition
C_{IN}	Input Capacitance		10	pF	Unmeasured Pins
C_{OUT}	Output Capacitance		15	pF	Returned to Ground.
CI/O	Bidirectional Capacitance		20	pF	
Note: f = 1 MHz over specified temperature range.					

Miscellaneous

Transistor Count: 174,000

Temperature Ratings

Standard = 0 °C to ±70 °C
Extended = –40 °C to +85 °C

DC Characteristics

Table 4. Z16C30 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	–0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	Output High Voltage	V_{CC}–0.8			V	I_{OH} = –250 µA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = +2.0 mA
I_{IL}	Input Leakage			±10.00	µA	0.4 < V_{IN} < +2.4 V
I_{OL}	Output Leakage			±10.00	µA	0.4 < V_{OUT} < +2.4 V
I_{CCI}	V_{CC} Supply Current		7	50	mA	V_{CC} = 5 V V_{IH} = 4.8 V V_{IL} = 0.2V
Note: V_{CC}= 5 V ±10% unless otherwise specified, over specified temperature range.						

AC Characteristics

Table 5. Z16C30 AC Characteristics

No	Symbol	Parameter	Min	Max	Units	Note
1	Tcyc	Bus Cycle Time	110		ns	
2	TwASl	$\overline{AS}$ Low Width	30		ns	
3	TwASh	$\overline{AS}$ High Width	60		ns	
4	TwDSl	$\overline{DS}$ Low Width	60		ns	
5	TwDSh	$\overline{DS}$ High Width	50		ns	
6	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay Time	5		ns	
7	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay Time	5		ns	
8	TdDS(DRa)	$\overline{DS}$ Fall to Data Active Delay	0		ns	
9	TdDS(DRv)	$\overline{DS}$ Fall to Data Valid Delay		60	ns	
10	TdDS(DRn)	$\overline{DS}$ Rise to Data Not Valid Delay	0		ns	
11	TdDS(DRz)	$\overline{DS}$ Rise to Data Float Delay		20	ns	

Table 5. Z16C30 AC Characteristics (Continued)

No	Symbol	Parameter	Min	Max	Units	Note
12	TsCS(AS)	$\overline{CS}$ to $\overline{AS}$ Rise Setup Time	15		ns	
13	ThCS(AS)	$\overline{CS}$ to $\overline{AS}$ Rise Hold Time	5		ns	
14	TsADD(AS)	Direct Address to $\overline{AS}$ Rise Setup Time	15		ns	1
15	ThADD(AS)	Direct Address to $\overline{AS}$ Rise Hold Time	5		ns	1
16	TsSIA(AS)	$\overline{SITACK}$ to $\overline{AS}$ Rise Setup Time	15		ns	
17	ThSIA(AS)	$\overline{SITACK}$ to $\overline{AS}$ Rise Hold Time	5		ns	
18	TsAD(AS)	Address to $\overline{AS}$ Rise Setup Time	15		ns	
19	ThAD(AS)	Address to $\overline{AS}$ Rise Hold Time	5		ns	
20	TsRW(DS)	R/$\overline{W}$ to $\overline{DS}$ Fall Setup Time	0		ns	
21	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ Fall Hold Time	25		ns	
22	TsDSf(RRQ)	$\overline{DS}$ Fall to $\overline{RxREQ}$ Inactive Delay		60	ns	4
23	TdDSr(RRQ)	$\overline{DS}$ Rise to $\overline{RxREQ}$ Active Delay	0		ns	
24	TsDW(DS)	Write Data to $\overline{DS}$ Rise Setup Time	30		ns	
25	ThDW(DS)	Write Data to $\overline{DS}$ Rise Hold Time	0		ns	
26	TdDSf(TRQ)	$\overline{DS}$ Fall to $\overline{TxREQ}$ Inactive Delay		65	ns	5,6
27	TdDSr(TRQ)	$\overline{DS}$ Rise to $\overline{TxREQ}$ Active Delay	0		ns	
28	TwRDl	$\overline{RD}$ Low Width	60		ns	
29	TwRDh	$\overline{RD}$ High Width	50		ns	
30	TdAS(RD)	$\overline{AS}$ Rise to $\overline{RD}$ Fall Delay Time	5		ns	
31	TdRD(AS)	$\overline{RD}$ Rise to $\overline{AS}$ Fall Delay Time	5		ns	
32	TdRD(DRa)	$\overline{RD}$ Fall to Data Active Delay	0		ns	
33	TdRD(DRv)	$\overline{RD}$ Fall to Data Valid Delay		60	ns	
34	TdRD(DRn)	$\overline{RD}$ Rise to Data Not Valid Delay	0		ns	

Table 5. Z16C30 AC Characteristics (Continued)

No	Symbol	Parameter	Min	Max	Units	Note
35	TdRD(DRz)	$\overline{RD}$ Rise to Data Float Delay		20	ns	
36	TdRDf(RRQ)	$\overline{RD}$ Fall to $\overline{RxREQ}$ Inactive Delay		60	ns	4
37	TdRDr(RRQ)	$\overline{RD}$ Rise to $\overline{RxREQ}$ Active Delay	0		ns	
38	TwWRl	$\overline{WR}$ Low Width	60		ns	
39	TwWRh	$\overline{WR}$ High Width	50		ns	
40	TdAS(WR)	$\overline{AS}$ Rise to $\overline{WR}$ Fall Delay Time	5		ns	
41	TdWR(AS)	$\overline{WR}$ Rise to $\overline{AS}$ Fall Delay Time	5		ns	
42	TsDW(WR)	Write Data to $\overline{WR}$ Rise Setup Time	30		ns	
43	ThDW(WR)	Write Data to $\overline{WR}$ Rise Hold Time	0		ns	
44	TdWRf(TRQ)	$\overline{WR}$ Fall to $\overline{TxREQ}$ Inactive Delay		65	ns	5
45	TdWRr(TRQ)	$\overline{WR}$ Rise to $\overline{TxREQ}$ Active Delay	0		ns	
46	TsCS(DS)	$\overline{CS}$ to $\overline{DS}$ Fall Setup Time	0		ns	2
47	ThCS(DS)	$\overline{CS}$ to $\overline{DS}$ Fall Hold Time	25		ns	2
48	TsADD(DS)	Direct Address to $\overline{DS}$ Fall Setup Time	5		ns	1,2
49	ThADD(DS)	Direct Address to $\overline{DS}$ Fall Hold Time	25		ns	1,2
50	TsSIA(DS)	$\overline{SITACK}$ to $\overline{DS}$ Fall Setup Time	5		ns	2
51	ThSIA(DS)	$\overline{SITACK}$ to $\overline{DS}$ Fall Hold Time	25		ns	2
52	TsCS(RD)	$\overline{CS}$ to $\overline{RD}$ Fall Setup Time	0		ns	2
53	ThCS(RD)	$\overline{CS}$ to $\overline{RD}$ Fall Hold Time	25		ns	2
54	TsADD(RD)	Direct Address to $\overline{RD}$ Fall Setup Time	5		ns	1,2
55	ThADD(RD)	Direct Address to $\overline{RD}$ Fall Hold Time	25		ns	1,2
56	TsSIA(RD)	$\overline{SITACK}$ to $\overline{RD}$ Fall Setup Time	5		ns	2
57	ThSIA(RD)	$\overline{SITACK}$ to $\overline{RD}$ Fall Hold Time	25		ns	2
58	TsCS(WR)	$\overline{CS}$ to $\overline{WR}$ Fall Setup Time	0		ns	2

Table 5. Z16C30 AC Characteristics (Continued)

No	Symbol	Parameter	Min	Max	Units	Note
59	ThCS(WR)	$\overline{CS}$ to $\overline{WR}$ Fall Hold Time	25		ns	2
60	TsADD(WR)	Direct Address to $\overline{WR}$ Fall Setup Time	5		ns	1,2
61	ThADD(WR)	Direct Address to $\overline{WR}$ Fall Hold Time	25		ns	1,2
62	TsSIA(WR)	$\overline{SITACK}$ to $\overline{WR}$ Fall Setup Time	5		ns	2
63	ThSIA(WR)	$\overline{SITACK}$ to $\overline{WR}$ Fall Hold Time	25		ns	2
64	TwRAKl	$\overline{RxACK}$ Low Width	60		ns	
65	TwRAKh	$\overline{RxACK}$ High Width	50		ns	
66	TdRAK(DRa)	$\overline{RxACK}$ Fall to Data Active Delay	0		ns	
67	TdRAK(DRv)	$\overline{RxACK}$ Fall to Data Valid Delay		60	ns	
68	TdRAK(DRn)	$\overline{RxACK}$ Rise to Data Not Valid Delay	0		ns	
69	TdRAK(DRz)	$\overline{RxACK}$ Rise to Data Float Delay		20	ns	
70	TdRAKf(RRQ)	$\overline{RxACK}$ Fall to $\overline{RxREQ}$ Inactive Delay		60	ns	4
71	TdRAKr(RRQ)	$\overline{RxACK}$ Rise to $\overline{RxREQ}$ Active Delay	0		ns	
72	TwTAKl	$\overline{TxACK}$ Low Width	60		ns	
73	TwTAKh	$\overline{TxACK}$ High Width	50		ns	
74	TsDW(TAK)	Write Data to $\overline{TxACK}$ Rise Setup Time	30		ns	
75	ThDW(TAK)	Write Data to $\overline{TxACK}$ Rise Hold Time	0		ns	
76	TdTAKf(TRQ)	$\overline{TxACK}$ Fall to $\overline{TxREQ}$ Inactive Delay		65	ns	5
77	TdTAKr(TRQ)	$\overline{TxACK}$ Rise to $\overline{TxREQ}$ Active Delay	0		ns	
78	TdDSf(RDY)	$\overline{DS}$ Fall (INTACK) to $\overline{RDY}$ Fall Delay		200	ns	
79	TdRDY(DRv)	$\overline{RDY}$ Fall to Data Valid Delay		40	ns	
80	TdDSr(RDY)	$\overline{DS}$ Rise to $\overline{RDY}$ Rise Delay		40	ns	

Table 5. Z16C30 AC Characteristics (Continued)

No	Symbol	Parameter	Min	Max	Units	Note
81	TsIEI(DSI)	IEI to $\overline{DS}$ Fall (INTACK) Setup Time	10		ns	
82	ThIEI(DSI)	IEI to $\overline{DS}$ Rise (INTACK) Hold Time	0		ns	
83	TdIEI(IEO)	IEI to IEO Delay		30	ns	
84	TdAS(IEO)	$\overline{AS}$ Rise (Intack) to IEO Delay		60	ns	
85	TdDSI(INT)	$\overline{DS}$ Fall (INTACK) to $\overline{INT}$ Inactive Delay		200	ns	7
87	TdDSI(Wr)	$\overline{DS}$ Fall (INTACK) to $\overline{WAIT}$ Rise Delay		200	ns	
88	TdW(DRv)	$\overline{WAIT}$ Rise to Data Valid Delay		40	ns	
89	TdRDf(RDY)	$\overline{RD}$ Fall (INTACK) to $\overline{RDY}$ Fall Delay		200	ns	
90	TdRDr(RDY)	$\overline{RD}$ Rise to $\overline{RDY}$ Rise Delay		40	ns	
91	TsIEI(RDI)	IEI to $\overline{RD}$ Fall (INTACK) Setup Time	10		ns	
92	ThIEI(RDI)	IEI to $\overline{RD}$ Rise (INTACK) Hold Time	0		ns	
93	TdRDI(INT)	$\overline{RD}$ Fall (INTACK) to $\overline{INT}$ Inactive Delay		200	ns	
94	TdRDI(Wf)	$\overline{RD}$ Fall (INTACK) to $\overline{WAIT}$ Fall Delay		40	ns	
95	TdRDI(Wr)	$\overline{RD}$ Fall (INTACK) to $\overline{WAIT}$ Rise Delay		200	ns	
96	TwPIAl	$\overline{PITACK}$ Low Width	60		ns	
97	TwPIAh	$\overline{PITACK}$ High Width	50		ns	
98	TdAS(PIA)	$\overline{AS}$ Rise to $\overline{PITACK}$ Fall Delay Time	5		ns	
99	TdPIA(AS)	$\overline{PITACK}$ Rise to $\overline{AS}$ Fall Delay Time	5		ns	
100	TdPIA(DRa)	$\overline{PITACK}$ Fall to Data Active Delay	0		ns	
101	TdPIA(DRn)	$\overline{PITACK}$ Rise to Data Not Valid Delay	0		ns	
102	TdPIA(DRz)	$\overline{PITACK}$ Rise to Data Float Delay		20	ns	

Table 5. Z16C30 AC Characteristics (Continued)

No	Symbol	Parameter	Min	Max	Units	Note
103	TsIEI(PIA)	IEI to $\overline{\text{PITACK}}$ Fall Setup Time	10		ns	
104	ThIEI(PIA)	IEI to $\overline{\text{PITACK}}$ Rise Hold Time	0		ns	
105	TdPIA(IEO)	$\overline{\text{PITACK}}$ Fall to IEO Delay		60	ns	
106	TdPIA(INT)	$\overline{\text{PITACK}}$ Fall to $\overline{\text{INT}}$ Inactive Delay		200	ns	
107	TdPIAf(RDY)	$\overline{\text{PITACK}}$ Fall to $\overline{\text{RDY}}$ Fall Delay		200	ns	
108	TdPIAr(RDY)	$\overline{\text{PITACK}}$ Rise to $\overline{\text{RDY}}$ Rise Delay		40	ns	
109	TdPIA(Wf)	$\overline{\text{PITACK}}$ Fall to $\overline{\text{WAIT}}$ Fall Delay		40	ns	
110	TdPIA(Wr)	$\overline{\text{PITACK}}$ Fall to $\overline{\text{WAIT}}$ Rise Delay		200	ns	
111	TdSIA(INT)	$\overline{\text{SITACK}}$ Fall to IEO Inactive Delay		200	ns	2
112	TwSTBh	$\overline{\text{Strobe}}$ High Width	50		ns	3
113	TwRESl	$\overline{\text{RESET}}$ Low Width	170		ns	
114	TwRESh	$\overline{\text{RESET}}$ High Width	60		ns	
115	Tdres(STB)	$\overline{\text{RESET}}$ Rise to $\overline{\text{STB}}$ Fall	60		ns	3
116	TdDSf(RDY)	$\overline{\text{DS}}$ Fall to $\overline{\text{RDY}}$ Fall Delay		50	ns	
117	TdWRf(RDY)	$\overline{\text{WR}}$ Fall to $\overline{\text{RDY}}$ Fall Delay		50	ns	
118	TdWRr(RDY)	$\overline{\text{WR}}$ Rise to $\overline{\text{RDY}}$ Rise Delay		40	ns	
119	TdRDf(RDY)	$\overline{\text{RD}}$ Fall to $\overline{\text{RDY}}$ Fall Delay		50	ns	
120	TdRAKf(RDY)	$\overline{\text{RxACK}}$ Fall to $\overline{\text{RDY}}$ Fall Delay		50	ns	
121	TdRAKr(RDY)	$\overline{\text{RxACK}}$ Rise to $\overline{\text{RDY}}$ Rise Delay		40	ns	
122	TdTAKf(RDY)	$\overline{\text{TxACK}}$ Fall to $\overline{\text{RDY}}$ Fall Delay		50	ns	

Table 5. Z16C30 AC Characteristics (Continued)

No	Symbol	Parameter	Min	Max	Units	Note
123	TdTAKr(RDY)	TxACK Rise to RDY Rise Delay		40	ns	

Notes
1. Direct address is any of A/B, D/C, or AD15–AD8 used as an address bus.
2. The parameter applies only when AS is not present.
3. Strobe (STB) is any of DS, RD, WR, PITACK, RxACK or TxACK.
4. Parameter applies only if read empties the receive FIFO.
5. Parameter applies only if write fills the transmit FIFO.
6. For extended temperature part TdDSI(Wf) max = 220 ns.
7. For extended temperature part TdDSF(TRQ) max = 75 ns.

USC Timing

The USC interface timing is similar to that found on a static RAM, except that it is much more flexible. Up to eight separate timing strobe signals may be present on the interface: DS, RD, WR, PITACK, RxACKA, RxACKB, TxACKA, and TxACKB. Only one of these timing strobes may be active at any time. Should the external logic activate more than one of these strobes at the same time the USC will enter a pre-reset state that is only exited by a hardware reset. Do not allow overlap of timing strobes. The timing diagrams beginning on the next page illustrate the different bus transactions possible with the necessary setup hold and delay times.

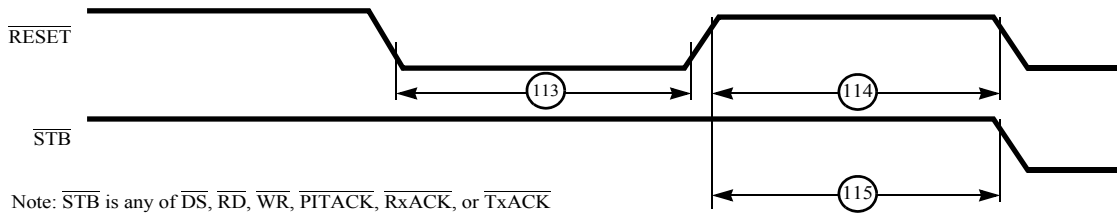


Figure 6. Reset Timing

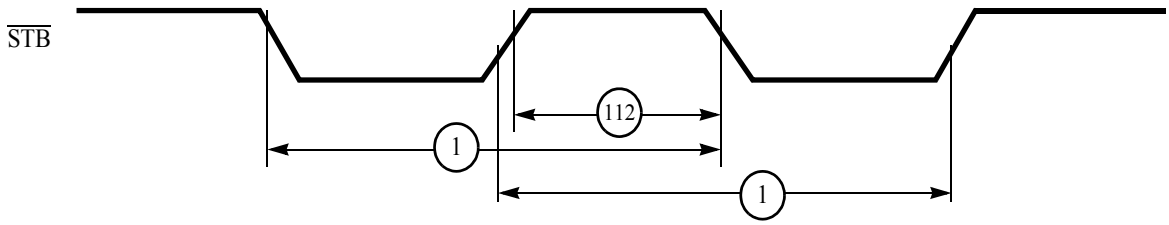
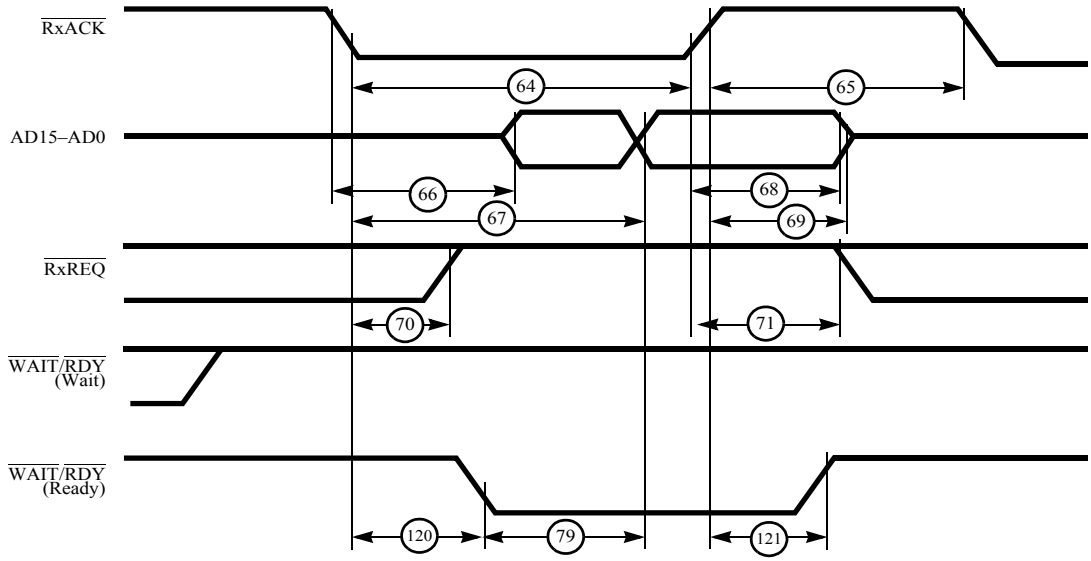


Figure 7. Bus Cycle Timing



Note: STB is any of DS, RD, WR, PITACK, RxACK, or TxACK

Figure 8. DMA Read Cycle

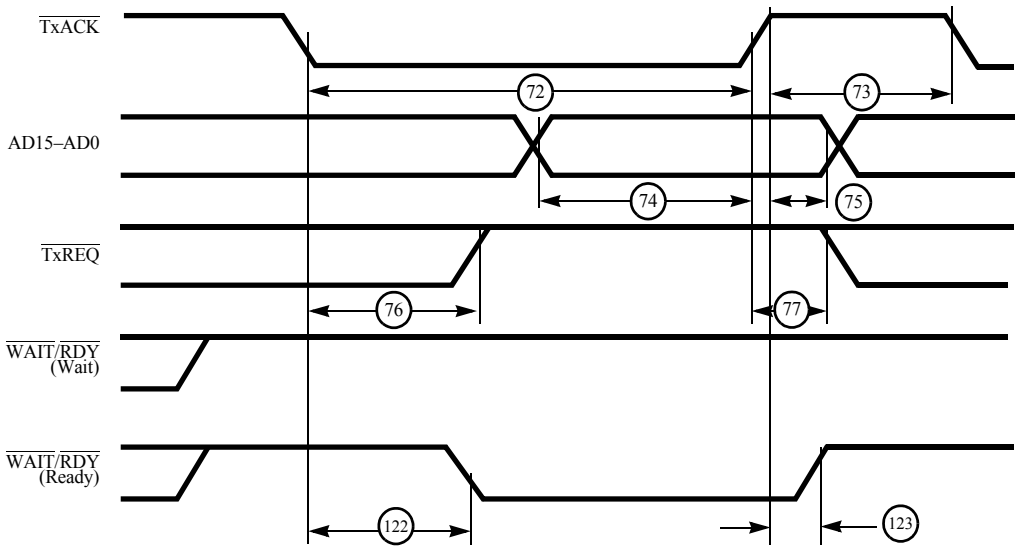


Figure 9. DMA Write Cycle

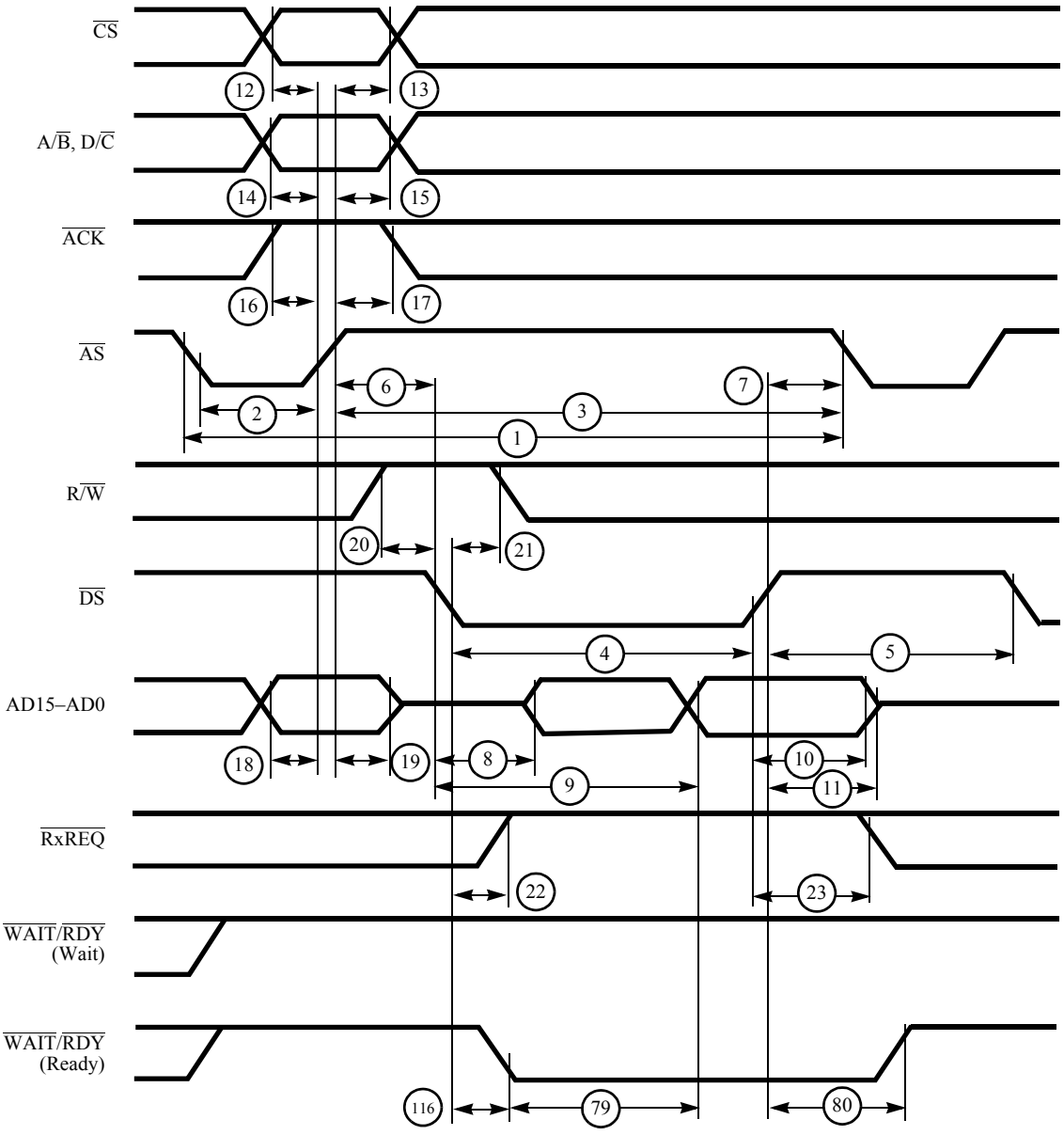


Figure 10. Multiplexed DS Read Cycle