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zilog
Embedded in Life
An IXYS Company

High Performance Microcontrollers

ZNEO® Z16F Series

Product Specification

PS022012-1113

PRELIMINARY

www.zilog.com

Warning: DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.

LIFE SUPPORT POLICY

ZILOG'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF ZILOG CORPORATION.

As used herein

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

Document Disclaimer

Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Section	Description	Page No.
Nov 2013	12	Signal Descriptions	Corrected active status of RD, WR and $\overline{CS}$ signals.	12
Jul 2013	11	Analog Functions	Updated the Analog Functions Block Diagram.	242
Aug 2011	10	Multi-Channel PWM Timer	Per CR#13095, corrected PWMEN description in PWM Control 0 Register (PWMCTL0) table; corrected description in PWM Deadband Register (PWMDB) table and added footnote; added same footnote to PWM Minimum Pulse Width Filter (PWMMPF), PWM Fault Mask Register (PWMFM), and PWM Fault Control Register (PWMFCTL) tables.	125, 127–129, 131
Jun 2011	09	Electrical Characteristics	Corrected V_{COFF} input offset value in Comparator Electrical Characteristics table	347
Aug 2010	08	N/A	Removed ISO information.	ii
		All	Updated logos.	All
		Table 191	Changed the Minimum, Typical and Maximum values for V_{REF} (Externally supplied Voltage Reference only).	346
Jan 2009	07	Timer 0–2 Control 0 Register	Table 62: added "Only Counter Mode should be used with this feature" to Bit 4 description.	109
		Analog Functions	ADC Overview, updated fast conversion time to 2.5µs.	243
		Electrical Characteristics	Updated Table 185.	337
		Internal Precision Oscillator	Removed reference to 32kHz.	336

Feb 2007	06	Independent and Complementary PWM Outputs	Corrected PWM Registers. Updated Edge-Aligned PWM Output figure.	117
		Electrical Characteristics	Replaced 105°C with 125°C in Tables 185 through 192. Added Figures 73 through 75.	337
		I2C Master/Slave Controller	Changes to Software Control of I2C Transactions section.	209
		Packaging	Updated Part Number Suffix Designations section.	359
		Enhanced Serial Peripheral Interface	Throughput section modified.	181
Jul 2006	05	External Interface, General-Purpose Input/Output, DMA Controller, Option Bits, On-Chip Debugger and Electrical Characteristics	Modifications done in the following chapters: External Interface, GPIO, DMA Controller, Option bits, on-chip debugger and Electrical characteristics.	37, 66, 267, 292, 298, 337
		Ordering Information	Ordering Information modified.	356
Jan 2006	04	All	Changed zneo to ZNEO in the entire document.	All
		All	Added TM symbol to ZNEO.	All
		Signal and Pin Descriptions, Interrupt Controller and Analog Functions	Modifications done to following chapters: Pin description, Interrupt controller and Analog functions.	7, 80, 242
		Ordering Information	Ordering Information modified.	356

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Document Objectives

This product specification provides detailed operating information about the Z16F2810, Z16F2811, Z16F3211, and Z16F6411 devices within Zilog's ZNEO Family of products. In this document, these four devices are collectively referred as the ZNEO or the ZNEO Z16F Series, unless specifically stated otherwise.

About This Manual

Zilog recommends that you read and understand the content contained in this product specification before setting up and using your ZNEO Z16F Series products. However, because we recognize that there are different styles of learning, this specification is designed to be used either as a procedural manual or a reference guide to important data.

Intended Audience

This document is written for Zilog customers who are experienced at working with microcontrollers, integrated circuits, or printed circuit assemblies.

Manual Conventions

The following assumptions and conventions are adopted to provide clarity and ease of use.

Courier New Typeface

Commands, code lines and fragments, hexadecimal addresses, and various executable items are distinguished from general text by the use of the Courier New typeface. Where the use of the font is not indicated, as in the Index, the name of the entity is presented in upper case.

Example. FLAGS[1] is SMRF.

Hexadecimal Values

Hexadecimal values are designated by lowercase h suffix and appear in the `Courier New` typeface.

Example. R1 is set to `F8h`.

Brackets

The square brackets, [ ], indicate a register or bus.

Example. For the register R1[7:0], R1 is an 8-bit register, R1[7] is the most significant bit, and R1[0] is the least significant bit.

Braces

The curly braces { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

Example. The 12-bit register address {0h, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0h) and two 4-bit register values taken from the register pointer (RP) and working register R1. 0h is the most significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

Parentheses

The parentheses ( ), indicate an indirect register address lookup.

Example. (R1) is the memory location referenced by the address contained in the working register R1.

Parentheses/Bracket Combinations

The parentheses ( ), indicate an indirect register address lookup and the square brackets [ ], indicate a register or bus.

Example. Assume PC[15:0] contains the value 1234h. (PC[15:0]) refers to the contents of the memory location at the address 1234h.

Use of the Words Set, Reset, and Clear

The word set implies that a register bit or a condition contains a logical 1. The words reset or clear imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word logical may not be included; however, it is implied.

Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[*n*:*n*].

Example. ADDR[15:0] refers to bit 15 through bit 0 of the address.