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Z80 Family

CPU Peripherals

User Manual

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Counter/Timer Channels

CTC FEATURES

- Four independently programmable counter/timer channels (CTC), each with a readable down-counter and a selectable 16 or 256 prescaler. Down-counters are reloaded automatically at zero count
- Selectable positive or negative trigger initiates timer operation
- Three channels have zero count/timeout outputs capable of driving Darlington transistors
- NMOS version for high-cost performance solutions
- CMOS version for the designs requiring low power consumption
- NMOS Z0843004 - 4 MHz, Z0843006 - 6.17 MHz
- CMOS Z84C3006 - dc to 6.17 MHz, Z84C3008 dc to 8 MHz, Z84C3010 - dc to 10 MHz
- Interfaces directly to the Z80 CPU. Interfaces to the Z80 SIO for baud rate generation
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller
- A 6 MHz version supports 6.144 MHz CPU clock operation

CTC General Description

The Z80 CTC is a four-channel counter/timer that can be programmed by system software for a broad range of counting and timing applications. These four independently programmable channels satisfy common

microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified by connecting the CTC directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

The CTC allows easy programming: each channel is programmed with two bytes; a third is necessary when interrupts are enabled. When started, the CTC counts down, automatically reloads its lime constant, and resumes counting. Software timing loops are eliminated. Interrupt processing is simplified because only one vector needs to be specified; the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is packaged in 28-pin DIPs, a 44-pin plastic chip carrier, and a 44-pin Quad Flat Pack. The QFP package is only available for CMOS versions.

CTC ARCHITECTURE

Overview

The internal structure of the Z80 CTC consists of:

- A Z80 CPU bus interface, internal control logic
- Four sets of Counter/Timer Channel logic
- Interrupt control logic

The four independent, counter/timer channels are identified by sequential numbers from 0 to 3. The CTC can generate a unique interrupt vector for each separate channel for automatic vectoring to an interrupt service routine. The four channels can be connected in four contiguous slots in the standard Z80 priority chain with channel number 0 having the highest

priority. The CPU bus interface logic allows the CTC device to interface directly to the CPU with no other external logic. However, port address decoders and/or line buffers may be required for large systems. A block diagram of the Z80 CTC is depicted in Figure 1.

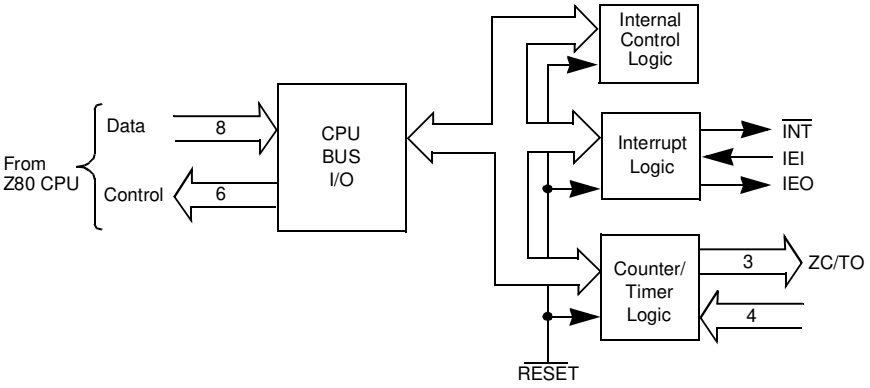

Figure 1. CTC Block Diagram

Structure of Channel Logic

The structure of one of the four sets of Counter/Timer channel logic is illustrated in Figure 2. This logic is composed of:

- Two registers
- Two counters
- Control logic

The registers consist of an 8-bit Time Constant register and an 8-bit Channel Control register. The counters consist of an 8-bit CPU-readable down-counter and an 8-bit prescaler.

In Channel Control Register and Logic

The Channel Control register (8-bit) and Logic is written to by the CPU to select the modes and parameters of the channel. Within the CTC device, four such registers correspond to the four Counter/Timer channels. The register to be written to is determined by the encoding of two channel select input pins: CS0 and CS1, which are usually attached to A0 and A1 of the CPU address bus. The channel values are described in Table 1.

Table 1. Channel Values

	CS0	CS1
Channel 0	0	0
Channel 1	0	1
Channel 2	1	0
Channel 3	1	1

In the control word, which is written to program each Channel Control register, bit 0 is always set; the other seven bits are programmed to select alternatives on the channel's operating modes and parameters. These values are described in Table 2. For a more complete discussion, see "CTC Operating Modes" on page 16 and "CTC Programming" on page 18).

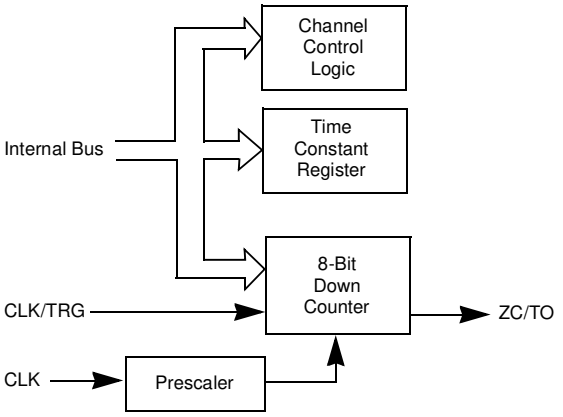

Figure 2. Channel Block Diagram

Table 2. Channel Control Register

7	6	5	4	3	2	1	0
Interrupt	Mode	Prescaler Value*	CLK/TRG Section	Time Trigger*	Time Constant	Reset	Control or Vector
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Field	R/W	Value	Description
7	Interrupt	R/W	1 0	Enable Interrupt Disable Interrupt
6	Mode	R/W	1 0	COUNTER Mode TIMER Mode
5	Prescaler Value*	R/W	1 0	256 16
4	CLK/TRG Edge Section	R/W	1 0	Rising Edge Falling Edge
3	Time Trigger*	R/W	1 0	CLK/TRG Pulse Starts Timer Automatic trigger when time constant is loaded
2	Time Constant	R/W	1 0	Time Constant Follows No Time Constant Follows
1	Reset	R/W	1 0	Software Reset Continue Operation
0	Control or Vector	R/W	1 0	Control Vector
*TIMER mode only				

The Prescaler

The prescaler is an 8-bit device that is used in the TIMER mode only. The prescaler is programmed by the CPU through the Channel Control register to divide its input, the System clock (0), by 16 or 256. The output of the prescaler is then fed as an input to clock the down-counter. Each time that

the down-counter counts to zero, the down-counter is automatically reloaded with the contents of the Time Constant register. This process divides the System clock by an additional factor of the time constant. Each time the down-counter counts to zero, its output, Zero Count/Timeout (ZC/TO), is pulsed High.

The Time Constant Register

The 8-bit Time Constant register is used in both Counter and Timer modes. It is programmed by the CPU just after the channel control word, with an integer time constant value of 1 through 256. This register loads the programmed value to the down-counter when the CTC is first initialized and reloads the same value into the down-counter automatically whenever it counts down thereafter to zero. If a new time constant is loaded into the Time Constant register while a channel is counting or timing, the present down count is completed before the new time constant is loaded into the down counter. For details about writing a time constant to a CTC channel, see “CTC Programming” on page 18

The Down-Counter

The down-counter is an 8-bit register that is used in both COUNTER and TIMER modes. This register is loaded by the Time Constant register both initially, and when it counts down to zero. In the COUNTER mode, the down-counter is decremented by each external clock edge. In the TIMER mode, it is decremented by the clock output of the prescaler. By performing a simple I/O Read at the port address assigned to the selected CTC channel, the CPU can access the contents of the down-counter and obtain the number of counts-to-zero. Any of the four CTC channels may be programmed to generate an interrupt request sequence each time the zero count is reached.

In Channels 0, 1, and 2, a signal pulse appears at the corresponding ZC/TO pin when the zero count condition is reached. Because of package pin limitations, however, Channel 3 does not have this pin and so may be used only in applications where this output pulse is not required.

Interrupt Control Logic

The Interrupt Control Logic insures that the CTC acts in accordance with Z80 system interrupt protocol for Nested Priority Interrupting and Return From Interrupt. The priority of any system device is determined by its physical location in a daisy-chain configuration. Two signal lines, CIEI and IEO, are provided in CTC devices to form this system daisy-chain. The device closest to the CPU has the highest priority. Within the CTC, interrupt priority is predetermined by channel number, with Channel 0 having highest and Channel 3 the lowest priority. See Table 3. The purpose of a CTC-generated interrupt, as with any peripheral device, is to force the CPU to execute an interrupt service routine. According to Z80 system interrupt protocol, lower priority devices or channels may not interrupt higher priority devices or channels that have not had their interrupt service routines completed. However, high priority devices or channels may interrupt the servicing of lower priority devices or channels.

Table 3. Interrupt Vector Register

7	6	5	4	3	2	1	0
Supplied by User					Channel Identifier		Word
R/W					R/W		R/W

Bit Number	Field	R/W	Value	Description
7–3	Reserved	R/W		Supplied by User
2–1	Channel Identifier (Automatically inserted by CTC)	R/W	11 10 01 00	Channel 3 Channel 2 Channel 1 Channel 0
0	Word	R/W	1 0	Control Interrupt Vector