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## ZNEO32! Cortex-M3

# Z32F0641 MCU

## Product Specification

PS034404-0417

PRELIMINARY

ZNEO32!

32 Bit Microcontrollers

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# Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

| Date | Revision Level | Description | Page |
|---|---|---|---|
| Apr 2017 | 04 | Updated part numbers to include the Cortex M identifier. | All |
| Aor 2016 | 03 | Added timing information for peripherals; global edits for clarity. | All |
| Feb 2016 | 02 | Updated Figure 18.2 LQFP-32 Package Dimension. | 178 |
| Nov 2015 | 01 | Original issue. | |

# 1. Overview

## Introduction

Zilog's Z32F0641 MCU, a member of the ZNEO32! Family of microcontrollers, is a cost-effective and high-performance 32-bit microcontroller. The Z32F0641 MCU provides a 3-phase PWM generator unit which is suitable for inverter bridges, including motor drive systems.

Two 12-bit high speed ADC units with 16-channel analog multiplexed inputs support feedback retrieval from the inverter bridge. Multiple powerful external serial interfaces help communicate with on-board sensors and devices.

Figure 1.1 shows a block diagram of the Z32F0641 MCU.

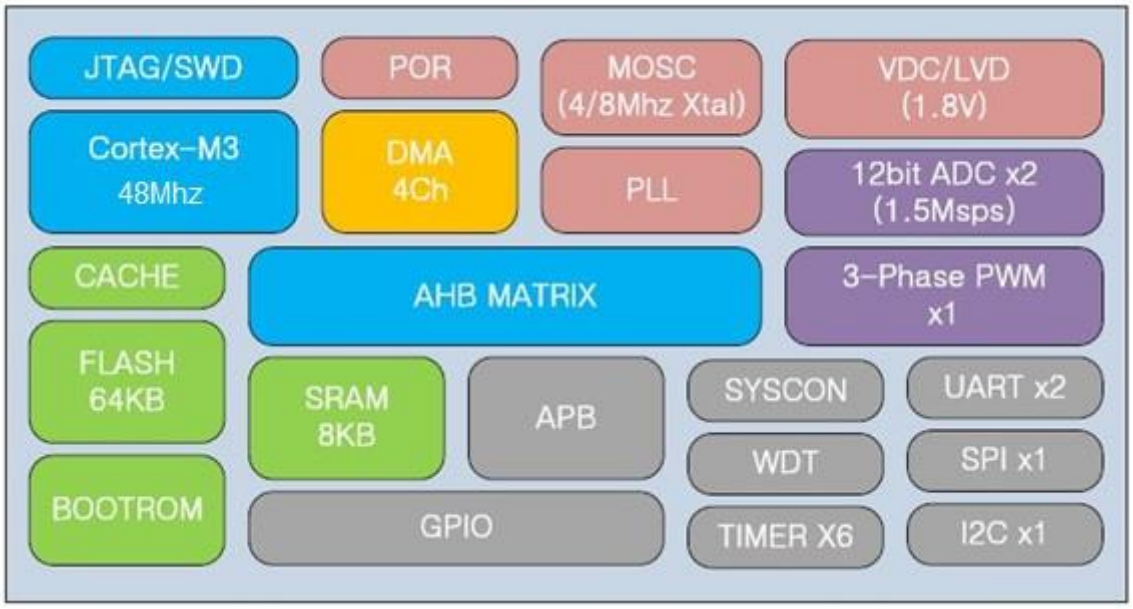


**Figure 1.1 Block Diagram**

Figure 1.2 and Figure 1.3 show the pin layouts.

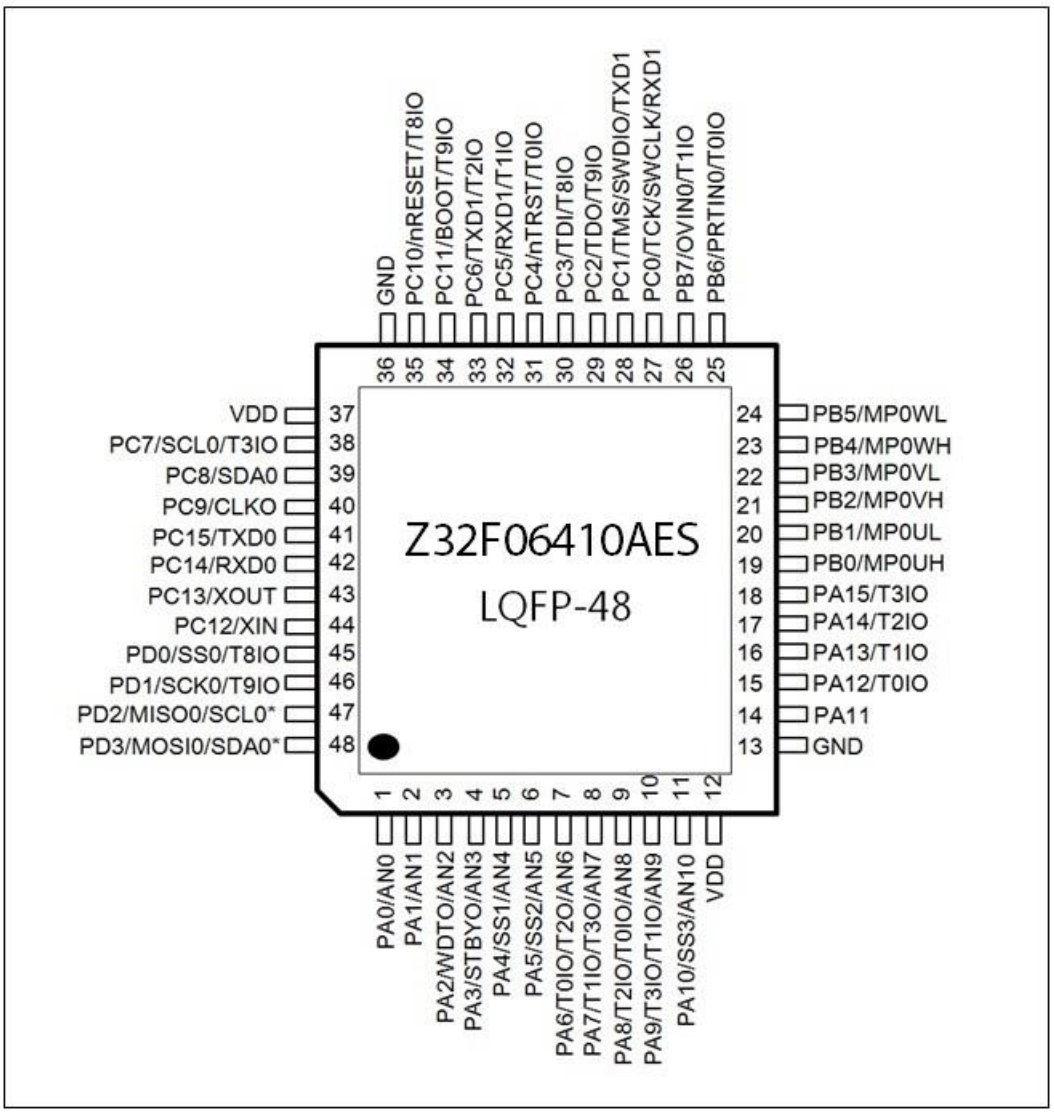


**Figure 1.2 Pin Layout (LQFP-48)**

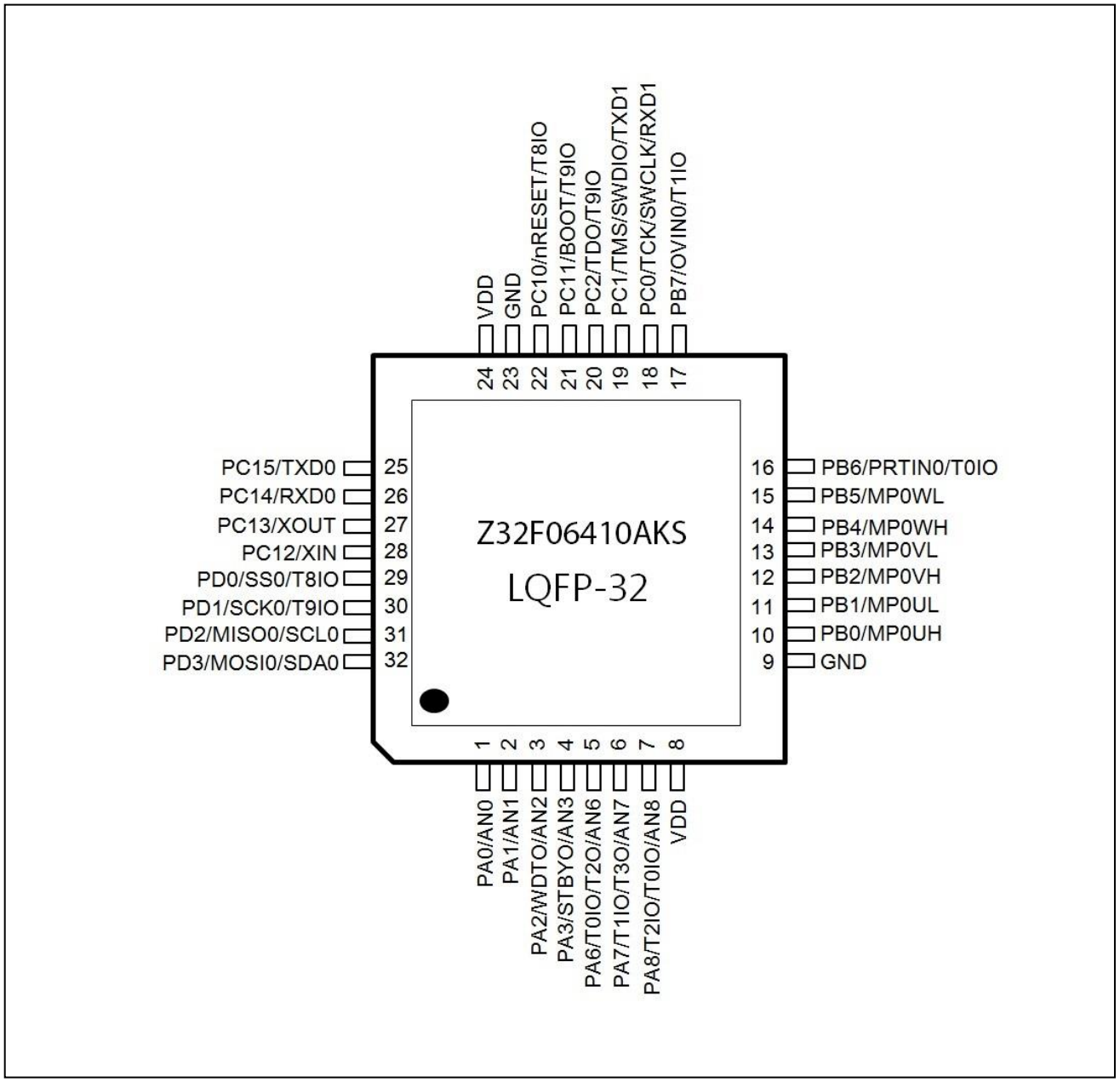


**Figure 1.3 Pin Layout (LQFP-32)**

# Product Features

The Z32F0641 MCU offers the following features:

- High Performance low-power Cortex-M3 core
- 64 KB code Flash memory with cache function
- 8 KB SRAM
- 3-Phase PWM with ADC triggering function
- 1.5Msps high-speed ADC with sequential conversion function
  - 2 units with 11 channel Inputs
- Watchdog timer
- Six general purpose timers
  - Periodic, One-shot, PWM, Capture mode
  - Multi-timer synchronization option
- External communication ports:
  - 2 UARTs
  - 1 $I^2C$
  - 1 SPI
- Direct Memory Access (DMA) controller with 4 channels
- System fail-safe function by clock monitoring
- XTAL OSC fail monitoring
- Debug and emergency stop function
- Serial Wire Debug (SWD) and JTAG Debugger (JTAG is only for LQFP-48)
- Supports UART and SPI ISP
- Two types of package options
  - LQFP-48 (0.5mm pitch)
  - LQFP-32 (0.65mm pitch)
- Industrial grade operating temperature (-40 ~ +85℃)

**Table 1.1 Device Type**

| Part Number | Flash | SRAM | UART | SPI | I2C | MPWM | ADC | I/O Ports | Package |
|---|---|---|---|---|---|---|---|---|---|
| Z32F06410AES | 64KB | 8KB | 2 | 1 | 1 | 1 | 2-unit 11 ch | 44 | LQFP-48 |
| Z32F06410AKS | 64KB | 8KB | 2 | 1 | 1 | 1 | 2-unit 8 ch | 30 | LQFP-32 |

# Architecture

## Block Diagram

An internal block diagram of the Z32F0641 MCU is shown in Figure 1.4.

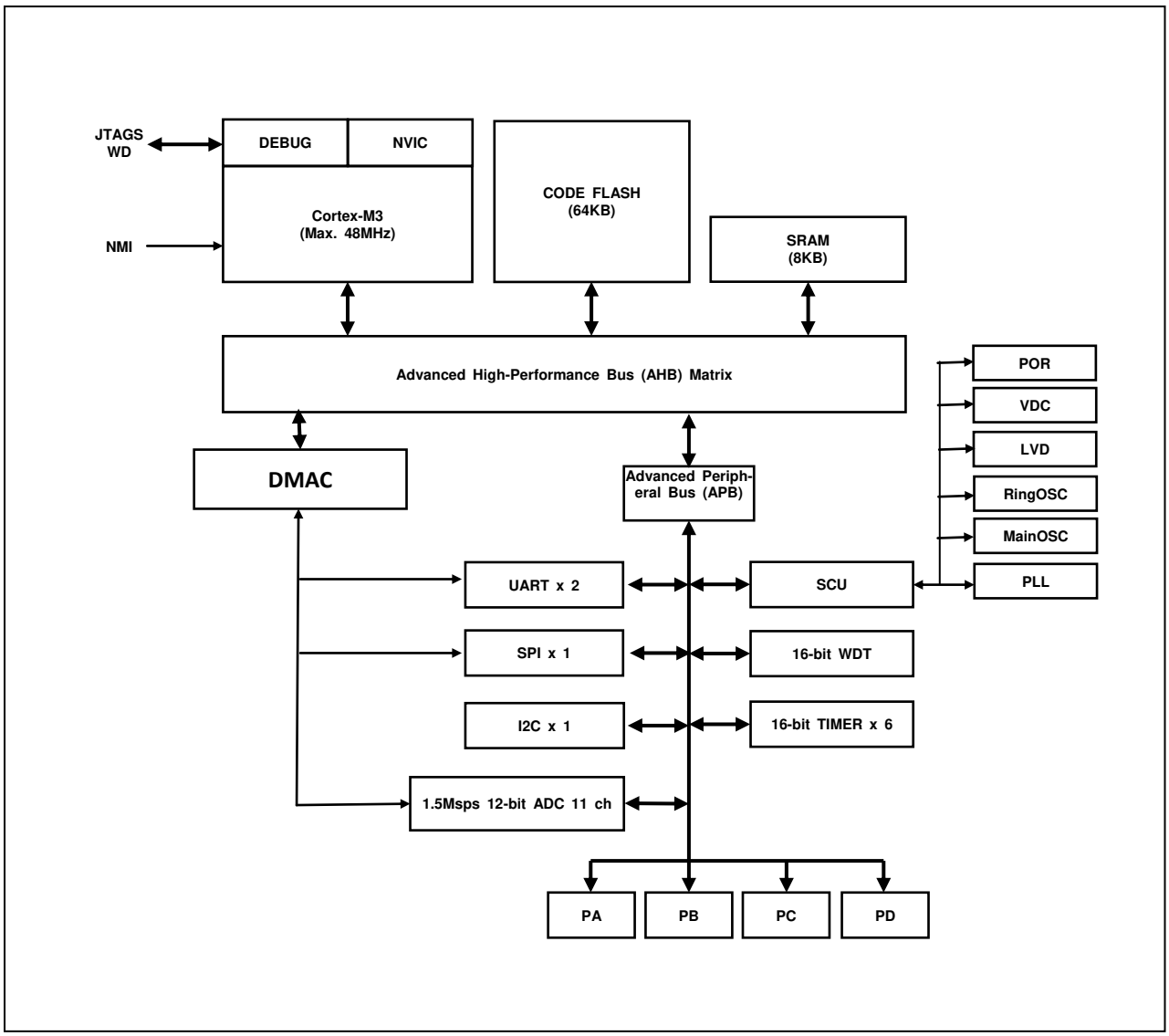


**Figure 1.4 Internal Block Diagram**

# Functional Description

The following section provides an overview of the features of the Z32F0641 microcontroller.

## ARM Cortex-M3

- ARM-powered Cortex-M3 core based on ARMv7M architecture, which is optimized for small-size and low-power systems. On core system timer (SYSTICK) provides a simple 24-bit timer that enables easy management of system operations
- Thumb-compatible Thumb-2 only instruction set processor core makes code high-density
- Hardware division and single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling
- JTAG and SWD debugging features
- Maximum 48 MHz operating frequency with zero wait execution

## Nested Vector-Interrupt Controller (NVIC)

- The ARM Nested Vectored Interrupt Controller (NVIC) on the ARM Cortex-M3 core handles all internal and external exceptions. When an interrupt condition is detected, the processor state is automatically stored to the stack and automatically restored from the stack at the end of interrupt service routine.
- The vector is fetched in parallel to the state saving, which enables efficient interrupt entry.
- The processor supports tail-chaining, which allows for back-to-back interrupts to be performed without the overhead of state saving and restoring

## 64 KB Internal Code Flash Memory

- The Z32F0641 MCU provides internal 64 KB code Flash memory and its controller, which is sufficient to program the motor algorithm and control the system. Self-programming is available and ISP and JTAG programming is also supported in boot or debugging mode.
- Instruction and data cache buffer are present and overcome the low-bandwidth Flash memory. The CPU can execute from Flash memory with zero wait state up to 48 MHz bus frequency.

## 8 KB 0-wait Internal SRAM

- On chip 8 KB 0-wait SRAM can be used for working memory space and program code can be loaded on this SRAM

## Boot Logic

- Smart boot logic supports Flash programming. The Z32F0641 MCU can be accessed by an external boot pin; UART and SPI programming are available in Boot Mode

## System Control Unit

- The System Control Unit (SCU) block manages internal power, clock, reset, and Operation Mode. The SCU also controls analog blocks (Oscillator Block, VDC and LVD)

## 32-bit Watchdog Timer

- The Watchdog Timer (WDT) performs the system monitoring function. The WDT generates an internal reset or interrupt if the system is in abnormal state

## Multi-purpose 16-bit Timer

- Six-channel 16-bit general purpose timers support the following functions
  - Periodic timer mode
  - Counter mode
  - PWM mode
  - Capture mode

- Built-in timer also supports counter-synchronization mode which can generate synchronized waves and timing

## Motor PWM Generator

- 3-phase Motor PWM Generator is implemented. 16-bit up/down counter with prescaler supports triangular and saw tooth waveforms
- PWM has the ability to generate internal ADC trigger signals to measure the signal on time
- Dead time insertion and emergency stop functionality provide overcurrent protection for the chip and system

## Serial Peripheral Interface (SPI)

- The Serial Peripheral Interface (SPI) block provides synchronous serial communication. The Z32F0641 MCU has 1 channel SPI module which includes the DMA function supported by a DMA controller. Transfer data is moved to/from the memory area without CPU operation
- Boot Mode uses this SPI block to download the Flash program

## Inter-Integrated Circuit Interface

- The Z32F0641 MCU has 1 channel Inter-Integrated Circuit ($I^2C$) block which supports up to 400 kHz $I^2C$ communication. Master and slave modes are supported

## Universal Asynchronous Receiver/Transmitter

- The Z32F0641 MCU has 2 channels Universal Asynchronous Receiver/Transmitter (UART) block. For accurate baud rate control, the fractional baud rate generator is provided
- The UART features the DMA function, supported by a DMA controller. Transfer data is moved to/from the memory area without CPU operation

## General PORT I/Os

- 16-bit PA, PB, PC, and PD ports are available and provide multiple functionality:
  - General I/O port
  - Independent bit set/clear function
  - External interrupt input port
- Programmable pull-up and open-drain selection
- On-chip input debounce filter

## 12-bit Analog-to-Digital Converter (ADC)

- 2 built-in Analog-to-Digital Converters (ADC) can convert analog signals up to 1.5 Msps conversion rate. 11-channel analog MUX provides various combinations from external analog signals.
- The ADC features the DMA function, supported by a DMA controller. Transfer data is moved to/from the memory area without CPU operation.

# Pin Description

Pin configurations are listed in Table 1.2.

**Table 1.2 Pin Description**

| Pin Name | | Pin Name | Type | Description | Remark |
|---|---|---|---|---|---|
| LQFP48 | LQFP32 | | | | |
| 1 | 1 | PA0* | IOUS | PORT A Bit 0 Input/Output | |
| | | AN0 | IA | Analog Input 0 | |
| 2 | 2 | PA1* | IOUS | PORT A Bit 1 Input/Output | |
| | | AN1 | IA | Analog Input1 | |
| 3 | 3 | PA2* | IOUS | PORT A Bit 2 Input/Output | |
| | | WDTO | O | Watchdog timer overflow output | |
| | | AN2 | IA | Comparator 2 Input | |
| 4 | 4 | PA3* | IOUS | PORT A Bit 3 Input/Output | |
| | | AN3 | IA | Analog Input 3 | |
| 5 | - | PA4* | IOUS | PORT A Bit 4 Input/Output | |
| | | SS1 | I/O | Slave Select 1 for SPI0 | |
| | | AN4 | IA | Analog Input 4 | |
| 6 | - | PA5* | IOUS | PORT A Bit 5 Input/Output | |
| | | SS2 | I/O | Slave Select 2 for SPI0 | |
| | | AN5 | IA | Analog Input 5 | |
| 7 | 5 | PA6* | IOUS | PORT A Bit 6 Input/Output | |
| | | T0IO | I/O | Timer 0 Input/Output | |
| | | T2IO | I/O | Timer 2 Input/Output | |
| | | AN6 | IA | Analog Input 6 | |
| 8 | 6 | PA7* | IOUS | PORT A Bit 7 Input/Output | |
| | | T1IO | I/O | Timer 1 Input/Output | |
| | | T3IO | I/O | Timer 3 Input/Output | |
| | | AN7 | IA | Analog Input 7 | |
| 9 | 7 | PA8* | IOUS | PORT A Bit 8 Input/Output | |
| | | T2IO | I/O | Timer 2 Input/Output | |
| | | T0IO | I/O | Timer 0 Input/Output | |
| | | AN8 | IA | Analog Input 8 | |
| 10 | - | PA9* | IOUS | PORT A Bit 9 Input/Output | |
| | | T3IO | I/O | Timer 3 Input/Output | |
| | | T1IO | I/O | Timer 1 Input/Output | |
| | | AN9 | IA | Analog Input 9 | |
| 11 | - | PA10* | IOUS | PORT A Bit 10 Input/Output | |
| | | SS3 | Output | ETM Trace Data 1 | |
| | | AN10 | IA | Analog Input 10 | |
| 12 | 8 | VDD | P | VDD | |
| 13 | 9 | GND | P | Ground | |
| 14 | - | PA11* | IOUS | PORT A Bit 11 Input/Output | |
| | | | | | |
| 15 | - | PA12* | IOUS | PORT A Bit 12 Input/Output | |
| | | T0IO | I/O | Timer 0 Input/Output | |
| | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| 16 | - | PA13* | IOUS | PORT A Bit 13 Input/Output | |
| | | T1IO | I/O | Timer 1 Input/Output | |
| | | | | | |
| 17 | - | PA14* | IOUS | PORT A Bit 14 Input/Output | |
| | | T2IO | I/O | Timer 2 Input/Output | |
| | | | | | |
| 18 | - | PA15* | IOUS | PORT A Bit 15 Input/Output | |
| | | T3IO | I/O | Timer 3 Input/Output | |
| | | | | | |
| 19 | 10 | PB0 | IOUS | PORT B Bit 0 Input/Output | |
| | | PWM0UH | Output | PWM0 UH Output | |
| 20 | 11 | PB1 | IOUS | PORT B Bit 1 Input/Output | |
| | | PWM0UL | Output | PWM0 UL Output | |
| 21 | 12 | PB2 | IOUS | PORT B Bit 0 Input/Output | |
| | | PWM0VH | Output | PWM0 VH Output | |
| 22 | 13 | PB3 | IOUS | PORT B Bit 1 Input/Output | |
| | | PWM0VL | Output | PWM0 VL Output | |
| 23 | 14 | PB4 | IOUS | PORT B Bit 4 Input/Output | |
| | | PWM0WH | Output | PWM0 WH Output | |
| 24 | 15 | PB5 | IOUS | PORT B Bit 5 Input/Output | |
| | | PWM0WL | Output | PWM0 WL Output | |
| 25 | 16 | PB6 | IOUS | PORT B Bit 6 Input/Output | |
| | | PRTIN0 | Input | PWM0 Protection Input signal 0 | |
| | | T0IO | I/O | Timer 0 Input/Output | |
| 26 | 17 | PB7 | IOUS | PORT B Bit 7 Input/Output | |
| | | OVIN0 | Input | PWM0 Over-voltage input signal 0 | |
| | | T1IO | I/O | Timer 1 Input/Output | |
| 27 | 18 | PC0 | IOUS | PORT C Bit 0 Input/Output | |
| | | TCK/SWCK | Input | JTAG TCK, SWD Clock Input | |
| | | RXD1 | Input | UART0 Rx Data Input | |
| 28 | 19 | PC1 | IOUS | PORT C Bit 1 Input/Output | |
| | | TMS/SWDIO | I/O | JTAG TMS, SWD Data Input/Output | |
| | | TXD1 | Input | UART0 Tx Data Output | |
| 29 | 20 | PC2 | IOUS | PORT C Bit 2 Input/Output | |
| | | TDO/SWO | Output | JTAG TDO, SWO Output | |
| | | T8IO | I/O | Timer 8 Input/Output | |
| 30 | - | PC3 | IOUS | PORT C Bit 3 Input/Output | |
| | | TDI | Input | JTAG TDI Input | |
| | | T9IO | I/O | Timer 9 Input/Output | |
| 31 | - | PC4 | IOUS | PORT C Bit 4 Input/Output | |
| | | nTRST | Input | JTAG nTRST Input | |
| | | T0IO | Input | Timer 0 input/Output | |
| 32 | - | PC5 | IOUS | PORT C Bit 5 Input/Output | |
| | | RXD1 | Input | UART1 RXD Input | |
| | | T1IO | I/O | Timer 1 input/Output | |
| 33 | - | PC6 | IOUS | PORT C Bit 6 Input/Output | |
| | | TXD1 | Output | UART1 TXD Output | |

| | | | | | |
|---|---|---|---|---|---|
| | | T2IO | I/O | Timer 2 input/Output | |
| 34 | 21 | PC11 | IOUS | PORT C Bit 11 Input/Output | |
| | | BOOT | Input | Boot mode Selection Input | |
| | | T9IO | I/O | Timer 9 input/Output | |
| 35 | 22 | PC10 | IOUS | PORT C Bit 10 Input/Output | |
| | | nRESET | Input | External Reset Input | Pull-up |
| | | T8IO | I/O | Timer 8 input/Output | |
| 36 | 23 | GND | P | Ground | |
| 37 | 24 | VDD | P | VDD | |
| 38 | - | PC7 | IOUS | PORT C Bit 7 Input/Output | |
| | | SCL0 | Output | $I^2C$ Channel 0 SCL In/Out | |
| | | T3IO | I/O | Timer 3 input/Output | |
| 39 | - | PC8 | IOUS | PORT C Bit 8Input/Output | |
| | | SDA0 | Output | $I^2C$ Channel 0 SDA In/Out | |
| 40 | - | PC9 | IOUS | PORT C Bit 9 Input/Output | |
| | | CLKO | Output | System Clock Output | |
| 41 | 25 | PC15 | IOUS | PORT C Bit 14 Input/Output | |
| | | TXD0 | Output | UART0 TXD Output | |
| | | MISO0 | I/O | SPI0 Master-Input/Slave-Output | |
| 42 | 26 | PC14 | IOUS | PORT C Bit 14 Input/Output | |
| | | RXD0 | Input | UART0 RXD Input | |
| | | MOSI0 | I/O | SPI0 Master-Output/Slave-Input | |
| 43 | 27 | PC13 | IOUS | PORT C Bit 13 Input/Output | |
| | | XOUT | OA | External Crystal Oscillator Output | |
| 44 | 28 | PC12 | IOUS | PORT C Bit 12 Input/Output | |
| | | XIN | IA | External Crystal Oscillator Input | |
| 45 | 29 | PD0 | IOUS | PORT D Bit 0 Input/Output | |
| | | SS0 | I/O | SPI1 Slave Select | |
| | | T8IO | I/O | Timer 8 input/Output | |
| 46 | 30 | PD1 | IOUS | PORT D Bit 1 Input/Output | |
| | | SCK0 | I/O | SPI0 Clock Input/Output | |
| | | T9IO | I/O | Timer 9 input/Output | |
| 47 | 31 | PD2 | IOUS | PORT D Bit 2 Input/Output | |
| | | MISO0 | I/O | SPI Channel 0 Master In / Slave Out | |
| | | SCL0 | Output | $I^2C$ Channel 0 SCL In/Out | |
| 48 | 32 | PD3* | IOUS | PORT D Bit 3 Input/Output | |
| | | MOSI0 | I/O | SPI Channel 0 Master Out / Slave In | |
| | | SDA0 | Output | $I^2C$ Channel 0 SDA In/Out | |

***Notation:**

I=Input, O=Output, U=Pull-up, D=Pull-down,

S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power

(*) Selected pin function after reset condition

Pin order may be changed with revision notice.

# Memory Map

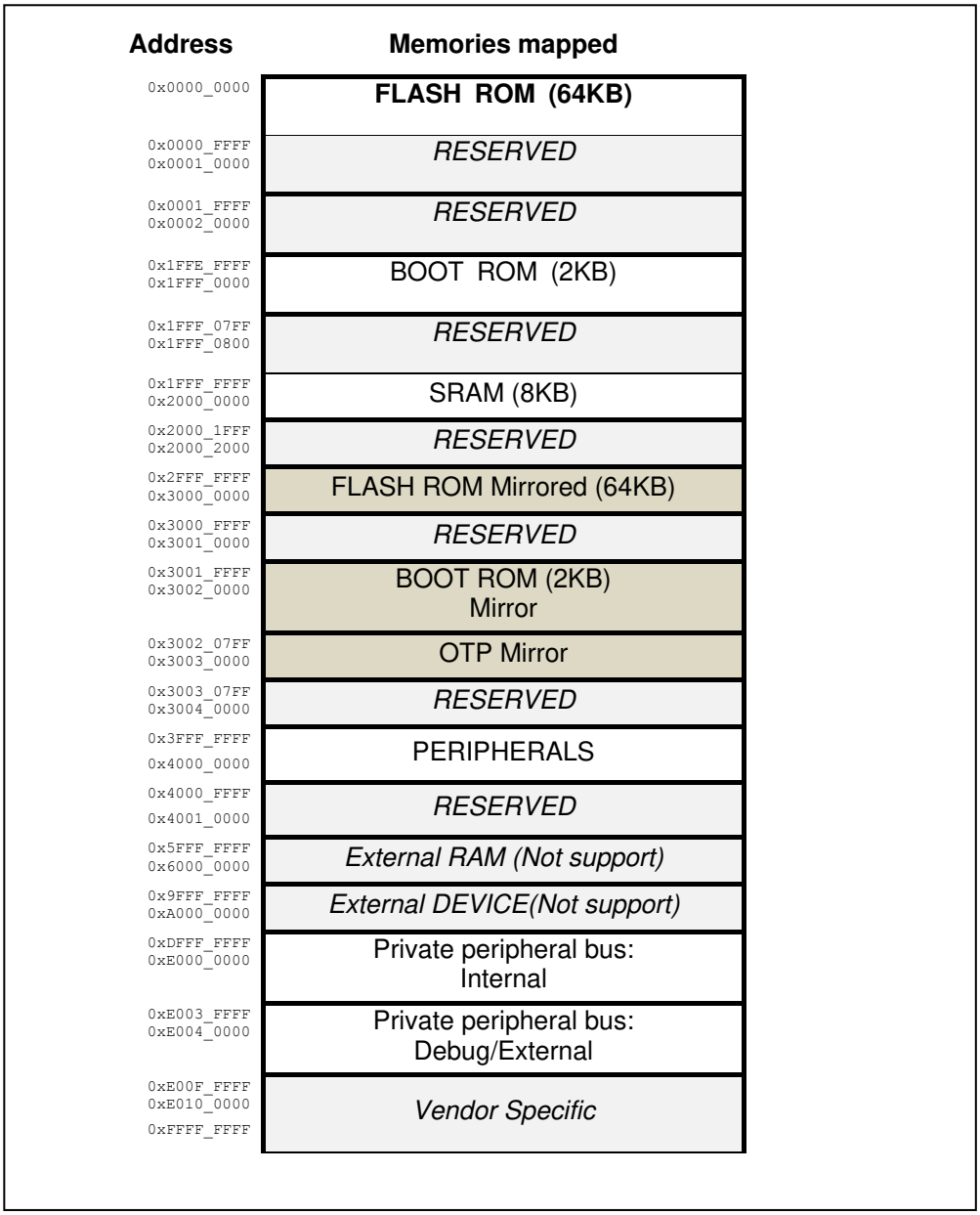


**Figure 1.5 Main Memory Map**

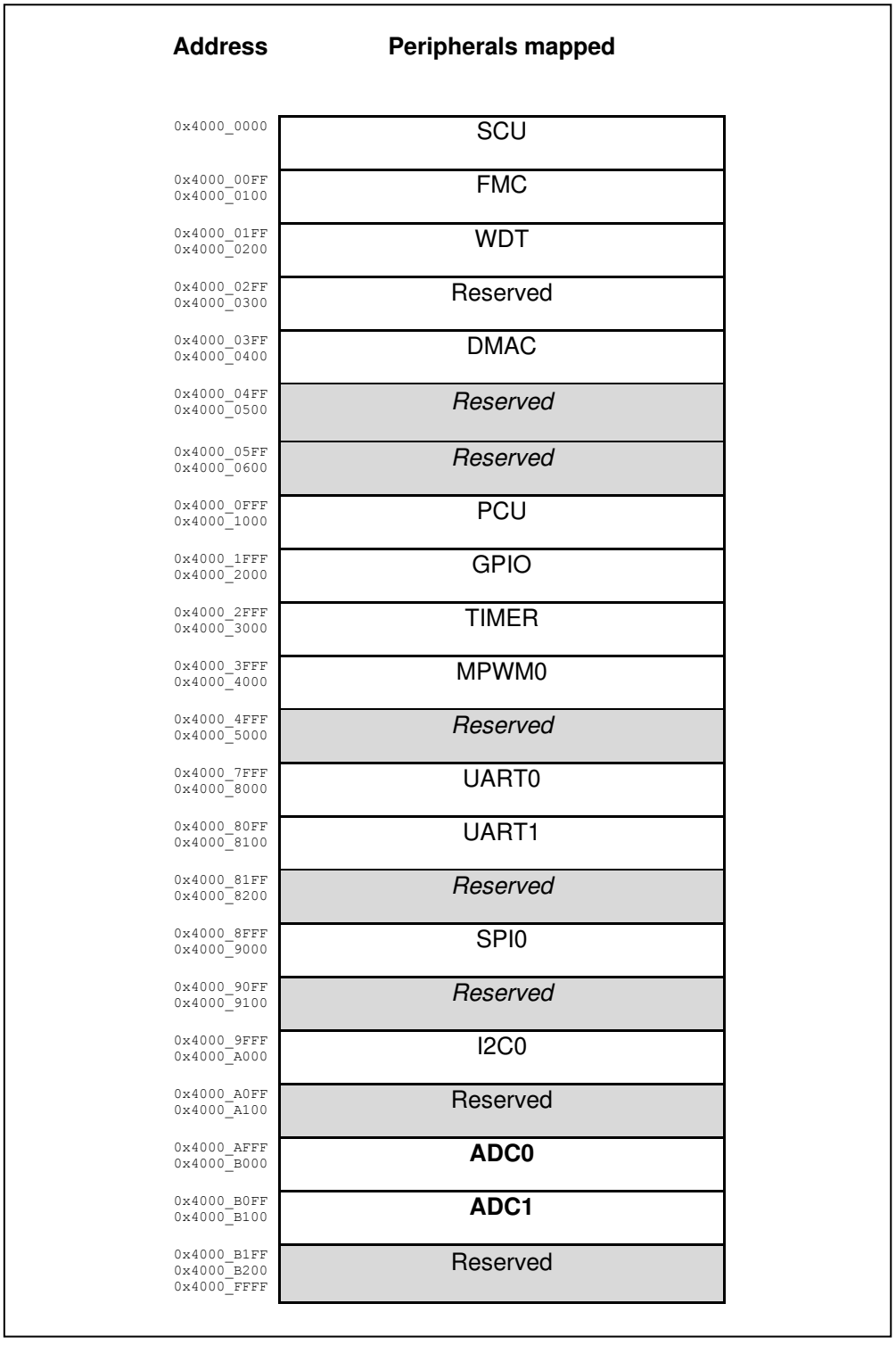


**Figure 1.6 Peripheral Memory Map**

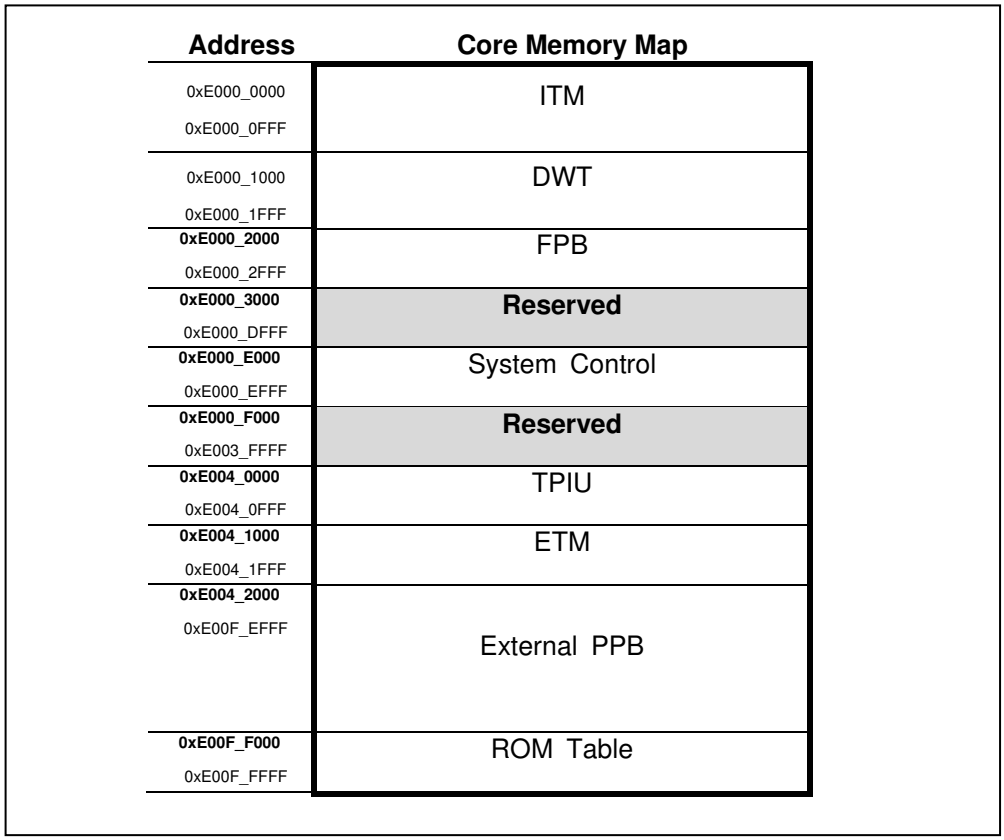


**Figure 1.7 Cortex-M3 Private Memory Map**

**Note:** Refer to document number DDI337 from ARM for more information about the memory maps.

# 2. CPU

## Cortex-M3 Core

The CPU core is supported by the ARM Cortex-M3 processor which provides a high-performance, low-cost platform. Document number DDI337 from ARM provides more information about Cortex-M3.

## Interrupt Controller

**Table 2.1 Interrupt Vector Map**

| Priority | Vector Address | Interrupt Source |
|---|---|---|
| **-16** | 0x0000_0000 | Stack Pointer |
| **-15** | 0x0000_0004 | Reset Address |
| **-14** | 0x0000_0008 | NMI Handler |
| **-13** | 0x0000_000C | Hard Fault Handler |
| **-12** | 0x0000_0010 | MPU Fault Handler |
| **-11** | 0x0000_0014 | BUS Fault Handler |
| **-10** | 0x0000_0018 | Usage Fault Handler |
| **-9** | 0x0000_001C | Reserved |
| **-8** | 0x0000_0020 | Reserved |
| **-7** | 0x0000_0024 | Reserved |
| **-6** | 0x0000_0028 | Reserved |
| **-5** | 0x0000_002C | SVCall Handler |
| **-4** | 0x0000_0030 | Debug Monitor Handler |
| **-3** | 0x0000_0034 | Reserved |
| **-2** | 0x0000_0038 | PenSV Handler |
| **-1** | 0x0000_003C | SysTick Handler |
| **0** | 0x0000_0040 | LVDDETECT |
| **1** | 0x0000_0044 | SYSCLKFAIL |
| **2** | 0x0000_0048 | XOSCFAIL |
| **3** | 0x0000_004C | WDT |
| **4** | 0x0000_0050 | Reserved |
| **5** | 0x0000_0054 | TIMER0 |
| **6** | 0x0000_0058 | TIMER1 |
| **7** | 0x0000_005C | TIMER2 |
| **8** | 0x0000_0060 | TIMER3 |
| **9** | 0x0000_0064 | Reserved |
| **10** | 0x0000_0068 | Reserved |
| **11** | 0x0000_006C | Reserved |
| **12** | 0x0000_0070 | Reserved |
| **13** | 0x0000_0074 | TIMER8 |
| **14** | 0x0000_0078 | TIMER9 |
| **15** | 0x0000_007C | Reserved |
| **16** | 0x0000_0080 | GPIOAE |
| **17** | 0x0000_0084 | GPIOAO |
| **18** | 0x0000_0088 | GPIOBE |

| | | |
|---|---|---|
| **19** | 0x0000_008C | GPIOBO |
| **20** | 0x0000_0090 | GPIOCE |
| **21** | 0x0000_0094 | GPIOCO |
| **22** | 0x0000_0098 | GPIODE |
| **23** | 0x0000_009C | GPIODO |
| **24** | 0x0000_00A0 | MPWM0 |
| **25** | 0x0000_00A4 | MPWM0PROT |
| **26** | 0x0000_00A8 | MPWM0OVV |
| **27** | 0x0000_00AC | Reserved |
| **28** | 0x0000_00B0 | Reserved |
| **29** | 0x0000_00B4 | Reserved |
| **30** | 0x0000_00B8 | Reserved |
| **31** | 0x0000_00BC | Reserved |
| **32** | 0x0000_00C0 | SPI0 |
| **33** | 0x0000_00C4 | Reserved |
| **34** | 0x0000_00C8 | Reserved |
| **35** | 0x0000_00CC | Reserved |
| **36** | 0x0000_00D0 | I2C0 |
| **37** | 0x0000_00D4 | Reserved |
| **38** | 0x0000_00D8 | UART0 |
| **39** | 0x0000_00DC | UART1 |
| **40** | 0x0000_00E0 | Reserved |
| **41** | 0x0000_00E4 | Reserved |
| **42** | 0x0000_00E8 | Reserved |
| **43** | 0x0000_00EC | ADC0 |
| **44** | 0x0000_00F0 | ADC1 |
| **45** | 0x0000_00F4 | Reserved |
| **46** | 0x0000_00F8 | Reserved |
| **47** | 0x0000_00FC | Reserved |
| **48** | 0x0000_0100 | Reserved |
| **49** | 0x0000_0104 | Reserved |
| **50** | 0x0000_0108 | Reserved |
| **51** | 0x0000_010C | Reserved |
| **52** | 0x0000_0110 | Reserved |
| **53** | 0x0000_0114 | Reserved |
| **54** | 0x0000_0118 | Reserved |
| **55** | 0x0000_011C | Reserved |
| **56** | 0x0000_0120 | Reserved |
| **57** | 0x0000_0124 | Reserved |
| **58** | 0x0000_0128 | Reserved |
| **59** | 0x0000_012C | Reserved |
| **60** | 0x0000_0130 | Reserved |
| **61** | 0x0000_0134 | Reserved |
| **62** | 0x0000_0138 | Reserved |
| **63** | 0x0000_013C | Reserved |

# 3. Boot Mode

## Boot Mode Pins

The Z32F0641 MCU includes a Boot Mode option to program internal Flash memory.To enter Boot Mode, set the BOOT pin to **Low** at reset timing.

**Note:** The Normal state of the BOOT pin is **High**.

Boot Mode supports UART boot and SPI boot.UART boot uses the UART0 port, and SPI boot uses SPI0.The pins used for Boot Mode are listed in Table 3.1.

**Table 3.1 Boot Mode Pins**

| Block | Pin Name | Dir | Description |
|---|---|---|---|
| **SYSTEM** | **nRESET/PC10** | I | Reset Input signal |
| | **BOOT/PC11** | I | '0' to enter Boot mode |
| **UART0** | **RXD0/PC14** | I | UART Boot Receive Data |
| | **TXD0/PC15** | O | UART Boot Transmit Data |
| **SPI0** | **SS0/PA12** | I | SPI Boot Slave Select |
| | **SCK0/PA13** | I | SPI Boot Clock Input |
| | **MOSI0/PA14** | I | SPI Boot Data Input |
| | **MISO0/PA15** | O | SPI Boot Data Output |

# Boot Mode Connections

Design the target board using either of the Boot Mode ports – UART or SPI. Figure 3.1 and Figure 3.2 display sample Boot Mode connections.

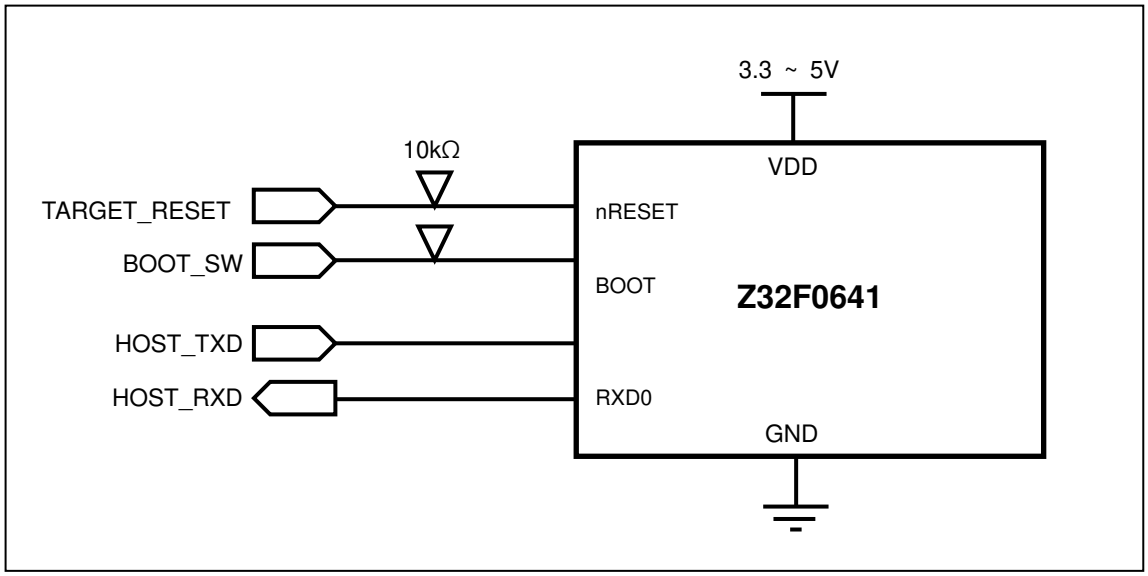


**Figure 3.1 UART Boot Connection Diagram**

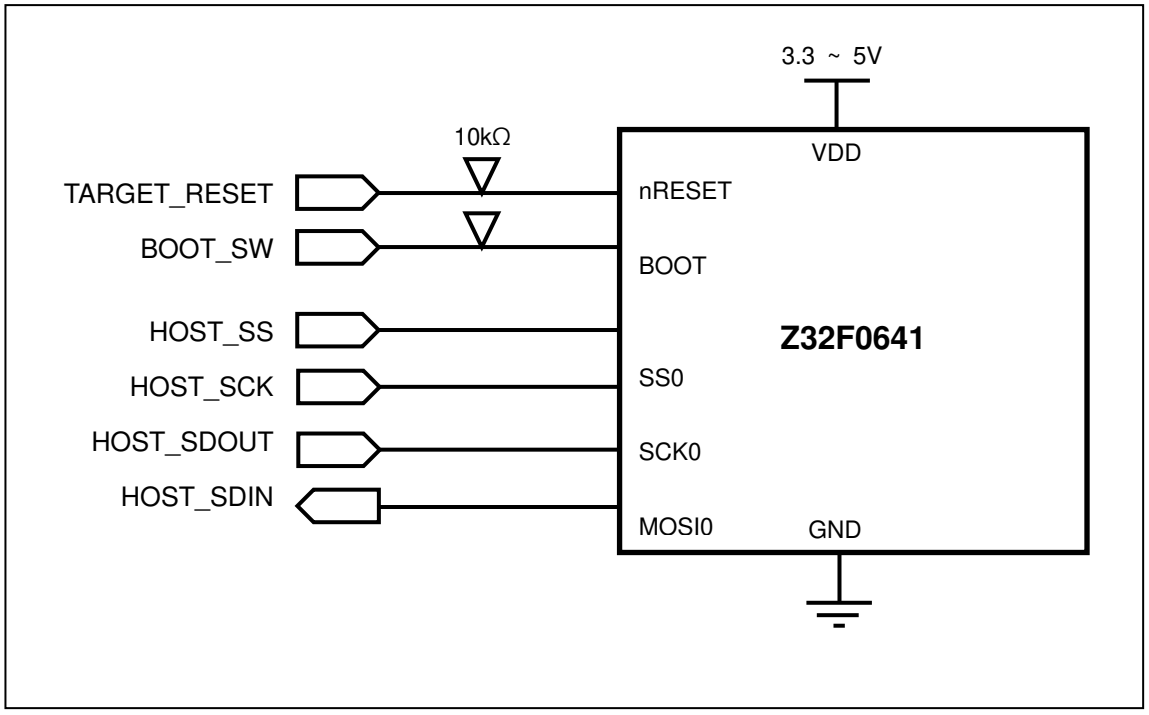


**Figure 3.2 SPI Boot Connection Diagram**

# 4. System Control Unit

## Overview

The Z32F0641 microcontroller has an in-built intelligent power control block which manages the system analog blocks and operating modes. Internal reset and clock signals are controlled by the SCU block to maintain optimal system performance and power dissipation.

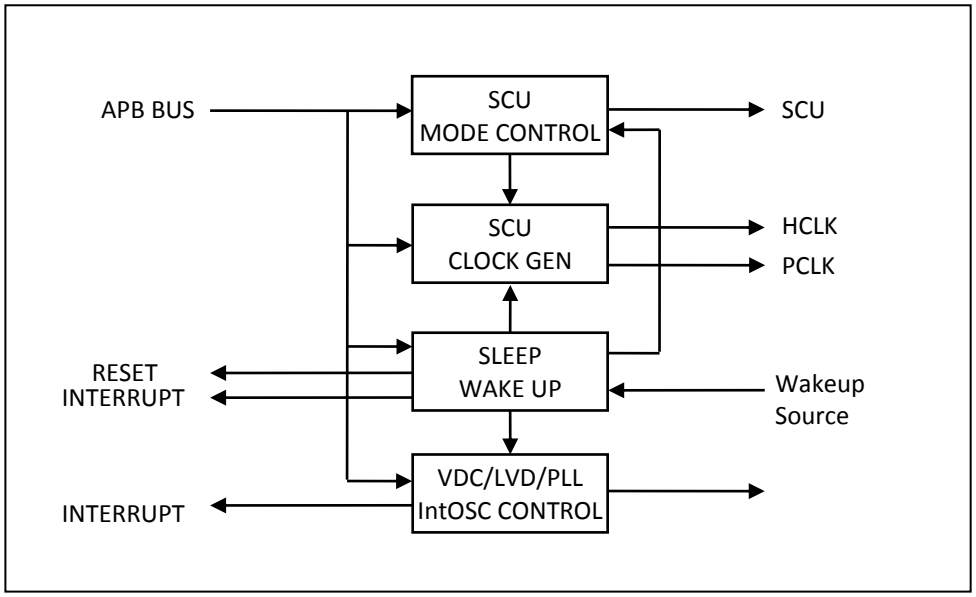


**Figure 4.1 SCU Block Diagram**

## Clock System

The Z32F0641 MCU has the following two main operating clocks:

HCLK – Clock for the CPU and AHB bus system
PCLK – Clock for peripheral systems

Figure 4.2 and Figure 4.3 show the chip's clock system. Table 4.1 lists the clock source descriptions.

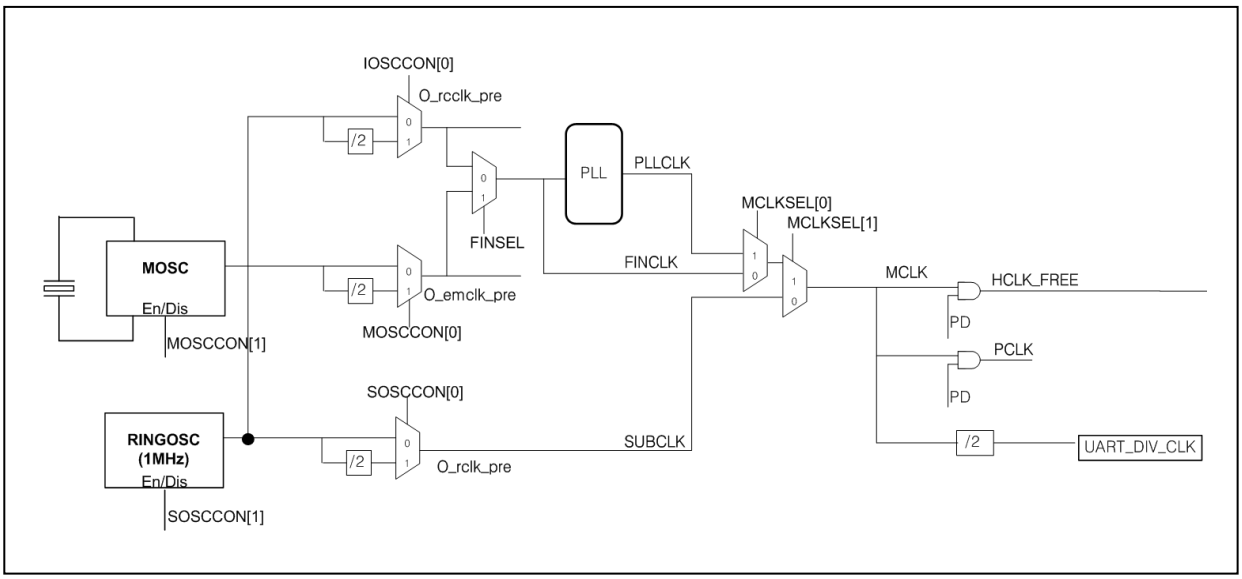


**Figure 4.2 Clock Source Configuration**

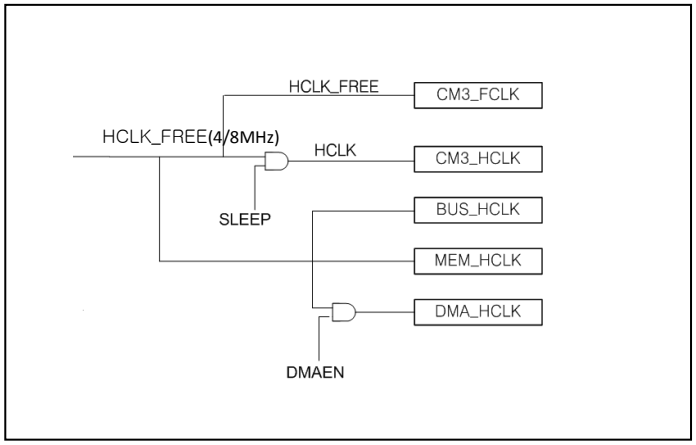


**Figure 4.3 System Clock Configuration**

Each of the multiplexers for switching the clock source contains a circuit which allows glitch-free switching between clock modes.

**Table 4.1 Clock Sources**

| Clock name | Frequency | Description |
|---|---|---|
| MainOSC | XTAL(4MHz~8MHz) | External Crystal IOSC |
| PLL Clock | 8MHz ~ 80MHz | On Chip PLL |
| ROSC | 1MHz | Internal RING OSC |

The PLL can synthesize the PLLCLK clock up to 80 MHz with the FIN reference clock. It also has an internal pre-divider and post-divider.

## HCLK Clock Domain

The HCLK clock feeds the clock to the CPU and AHB bus. The Cortex-M3 CPU requires two clocks related with the HCLK clock:

FCLK – FCLK is a free-running clock which runs continuously except during Power-Down Mode
HCLK – HCLK can be stopped during Idle Mode

## Miscellaneous Clock Domain for Cortex-M3

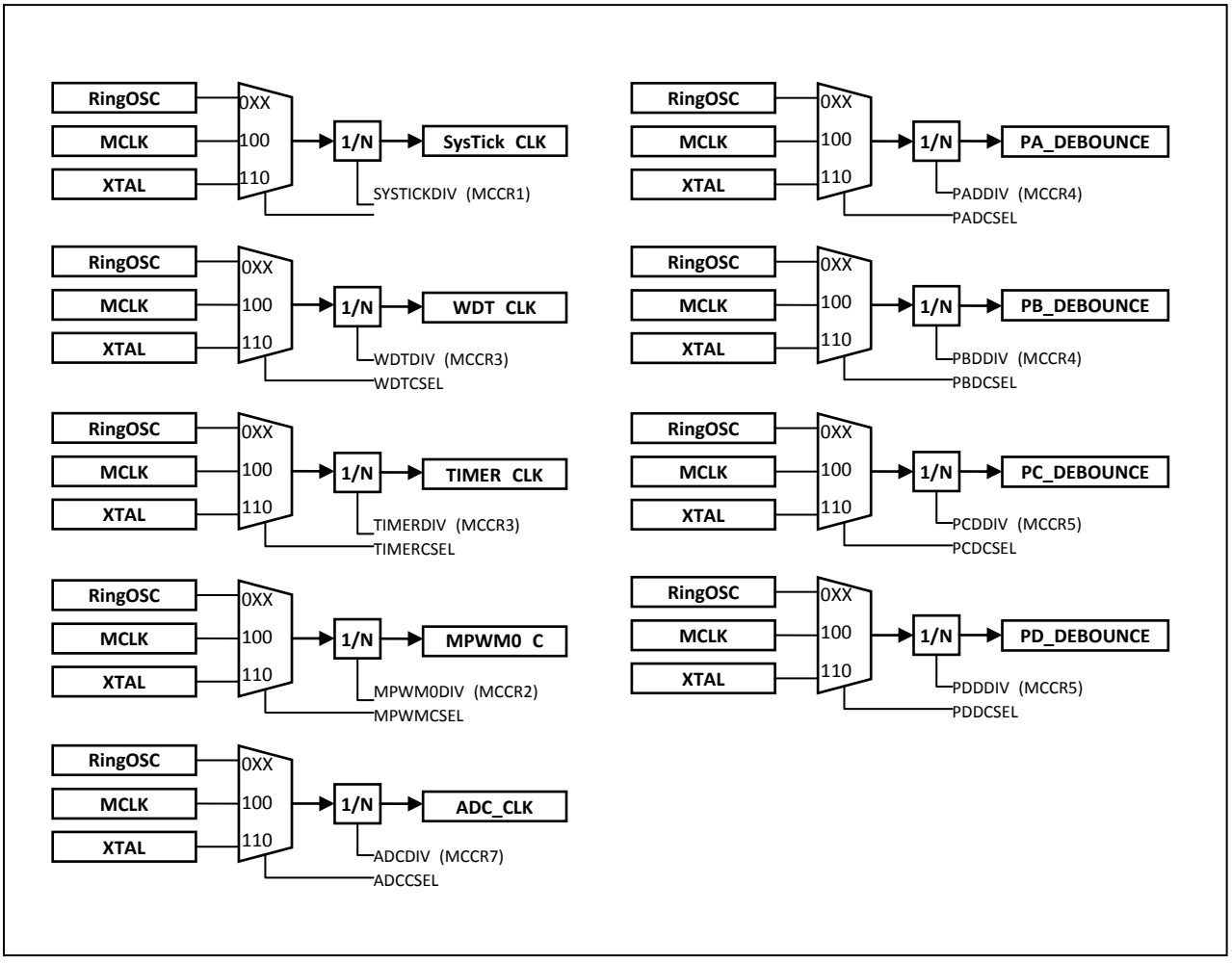


**Figure 4.4 Miscellaneous Clock Configuration**

## PCLK Clock Domain

PCLK is the master clock of all the peripherals. It can be stopped in Power-Down Mode. Each peripheral clock is generated by the PCER register set.

## Clock Configuration

After power up, the default system clock is fed by the RINGOSC (1 MHz) clock. RINGOSC is enabled by default at power up. The other clock sources are enabled by user controls with the RINGOSC system clock.

The MOSC clock can be enabled by the CSCR register. Before enabling the MOSC block, the pin mux configuration should be set for XIN, XOUT function. PC12 and PC13 pins are shared with MOSC's XIN and XOUT function - PCCMR and PCCCR registers should be correctly configured. After enabling the MOSC block, you must wait for more than 1 msec to ensure stable operation of crystal oscillation.

The PLL clock can be enabled by the PLLCON register. After enabling the PLL block, you must wait for the PLL lock flag. When the PLL output clock is stable; you can select MCLK for your system requirement. Before changing the system clock, Flash access wait should be set to the maximum value. After the system clock is changed, you will need to set the desired Flash access wait time.

An example flow chart outlining the steps to configure the system clock is shown in Figure 4.5.

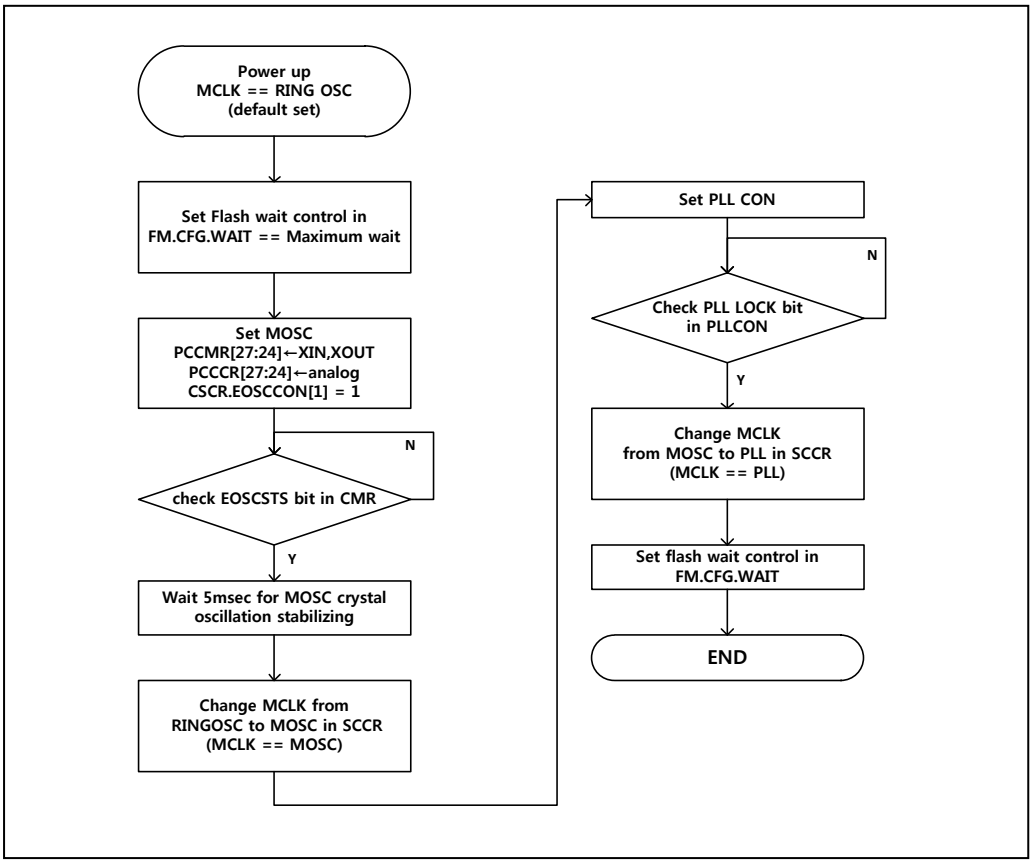


**Figure 4.5. Clock Configuration Flow Chart**

When you speed up the system clock up to maximum operating frequency, you should check the Flash wait control configuration. Flash read access time is one of the limiting factors in performance. The wait control recommendation is provided in Table 4.2.

**Table 4.2. Flash Wait Control Recommendation**

| FM.CFG.WAIT | FLASH Access Wait | Available Max System Clock Frequency |
|---|---|---|
| 000 | 0 clock wait | ~16MHz |
| 001 | 1 clock wait | ~32MHz |
| 010 | 2 clock wait | ~48MHz |
| 011 | 3 clock wait | ~48MHz |

# Reset

The Z32F0641 MCU has two system resets:

- Cold reset by POR, which is effective during power up or down sequence, and
- Warm reset, which is generated by several reset sources. The reset event causes the chip to return to initial state.

The cold reset has only one reset source, POR. The warm reset has the following reset sources:

- nRESET pin
- WDT reset
- LVD reset
- MCLK Fail reset
- MOSC Fail reset
- S/W reset
- CPU request reset

## Cold Reset

Cold reset is an important feature of the chip when power is up. This characteristic globally affects the system boot. Internal VDC is enabled when VDD power is turned on. The internal VDD level slope is followed by the external VDD power slope. The internal PoR trigger level is 1.4 V of internal VDC voltage out level. At this time, boot operation is started. The RINGOSC clock is enabled and counts to 4 msec for internal VDC level stabilizing. During this time, the external VDD voltage level should be greater than the initial LVD level (2.3 V). After counting 4 msec, the CPU reset is released and the operation is started.

Figure 4.6 shows the power up sequence and internal reset waveform.