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Embedded in Life

An IXYS Company

ZNEO32! Family of Microcontrollers

Z32F1281 MCU

Product Specification

PS034504-0617

PRELIMINARY

ZNEO32!

32 Bit Microcontrollers

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Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Description	Page
Jun 2017	04	Updated part numbers to include the Cortex M identifier.	All
May 2016	03	Added Quadrature Encoder Interface information.	122
Apr 2016	02	Added timing information for peripherals; global edits for clarity.	All
Nov 2015	01	Original issue.	

1. Overview

Introduction

Zilog's Z32F1281 MCU, a member of the ZNEO32! Family of microcontrollers is a cost-effective and high-performance 32-bit microcontroller. The Z32F1281 MCU provides 3-phase PWM generator units which are suitable for inverter bridges, including motor drive systems. The two built-in channels of these generators control two inverter motors simultaneously.

Three 12-bit high speed ADC units with 16-channel analog multiplexed inputs are included to gather information from the motor. The Z32F1281 MCU can control up to two inverter motors or one inverter motor and the Power Factor Correction (PFC) function simultaneously. Four on-chip operational AMPs and four analog comparators are available to measure analog input signals. The operational amplifier can amplify the input signal to the proper signal range and transfer it to the ADC input channel. The comparator monitors external signals and helps create an internal emergency signal. Multiple powerful external serial interface engines communicate with on-board sensors.

Figure 1.1 shows a block diagram of the Z32F1281 MCU.

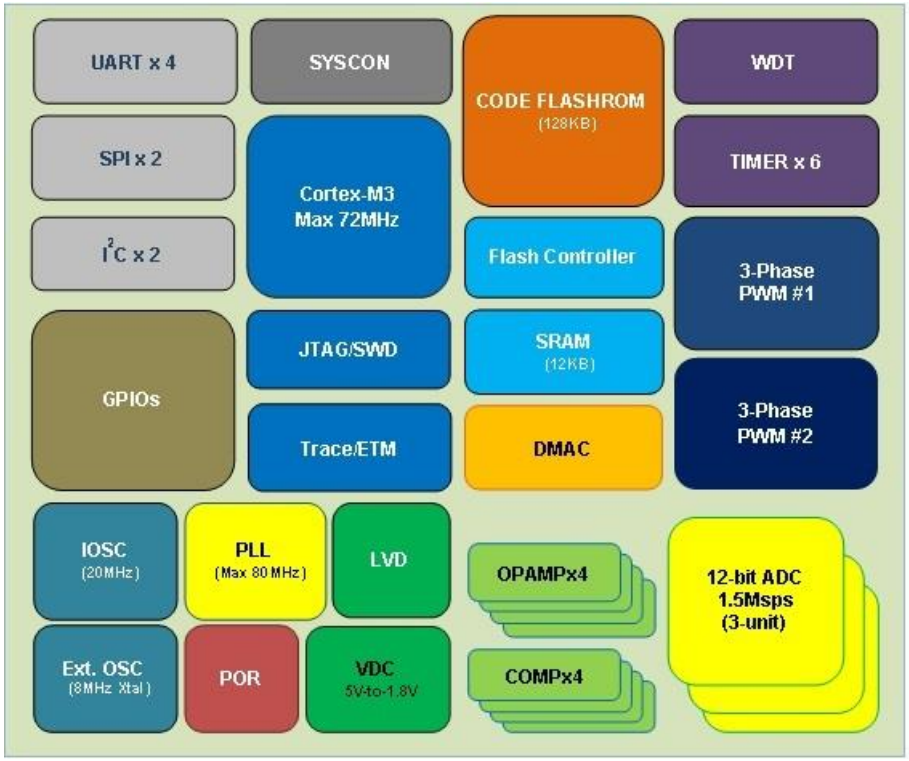

Figure 1.1. Z32F1281 MCU Block Diagram

Figure 1.2 and Figure 1.3 show the pin layouts.

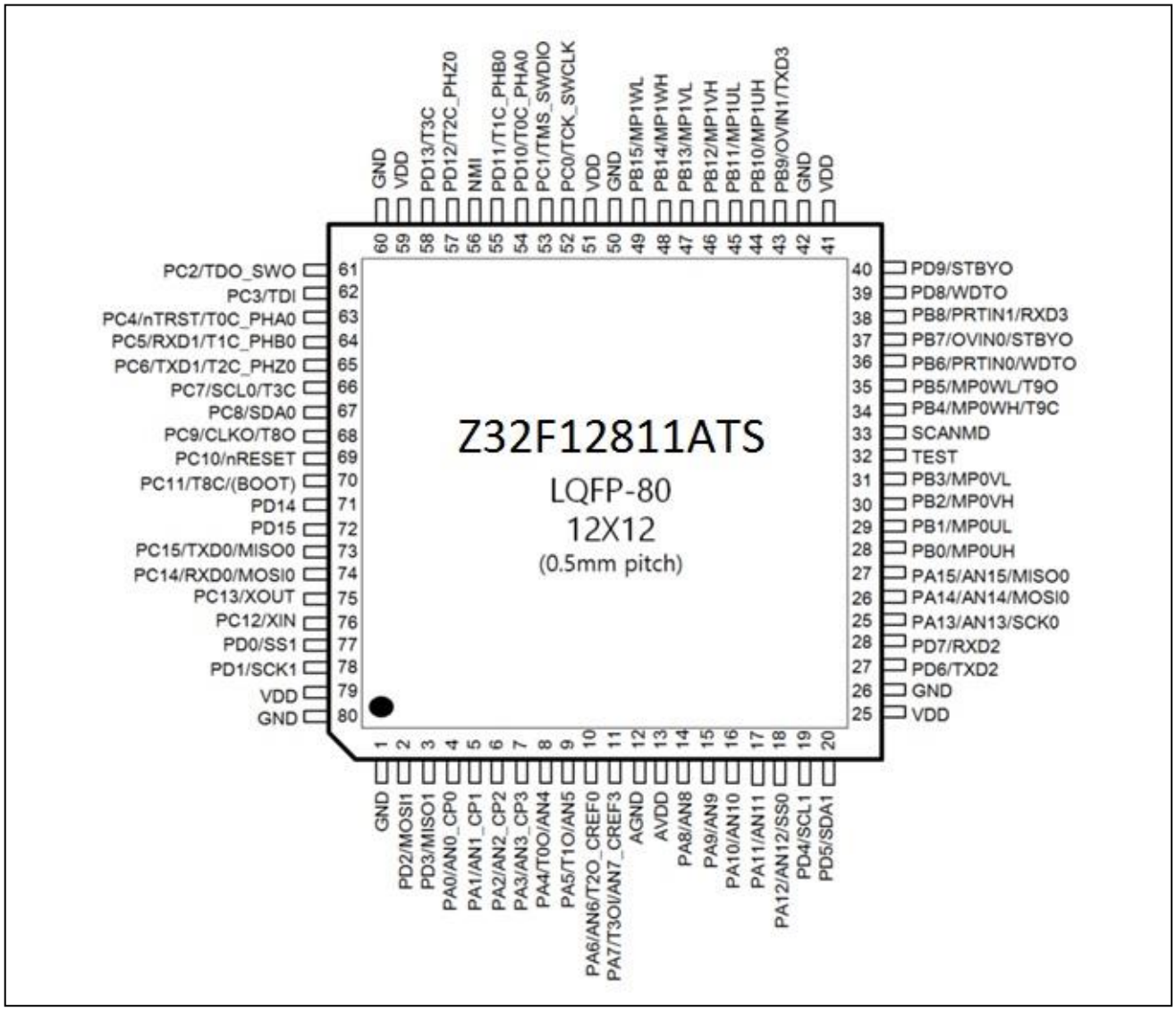

Figure 1.2. Pin Layout (LQFP-80)

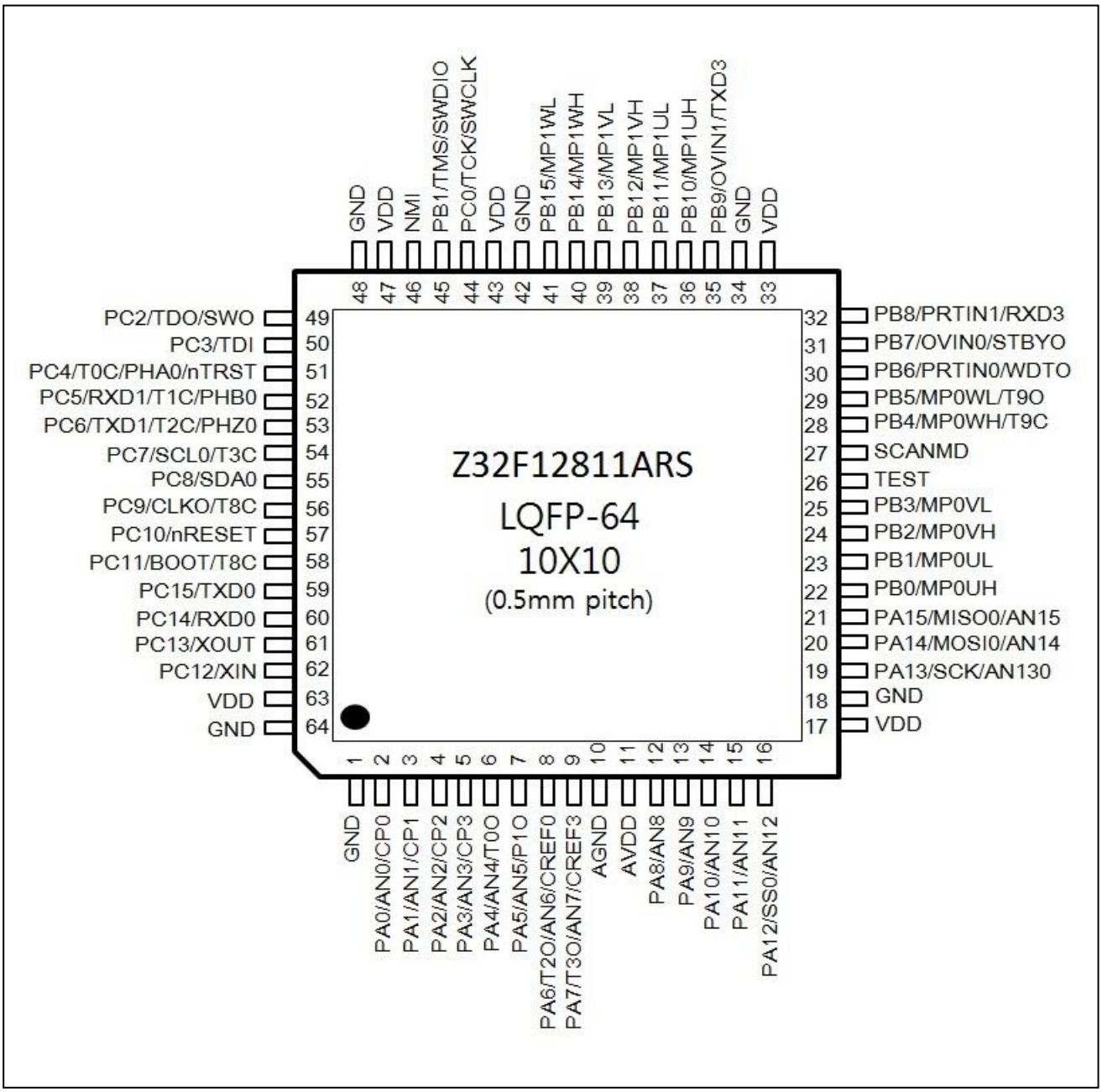

Figure 1.3. Pin Layout (LQFP-64)

Product Features

The Z32F1281 MCU offers the following features:

- High performance low-power Cortex-M3 core
- 128 KB code Flash memory with cache function
- 12 KB SRAM
- 3-Phase Motor PWM with ADC triggering function
  - 2 channels
- 1.5Msps high-speed ADC with burst conversion function
  - 2 or 3 units with 16 channel input
- Built-in Programmable Gain Amplifier (PGA) for ADC inputs
  - 4 channels
    - 3 channels for 3 shunt resistor configuration
    - 1 channel for 1 shunt resistor configuration
- Built-in analog comparator
  - 4 channels
    - 3 channels for 3 shunt resistor configuration
    - 1 channel for 1 shunt resistor configuration
- System fail-safe function by clock monitoring
- XTAL OSC fail monitoring
- Precision internal oscillator clock (20MHz ±3%)
- Watchdog timer
- Six general purpose timers
- Quadrature encoder interface counter
- External communication ports: 4 UARTs, 2 I^2Cs, 2 SPIs
- High current driving port for UART photo couplers
- Debug and emergency stop function
- Real-time monitoring function support for more effective development
- JTAG and Serial Wire Debug (SWD) in-circuit debugger
- Various memory size and package options
  - LQFP-80, LQFP-64
- Industrial grade operating temperature (-40 ~ +85℃)

Table 1.1. Device Type

Part Number	Flash	SRAM	UART	SPI	I2C	MPWM	ADC	I/O PORT	PKG
Z32F12811ATS	128KB	12KB	4	2	2	2	3-unit 16 ch	68	LQFP-80
Z32F12811ARS			2	2	1	2		48	LQFP-64

Architecture

Block Diagram

An internal block diagram of the Z32F1281 MCU is shown in Figure 1.4.

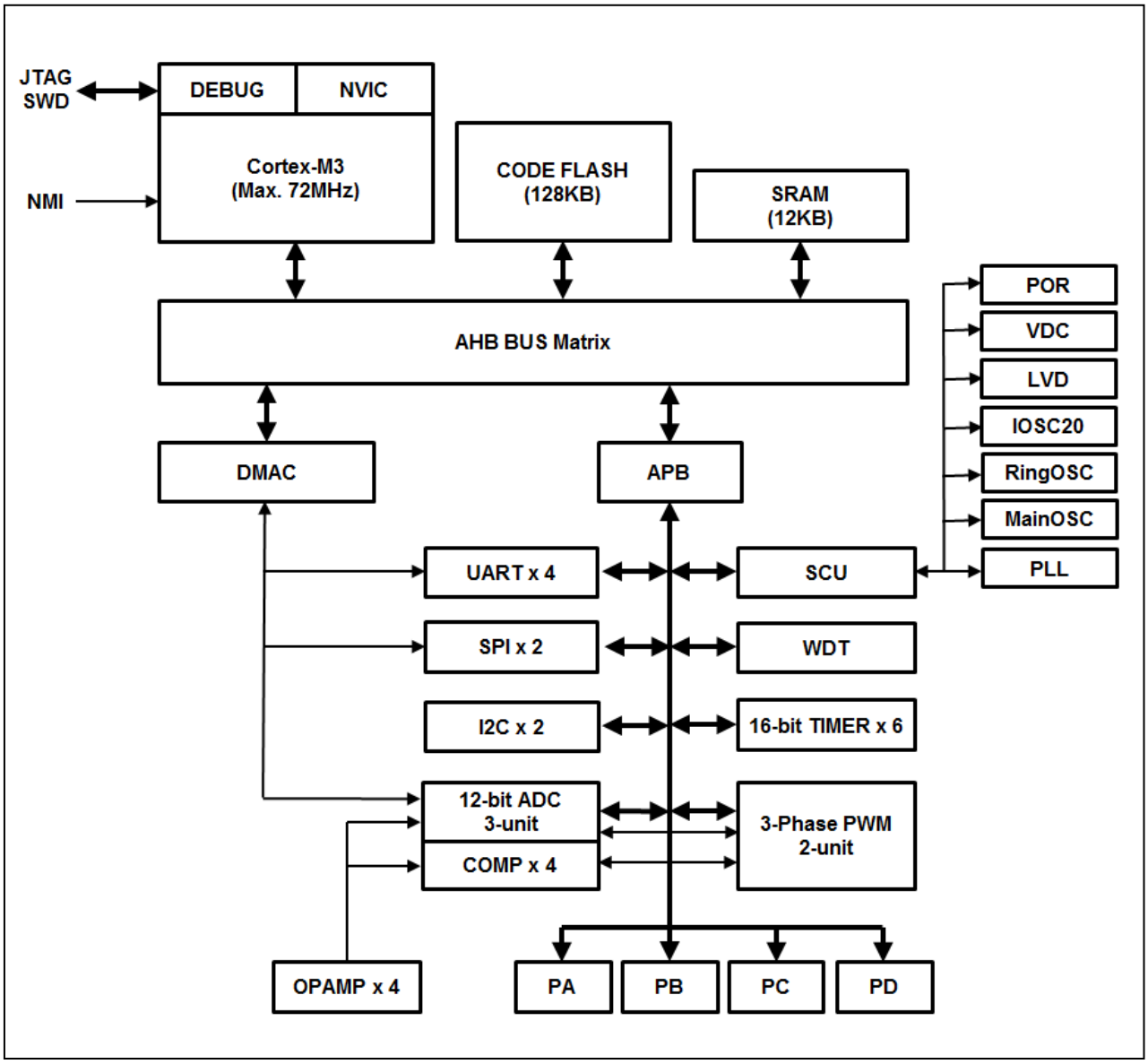

Figure 1.4. Internal Block Diagram

Functional Description

The following section provides an overview of the features of the Z32F1281 microcontroller.

ARM Cortex-M3

- ARM powered Cortex-M3 Core based on v7M architecture, which is optimized for small size and low-power systems. On core system timer (SYSTICK) provides a simple 24-bit timer that makes it easy to manage the system operations
- Thumb-compatible Thumb-2 only instruction set processor core makes code high-density
- Hardware division and single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling
- Full featured debug solutions – JTAG and SWD, FPB, DWT, ITM, and TPIU
- Maximum 72 MHz operating frequency with zero wait execution

Nested Vector-Interrupt Controller (NVIC)

- The ARM Nested Vectored Interrupt Controller (NVIC) on the ARM Cortex-M3 core handles all internal and external exceptions. When an interrupt condition is detected, the processor state is automatically stored to the stack and automatically restored from the stack at the end of the interrupt service routine.
- The vector is fetched in parallel to the state saving, which enables efficient interrupt entry.
- The processor supports tail-chaining, which enables back-to-back interrupts to be performed without the overhead of state saving and restoring.

128 KB Internal Code Flash Memory

- The Z32F1281 MCU provides internal 128 KB code Flash memory and its controller. This is enough to program the motor algorithm and control the system. Self-programming is available and ISP and JTAG programming is also supported in Boot or Debugging Mode.
- Instruction and data cache buffer overcome the limitations of low-bandwidth Flash memory. The CPU can execute from Flash memory with zero wait state up to 72 MHz bus frequency.

12 KB Zero-wait Internal SRAM

- On chip 12 KB zero-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

Boot Logic

- The smart boot logic supports Flash programming. The Z32F1281 MCU can be entered by external boot pin and UART and SPI programming are available in Boot Mode. UART0 or SPI0 is used in Boot mode communication.

System Control Unit (SCU)

- The SCU block manages internal power, clock, reset and operation mode. It also controls analog blocks (INTOSC, VDC and LVD).

32-bit Watchdog Timer (WDT)

- The watchdog timer performs the system monitoring function. It generates an internal reset or interrupt to notice an abnormal status of the system.

Multi-purpose 16-bit Timer

- Six-channel 16-bit general purpose timers support:
  - Periodic timer mode
  - Counter mode
  - PWM mode
  - Capture mode

PWM Generator

- Two channels of the 3-phase PWM generator are implemented. 16 bit up/down counter with prescaler supports triangular and saw tooth waveforms.
- The PWM generates an internal ADC trigger signal to measure the signal on time.
- Dead time insertion and emergency stop functionality ensure that the chip and system operate under safe conditions.

Serial Peripheral Interface (SPI)

- Synchronous serial communication is provided by the SPI block. The Z32F1281 MCU has 2 channel SPI modules. The DMA function is supported by the DMA controller. Transfer data is moved to/from the memory area without CPU operation.
- Boot mode uses this SPI block to download the Flash program.

Inter-Integrated Circuit Interface (I^2C)

- The Z32F1281 MCU has a 2-channel I^2C block and it supports up to 400 kHz I^2C communication. Master and the slave modes are supported.

Universal Asynchronous Receiver/Transmitter (UART)

- The Z32F1281 MCU includes a 4-channel UART block. For accurate baud rate control, a fractional baud rate generator is provided.
- The DMA function is supported by the DMA controller. Transfer data is moved to/from memory area without CPU operation.

General PORT I/Os

- 16-bit PA, PB, PC, PD ports are available and provide multiple functionality:
- General I/O port
- Independent bit set/clear function
- External interrupt input port
- Pull-up/Open-drain
- On chip debounce Filter

12-bit Analog-to-Digital Converter (ADC)

- 3 built-in ADCs can convert analog signal up to 1usec conversion rate. 16-channel analog mux and OP-AMP provides various combinations from external analog signals.

Analog Front End (AFE)

- Operational Amplifier (OPAMP)
  - 4 built-in OPAMPs amplify analog signals up to x8.74 gain
- Analog Comparator (COMP)
  - 4 built-in analog comparators

Pin Description

The pin configurations are shown in Table 1.2. 16 pins are reserved for power/ground pair and dedicated pins.

Table 1.2. Pin Description

Pin Name		Type	Description		Remark
LQFP80	LQFP64				
79	63	VDD	P	VDD	
80	64	GND	P	Ground	
1	1	GND	P	Ground	
2	-	PD2	IOUS	PORT D Bit 2 Input/Output	
		MOSI1	I/O	SPI Channel 1 Master Out / Slave In	
3	-	PD3*	IOUS	PORT D Bit 3 Input/Output	
		MISOI1	I/O	SPI Channel 1 Master In / Slave Out	
4	2	PA0*	IOUS	PORT A Bit 0 Input/Output	
		AN0	IA	Analog Input 0	
		COMP0	IA	Comparator 0 Input	
5	3	PA1*	IOUS	PORT A Bit 1 Input/Output	
		AN1	IA	Analog Input1	
		COMP1	IA	Comparator 1 Input	
6	4	PA2*	IOUS	PORT A Bit 2 Input/Output	
		AN2	IA	Analog Input 2	
		COMP2	IA	Comparator 2 Input	
7	5	PA3*	IOUS	PORT A Bit 3 Input/Output	
		AN3	IA	Analog Input 3	
		COMP3	IA	Comparator 3 Input	
8	6	PA4*	IOUS	PORT A Bit 4 Input/Output	
		T0O	Output	Timer 0 Output	
		AN4	IA	Analog Input 4	
9	7	PA5*	IOUS	PORT A Bit 5 Input/Output	
		T1O	Output	Timer 1 Output	
		AN5	IA	Analog Input 5	
10	8	PA6*	IOUS	PORT A Bit 6 Input/Output	
		T2O	Output	Timer 2 Output	
		AN6	IA	Analog Input 6	
		CREF0	IA	Comparator 0 Reference Input	
11	9	PA7*	IOUS	PORT A Bit 7 Input/Output	
		TRACED3	Output	ETM Trace Data 3	
		T3O	Output	Timer 3 Output	
		AN7	IA	Analog Input 7	
		CREF1	IA	Comparator 1 Reference Input	
12	10	AGND	P	Analog Ground	
13	11	AVDD	P	Analog VDD	
14	12	PA8*	IOUS	PORT A Bit 8 Input/Output	
		TRACECLK	Output	ETM Trace Clock	
		AD0O	Output	ADC0 Start Signal	
		AN8	IA	Analog Input 8	
15	13	PA9*	IOUS	PORT A Bit 9 Input/Output	
		TRACED0	Output	ETM Trace Data 0	
		AD1O	Output	ADC1 Start Signal	
		AN9	IA	Analog Input 9	
16	14	PA10*	IOUS	PORT A Bit 10 Input/Output	
		TRACED1	Output	ETM Trace Data 1	
		AD2O	Output	ADC2 Start Signal	
		AN10	IA	Analog Input 10	
17	15	PA11*	IOUS	PORT A Bit 11 Input/Output	
		TRACED2	Output	ETM Trace Data 2	

		AN11	IA	Analog Input 11	
18	16	PA12*	IOUS	PORT A Bit 12 Input/Output	
		SS0	I/O	SPI0 Slave Select signal	
		AD2I	Input	ADC2 Start Input signal	
		AN12	IA	Analog Input 12	
19	-	PD4	IOUS	PORT D Bit 4 Input/Output	
		SCL1	Output	I^2C Channel 1 SCL In/Out	
20	-	PD5	IOUS	PORT D Bit 5 Input/Output	
		SDA1	Output	I^2C Channel 1 SDA In/Out	
21	17	VDD	P	VDD	
22	18	GND	P	Ground	
23	-	PD6*	IOUS	PORT D Bit 6 Input/Output	
		TXD2	Output	UART Channel 2 TxD Input	
		AD0I	Input	ADC0 Start Input signal	
24	-	PD7*	IOUS	PORT D Bit 7 Input/Output	
		RXD2	Input	UART Channel 2 RxD Input	
		AD1I	Input	ADC1 Start Input signal	
25	19	PA13*	IOUS	PORT A Bit 13 Input/Output	
		SCK0	I/O	SPI0 Data Clock Input/Output	
		AN13	IA	Analog Input 13	
26	20	PA14*	IOUS	PORT A Bit 14 Input/Output	
		MOSI0	I/O	SPI0 Master-Output/Slave-Input Data signal	
		AN14	IA	Analog Input 14	
27	21	PA15*	IOUS	PORT A Bit 15 Input/Output	
		MISO0	I/O	SPI0 Master-Input/Slave-Output Data signal	
		AN15	IA	Analog Input 15	
28	22	PB0	IOUS	PORT B Bit 0 Input/Output	
		PWM0H0	Output	PWM0 H0 Output	
29	23	PB1	IOUS	PORT B Bit 1 Input/Output	
		PWM0L0	Output	PWM0 L0 Output	
30	24	PB2	IOUS	PORT B Bit 0 Input/Output	
		PWM0H1	Output	PWM0 H1 Output	
31	25	PB3	IOUS	PORT B Bit 1 Input/Output	
		PWM0L1	Output	PWM0 L1 Output	
32	26	TEST	Input	Test-mode Input (Always tied ‘L’)	Pull-down
33	27	SCANMD	Input	Scan-mode Input (Always tied ‘L’)	Pull-down
34	28	PB4	IOUS	PORT B Bit 4 Input/Output	
		PWM0H2	Output	PWM0 H2 Output	
		T9C	I/O	Timer 9 Clock/Capture Input	
35	29	PB5	IOUS	PORT B Bit 5 Input/Output	
		PWM0L2	Output	PWM0 L2 Output	
		T9O	I/O	Timer 9 Output	
36	30	PB6	IOUS	PORT B Bit 6 Input/Output	
		PRTIN0	Input	PWM0 Protection Input signal 0	
		WDTO	Output	WDT Output	
37	31	PB7	IOUS	PORT B Bit 7 Input/Output	
		OVIN0	Input	PWM0 Over-voltage put signal 1	
		STBYO	Output	Power-down mode indication signal	
38	32	PB8	IOUS	PORT B Bit 8 Input/Output	
		PRTIN1	Input	PWM1 Protection Input signal 0	
		RXD3	Input	UART3 RXD Input	

39	-	PD8	IOUS	PORT D Bit 8 Input/Output	
		WDTO	Output	WDT Output	
30	-	PD9	IOUS	PORT D Bit 9 Input/Output	
		STBYO	Output	Power-down mode indication signal	
41	33	VDD	P	VDD	
42	34	GND	P	Ground	
43	35	PB9	IOUS	PORT B Bit 9 Input/Output	
		OVIN1	Input	PWM1 Over-voltage Input signal 1	
		TXD3	Output	UART3 TXD Output	
44	36	PB10	IOUS	PORT B Bit 10 Input/Output	
		PWM1H0	Output	PWM Channel 1 Phase 0 H-side Output	
45	37	PB11	IOUS	PORT B Bit 11 Input/Output	
		PWM1L0	Output	PWM Channel 1 Phase 0 L-side Output	
46	38	PB12	IOUS	PORT B Bit 12 Input/Output	
		PWM1H1	Output	PWM Channel 1 Phase 1 H-side Output	
47	39	PB13	IOUS	PORT B Bit 13 Input/Output	
		PWM1L1	Output	PWM Channel 1 Phase 1 L-side Output	
48	40	PB14	IOUS	PORT B Bit 14 Input/Output	
		PWM1H2	Output	PWM Channel 1 Phase 2 H-side Output	
49	41	PB15	IOUS	PORT B Bit 15 Input/Output	
		PWM1L2	Output	PWM Channel 1 Phase 2 L-side Output	
50	42	GND	P	Ground	
51	43	VDD	P	VDD	
52	44	PC0	IOUS	PORT C Bit 0 Input/Output	
		TCK/SWCK	Input	JTAG TCK, SWD Clock Input	
53	45	PC1	IOUS	PORT C Bit 1 Input/Output	
		TMS/SWDIO	I/O	JTAG TMS, SWD Data Input/Output	
54	-	PD10	IOUS	PORT D Bit 10 Input/Output	
		AD0SOC	Output	ADC0 Start-of-Conversion	
		T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
55	-	PD11	IOUS	PORT D Bit 10 Input/Output	
		AD0EOC	Output	ADC0 End-of-Conversion	
		T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
56	46	NMI	Input	Non-maskable Interrupt Input	
57	-	PD12	IOUS	PORT D Bit 12 Input/Output	
		AD1SOC	Output	ADC1 Start-of-Conversion	
		T2C/PHZ0	Input	Timer 2 Clock/Capture/Phase-Z Input	
58	-	PD13	IOUS	PORT D Bit 13 Input/Output	
		AD1EOC	Output	ADC1 End-of-Conversion	
		T3C	Input	Timer 3 Clock/Capture Input	
59	47	VDD	P	VDD	
60	48	GND	P	Ground	
61	49	PC2	IOUS	PORT C Bit 2 Input/Output	
		TDO/SWO	Output	JTAG TDO, SWO Output	
62	50	PC3	IOUS	PORT C Bit 3 Input/Output	
		TDI	Input	JTAG TDI Input	
63	51	PC4	IOUS	PORT C Bit 4Input/Output	
		nTRST	Input	JTAG nTRST Input	
		T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
64	52	PC5	IOUS	PORT C Bit 5Input/Output	
		RXD1	Input	UART1 RXD Input	
		T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
65	53	PC6	IOUS	PORT C Bit 6Input/Output	

		TXD1	Output	UART1 TXD Output	
		T2C/PHZ	Input	Timer 2 Clock/Capture/Phase-Z Input	
66	54	PC7	IOUS	PORT C Bit 7Input/Output	
		SCL0	Output	I^2C Channel 0 SCL In/Out	
		T3C	Input	Timer 3 Clock/Capture input	
67	55	PC8	IOUS	PORT C Bit 8 Input/Output	
		SDA0	Output	I^2C Channel 0 SDA In/Out	
68	56	PC9	IOUS	PORT C Bit 9 Input/Output	
		CLKO	Output	System Clock Output	
		T8O	Output	Timer 8 Output	
69	57	PC10	IOUS	PORT C Bit 10 Input/Output	
		nRESET	Input	External Reset Input	Pull-up
70	58	PC11	IOUS	PORT C Bit 11 Input/Output	
		BOOT	Input	Boot mode Selection Input	
		T8C	Input	Timer 8 Clock/Capture Input	
71	-	PD14	IOUS	PORT D Bit 14 Input/Output	
		AD2SOC	Output	ADC2 Start-of-Conversion Output signal	
72	-	TD15	IOUS	PORT D Bit 15 Input/Output	
		AD2EOC	Output	ADC2 Start-of-Conversion Output signal	
73	59	PC15	IOUS	PORT C Bit 14 Input/Output	
		TXD0	Output	UART0 TXD Output	
		MISO0	I/O	SPI0 Master-Input/Slave-Output	
74	60	PC14	IOUS	PORT C Bit 14 Input/Output	
		RXD0	Input	UART0 RXD Input	
		MOSI0	I/O	SPI0 Master-Output/Slave-Input	
		VMARGIN	OA	Not used. (test purpose)	
75	61	PC13	IOUS	PORT C Bit 13 Input/Output	
		XOUT	OA	External Crystal Oscillator Output	
76	62	PC12	IOUS	PORT C Bit 12 Input/Output	
		XIN	IA	External Crystal Oscillator Input	
77	-	PD0	IOUS	PORT D Bit 0 Input/Output	
		SS1	I/O	SPI1 Slave Select	
78	-	PD1	IOUS	PORT D Bit 1 Input/Output	
		SCK1	I/O	SPI1 Clock Input/Output	

*Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

Memory Map

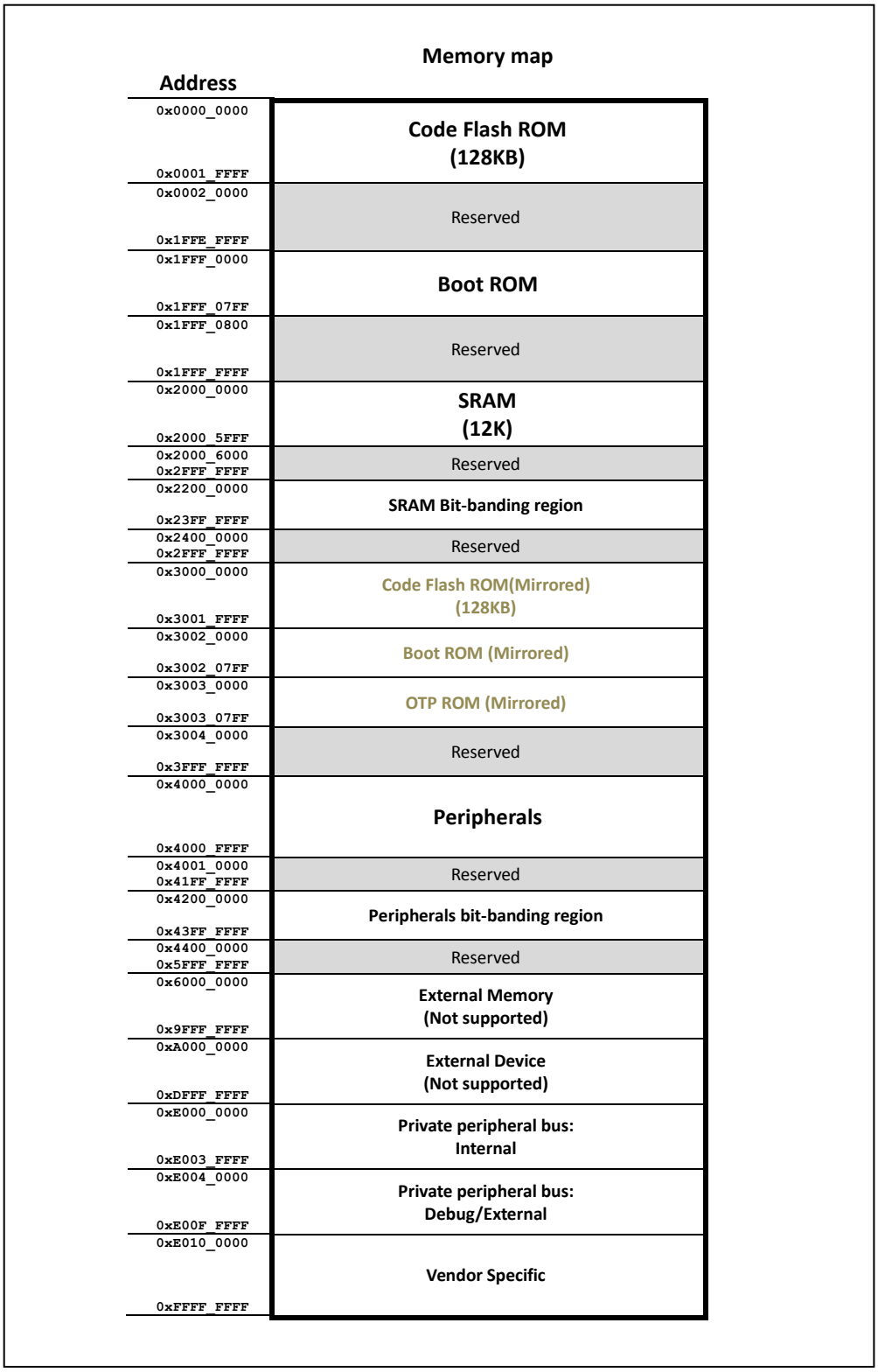

Figure 1.5. Main Memory Map

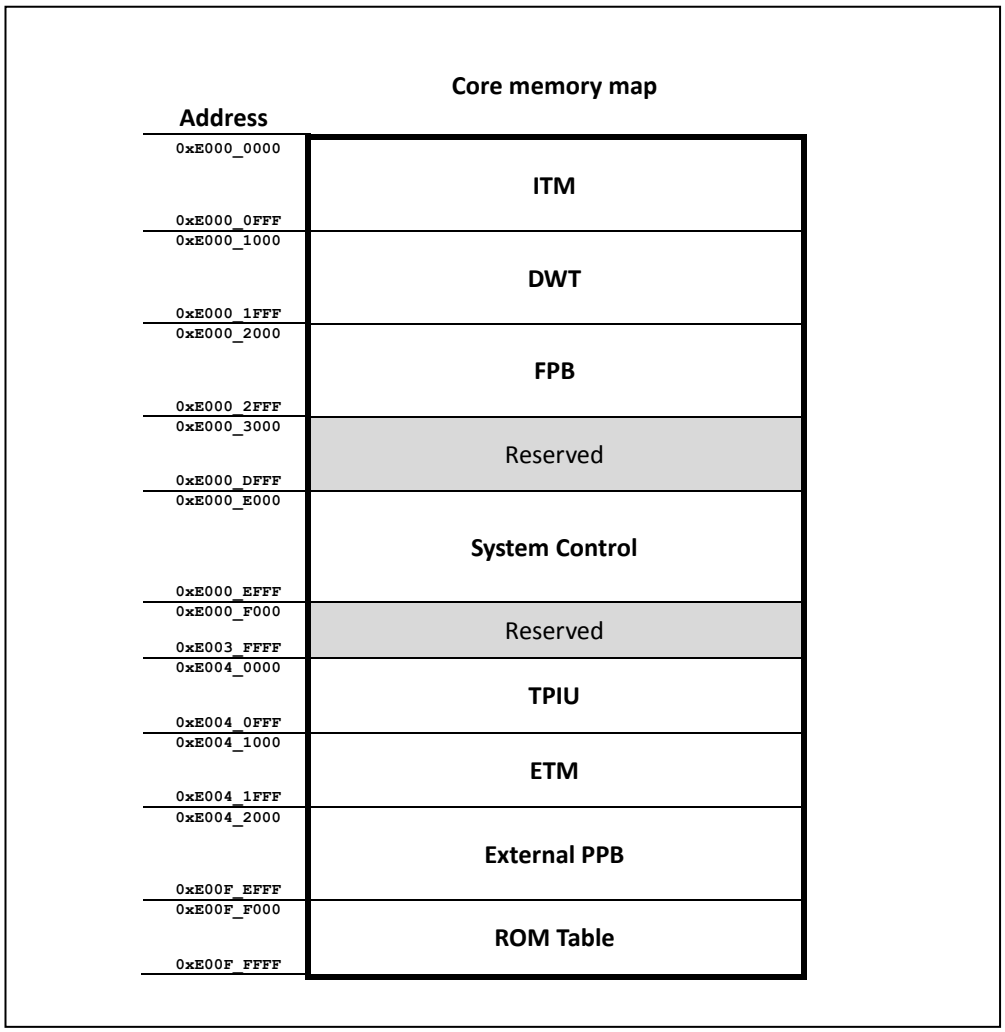

Figure 1.6. Cortex-M3 Private Memory Map

Note: For more information about the memory maps, refer to document number DDI337 from ARM.

Address	Peripheral map
0x4000_0000	SCU
0x4000_0100	FMC
0x4000_0200	WDT
0x4000_0300	Reserved
0x4000_0400	DMAC(15)
0x4000_0500	Reserved
0x4000_1000	PCU
0x4000_2000	GPIO(A,B,C,D)
0x4000_3000	TIMER(6)
0x4000_4000	MPWM0
0x4000_5000	MPWM1
0x4000_6000	Reserved
0x4000_8000	UART0
0x4000_8100	UART1
0x4000_8200	UART2
0x4000_8300	UART3
0x4000_8600	Reserved
0x4000_9000	SPI0
0x4000_9100	SPI1
0x4000_9200	Reserved
0x4000_A000	I^2C0
0x4000_A100	I^2C1
0x4000_A200	Reserved
0z4000_B000	ADC0
0x4000_B100	ADC1
0x4000_B200	ADC2
0x4000_B300	AFE
0x4000_B400 0x4000_FFFF	Reserved

Figure 1.7. Peripheral Memory Map

2. CPU

Cortex-M3 Core

The CPU core is supported by the ARM Cortex-M3 processor which provides a high-performance, low-cost platform. For more information about Cortex-M3, refer to document number DDI337 from ARM.

System Timer

The System Timer (SYSTICK) is a 24-bit timer and is part of the Cortex-M3 core. The system timer can be configured either through the registers (see the Cortex-M3 Technical Reference Manual) or through the provided functions defined in `core_cm3.h`. There is an interrupt vector for the system timer. To configure the system timer, call `SysTickConfig()` with the number of system clocks in between interrupt intervals (up to a maximum of 24 bits).

Interrupt Controller

The Nested Vectored Interrupt Controller (NVIC) is part of the core Cortex-M3 MCU. The NVIC controls system exceptions and peripheral interrupts and is closely coupled with the core to provide low latency and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the nested interrupts to enable tail-chaining of interrupts.

The Z32F1281 MCU supports 64 peripheral interrupts (of which 25 are not used) and 16 system interrupts. The NVIC also allows setting software interrupts and resetting the system.

Interrupts can be assigned a PRIORITY GROUP (common interrupts with the same priorities) as well as individual priorities. There are 8 priority levels available. For an interrupt to be active, it must be enabled in the peripheral and the NVIC registers. For more information on NVIC, see the Cortex M3 Technical Reference Manual.

The system includes functions to set the NVIC registers which are defined in `core_cm3.h`.

Table2.1. Interrupt Vector Map

Interrupt Number	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MPU Fault Handler
-11	0x0000_0014	BUS Fault Handler
-10	0x0000_0018	Usage Fault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVDDETECT
1	0x0000_0044	SCLKFAIL
2	0x0000_0048	XOSCFAIL
3	0x0000_004C	WDT
4	0x0000_0050	Reserved
5	0x0000_0054	TIMER0
6	0x0000_0058	TIMER1
7	0x0000_005C	TIMER2
8	0x0000_0060	TIMER3
9	0x0000_0064	Reserved
10	0x0000_0068	

11	0x0000_006C	
12	0x0000_0070	
13	0x0000_0074	TIMER8
14	0x0000_0078	TIMER9
15	0x0000_007C	Reserved
16	0x0000_0080	GPIOAE
17	0x0000_0084	GPIOAO
18	0x0000_0088	GPIOBE
19	0x0000_008C	GPIOBO
20	0x0000_0090	GPIOCE
21	0x0000_0094	GPIOCO
22	0x0000_0098	GPIODE
23	0x0000_009C	GPIODO
24	0x0000_00A0	MPWM0
25	0x0000_00A4	MPWM0PROT
26	0x0000_00A8	MPWM0OVV
27	0x0000_00AC	MPWM1
28	0x0000_00B0	MPWM1PROT
29	0x0000_00B4	MPWM1OVV
30	0x0000_00B8	Reserved
31	0x0000_00BC	Reserved
32	0x0000_00C0	SPI0
33	0x0000_00C4	SPI1
34	0x0000_00C8	Reserved
35	0x0000_00CC	
36	0x0000_00D0	I2C0
37	0x0000_00D4	I2C1
38	0x0000_00D8	UART0
39	0x0000_00DC	UART1
40	0x0000_00E0	UART2
41	0x0000_00E4	UART3
42	0x0000_00E8	Reserved
43	0x0000_00EC	ADC0
44	0x0000_00F0	ADC1
45	0x0000_00F4	ADC2
46	0x0000_00F8	COMP0
47	0x0000_00FC	COMP1
48	0x0000_0100	COMP2
49	0x0000_0104	COMP3
50	0x0000_0108	Reserved
51	0x0000_010C	Reserved
52	0x0000_0110	Reserved
53	0x0000_0114	Reserved

54	0x0000_0118	Reserved
55	0x0000_011C	Reserved
56	0x0000_0120	Reserved
57	0x0000_0124	Reserved
58	0x0000_0128	Reserved
59	0x0000_012C	Reserved
60	0x0000_0130	Reserved
61	0x0000_0134	Reserved
62	0x0000_0138	Reserved
63	0x0000_013C	Reserved

3. Boot Mode

Boot Mode Pins

The Z32F1281 MCU has a Boot Mode option to program internal Flash memory. When the BOOT pin is pulled low, the system will start up in the BOOT area (0x1FFF_0000) instead of the default Flash area (0x0000_0000). This provides the ability to flash the part using either UART or SPI interfaces. The BOOT pin has an internal pull up resistor. Therefore, when the BOOT pin is not connected, it rides high (normal state).

Boot Mode uses the UART0 port and the SPI0 ports for the interface. The JTAG and SW interfaces can also be used, which provide the ability to recover from a bad Flash update that prevents the JTAG or SW debugger from attaching.

The pins for Boot Mode are listed in Table 3.1.

Table 3.1. Boot Mode Pin List

Block	Pin Name	Dir	Description
SYSTEM	nRESET/PC10	I	Reset Input signal
	BOOT/PC11	I	'0' to enter Boot mode
UART0	RXD0/PC14	I	UART Boot Receive Data
	TXD0/PC15	O	UART Boot Transmit Data
SPI0	SS0/PA12	I	SPI Boot Slave Select
	SCK0/PA13	I	SPI Boot Clock Input
	MOSI0/PA14	I	SPI Boot Data Input
	MISO0/PA15	O	SPI Boot Data Output

Boot Mode Connections

The target board can be designed using either of the Boot Mode ports – UART or SPI.

Figure 3.1 and Figure 4.1Figure 3.2 show sample connection diagrams in Boot Mode.

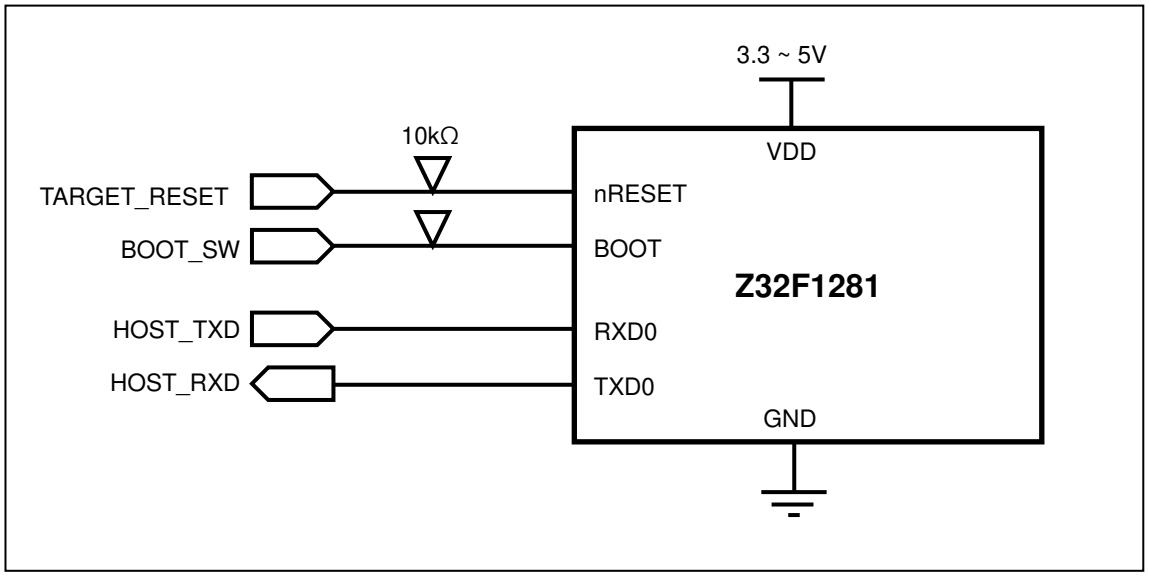

Figure 3.1. Connection Diagram of UART Boot

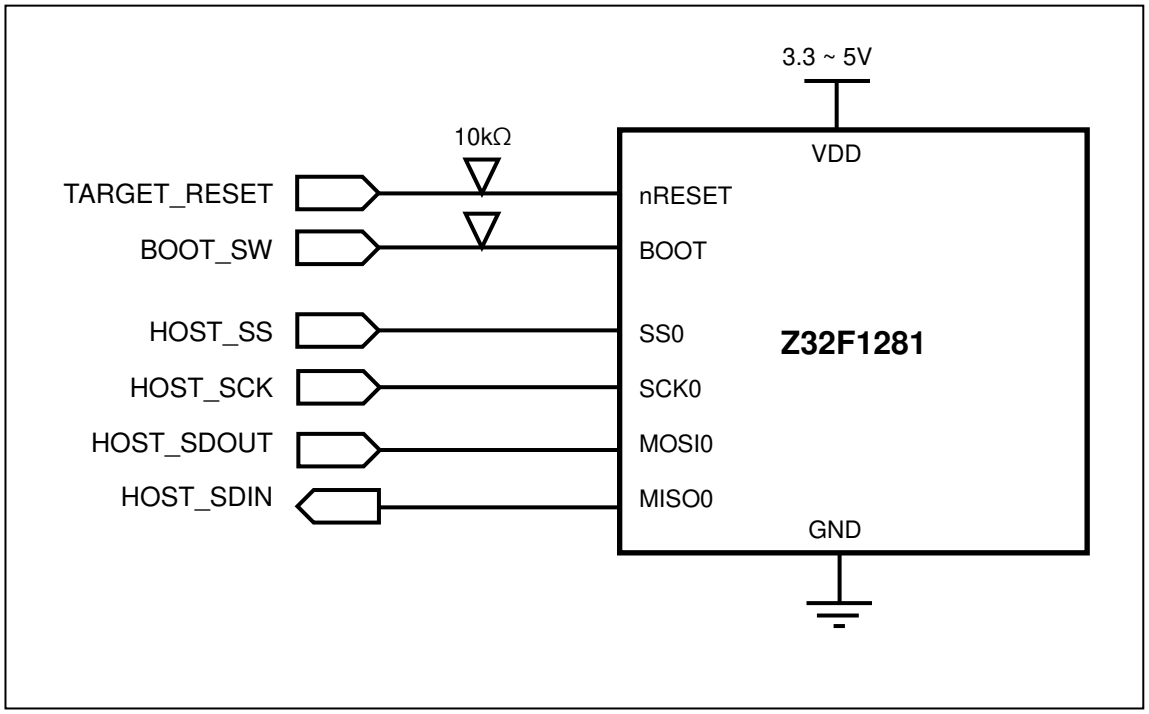

Figure 3.2. Connection Diagram of SPI Boot

4. System Control Unit

Overview

The Z32F1281 MCU has a built-in intelligent power control block which manages system analog blocks and operating modes. Internal reset and clock signals are controlled by the SCU block to maintain optimal system performance and power dissipation.

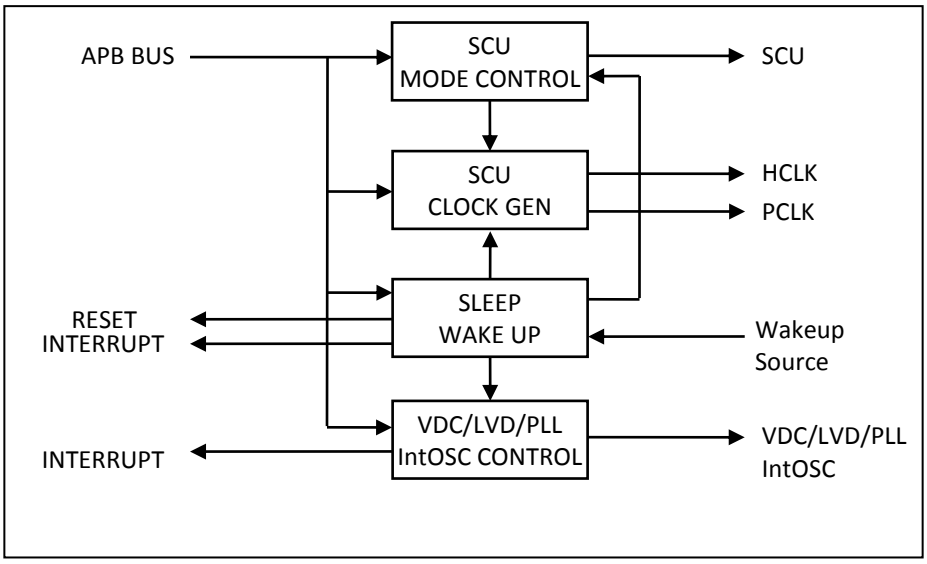

Figure 4.1. SCU Block Diagram

Clock System

The Z32F1281 MCU contains two main operating clocks – HCLK, which supplies the clock to the CPU and the AHB bus system; and PCLK, which supplies the clock to the peripheral systems. Users can control the clock system variation by software. Figure 4.2 shows the clock system of the chip. Table 4.1 lists the clock source descriptions.

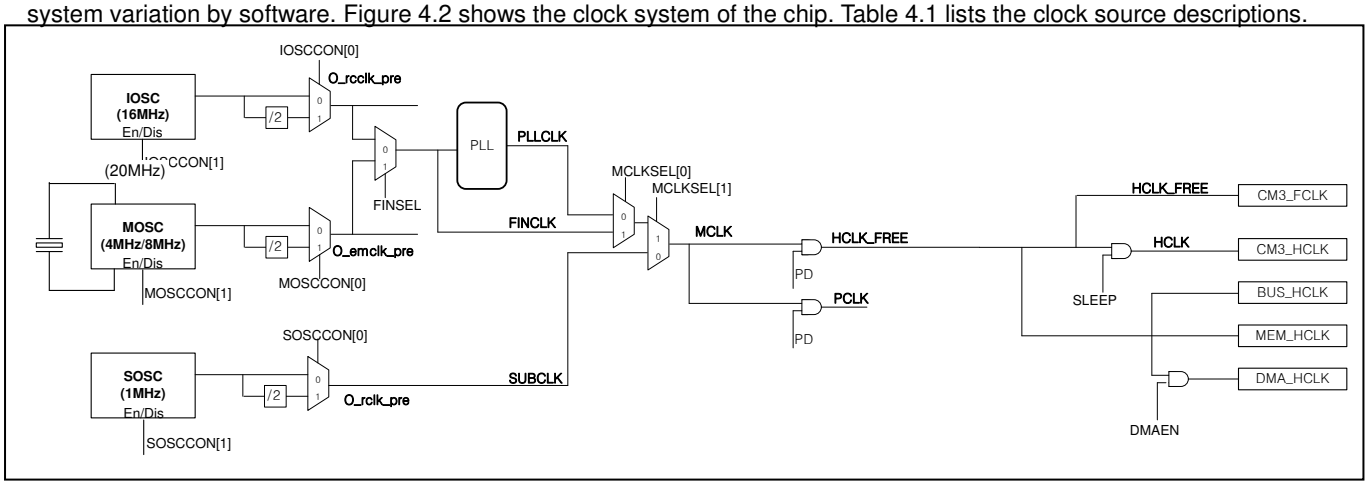

Figure 4.2. System Clock Configuration

Each of the registers to switch the clock source has a glitch-free circuit. Therefore, the clock can be switched without the risk of glitches.

Table 4.1. Clock Sources

Clock name	Frequency	Description
IOSC20	20MHz	Internal OSC
MOSC	XTAL(4MHz~8MHz)	External Crystal IOSC
PLL Clock	8MHz ~ 80MHz	On Chip PLL
ROSC	1MHz	Internal RING OSC

The PLL can synthesize the PLLCLK clock up to 80 MHz with the FIN reference clock. It also has an internal pre-divider and post-divider.

HCLK Clock Domain

The HCLK clock feeds the clock to the CPU and AHB bus. The Cortex-M3 CPU requires two clocks related with HCLK clock – FCLK and HCLK. FCLK is the free running clock and it is always running except in Power-down mode. HCLK can be stopped in Idle mode.