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Embedded in Life

An IXYS Company

ZNEO32! Family of Microcontrollers

Z32F3841 MCU

Product Specification

PS034603-0617

PRELIMINARY

ZNEO32!

32 Bit Microcontrollers

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Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Description	Page
Jun 2017	03	Updated part numbers to include the Cortex M identifier.	All
Mar 2016	02	Update to reflect new part, revision B (0x0002); Added timing information for most of the peripherals; corrected typos.	All
Dec 2015	01	Original issue.	

1. Overview

Introduction

Zilog's Z32F3841 MCU, a member of the ZNEO32! Family of microcontrollers, is a cost-effective and high-performance 32-bit microcontroller. The Z32F3841 MCU provides 3-phase PWM generator units which are suitable for inverter bridges, including motor drive systems. Two built-in channels of these generators control two inverter bridges simultaneously.

Two 12-bit high speed ADC units with 16-channel analog multiplexed inputs support feedback retrieval from the inverter bridge. The Z32F3841 MCU can control up to two inverter motors or one inverter motor and the Power Factor Correction (PFC) function simultaneously.

Figure 1.1 shows a block diagram of the Z32F3841 MCU.

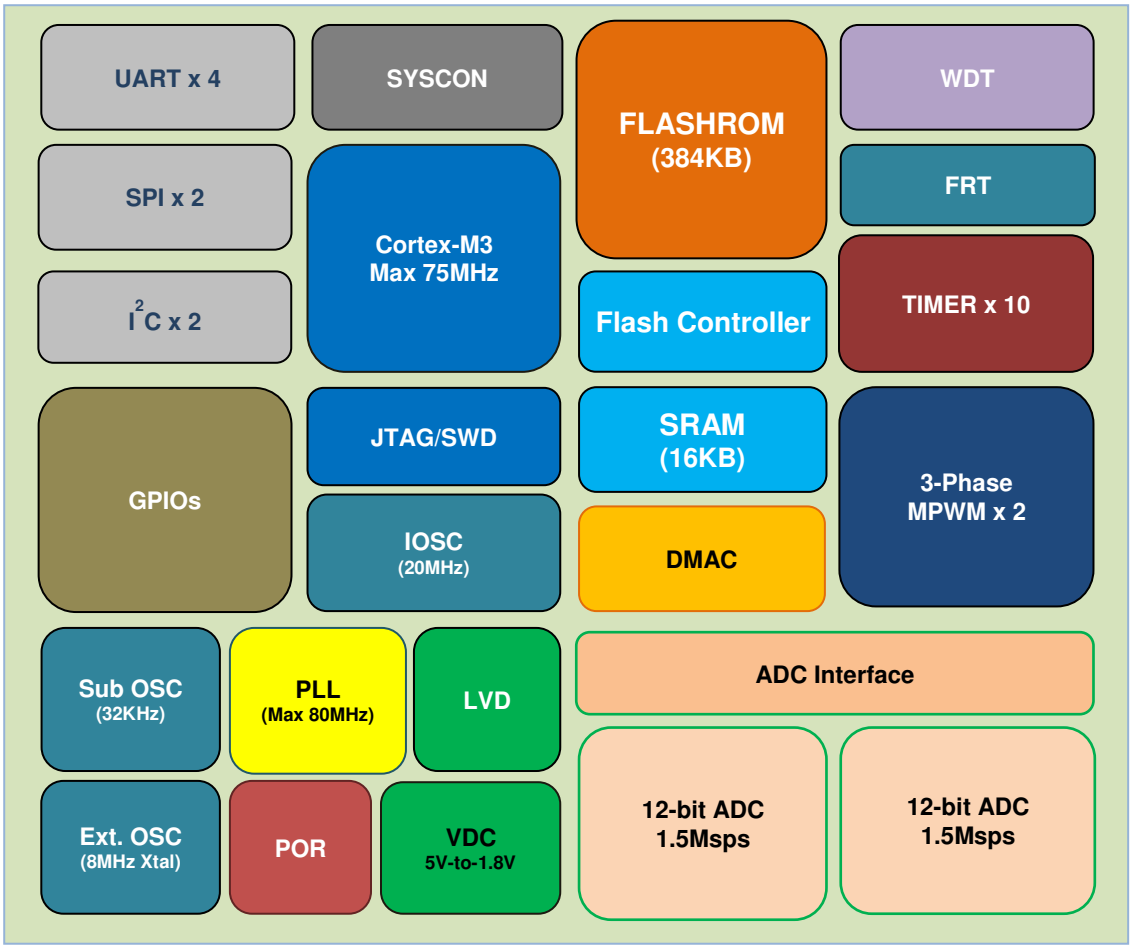

Figure 1.1. Block Diagram

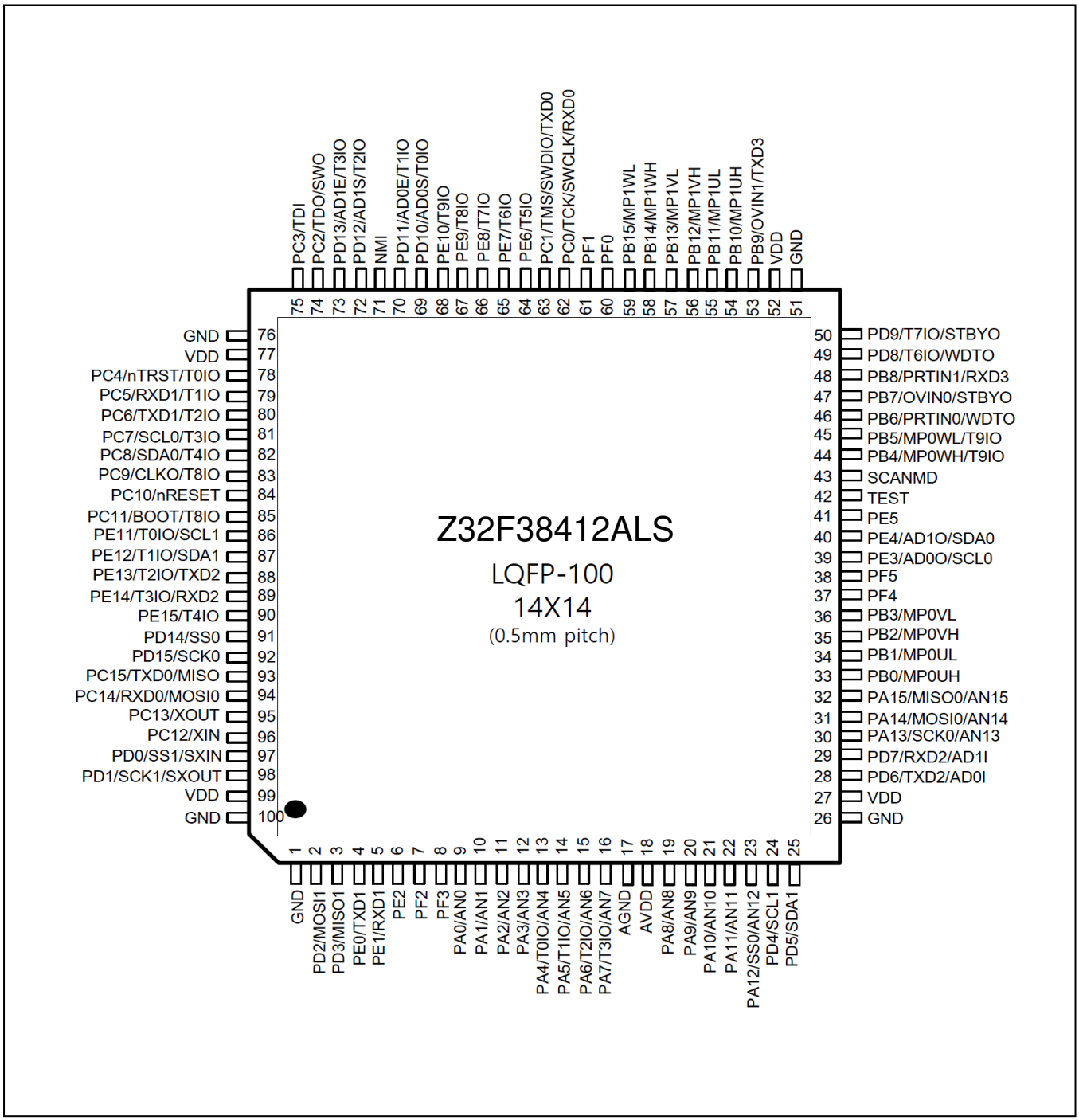

Figure 1.2. Pin Layout (LQFP-100)

Product Features

The Z32F3841 MCU includes the following features:

- High performance low-power Cortex-M3 core
- 384KB code Flash memory with cache function
- 16 KB SRAM
- 3-Phase PWM with ADC triggering function
  - 2 Channels
- 1.5 MSPS high-speed ADC with sequential conversion
  - 2 units with 16 Channel input
- System fail-safe function by clock monitoring
  - XTAL OSC fail monitoring function
  - System clock Fail monitoring function
- Internal clock sources
  - Internal ring oscillator (1 MHz ±50%)
  - Internal oscillator clock (20 MHz ±3%)
  - Internal Phase Lock Loop (PLL) up to 80Mhz
- External clock sources
  - External crystal oscillator (4~16 MHz)
  - External sub oscillator (32 kHz)
- Watchdog timer
- 10 general purpose timer channels
  - Timer/capture/PWM mode
- Free run timer
- Various external communication ports:
  - 4 UARTs
  - 2 I^2Cs
  - 2 SPIs
- High current driving port for UART photo couplers
- Direct Memory Access (DMA) controller with 8 channels
- Debug and emergency stop function
- JTAG and SWD debugger
- Package: LQFP-100 (0.5mm pitch)
- Industrial grade operating temperature (– 40 ~ +85°C)

Architecture

Block Diagram

Figure 1.3 shows the Z32F3841 MCU's internal block diagram.

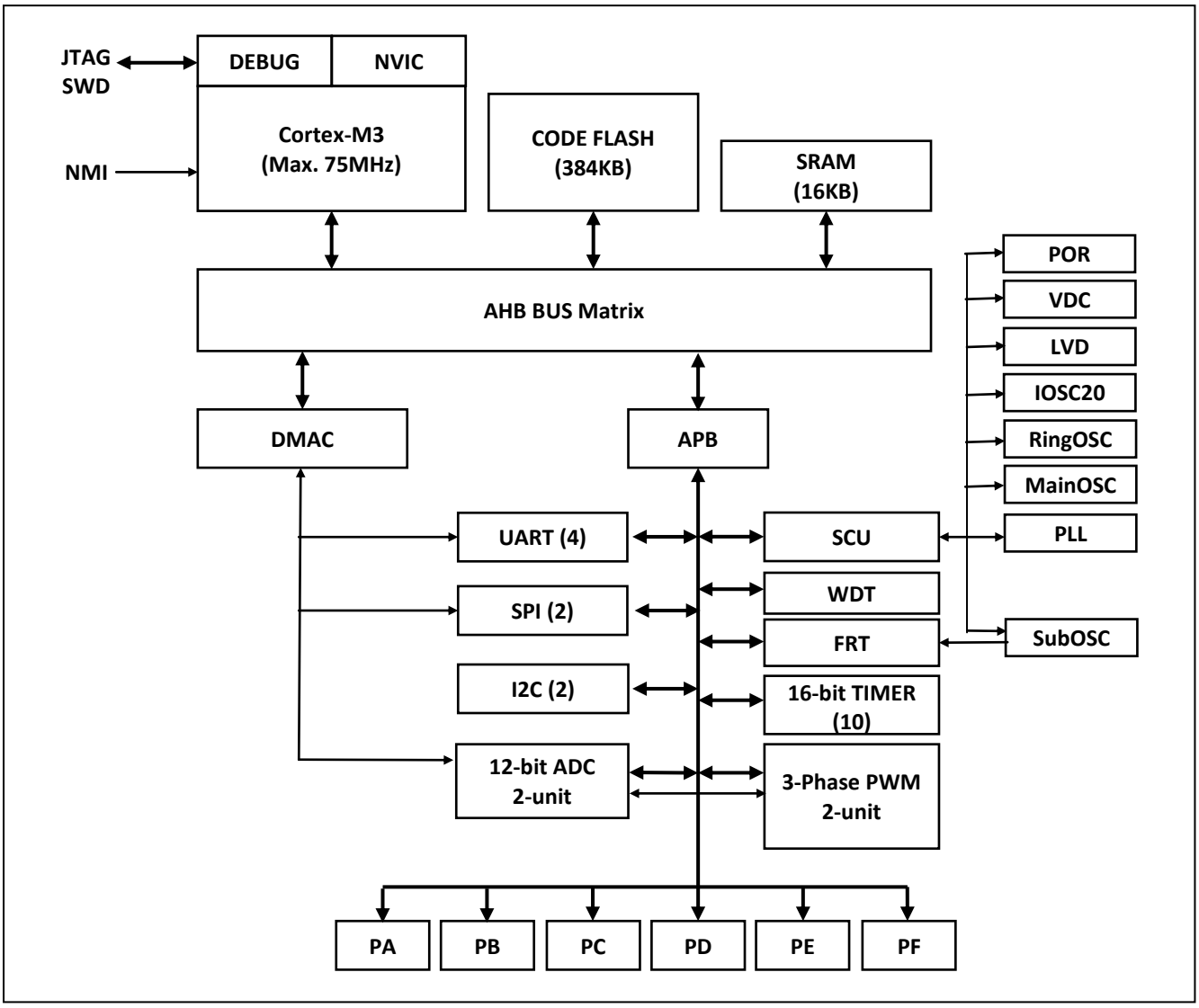

Figure1.3. Internal Block Diagram

Functional Description

The following section provides an overview of the features of the Z32F3841 microcontroller.

ARM Cortex-M3

The ARM-powered Cortex-M3 Core based on v7M architecture is optimized for small size and low power system. An on core system timer (SYSTICK) provides a simple 24-bit timer, that enables easy management of the system operation. The thumb-compatible Thumb-2 only instruction set processor core makes code high-density. Hardware division and single-cycle multiplication is present. Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling. Full featured debug solutions are provided – JTAG and SWD, FPB, DWT, ITM and TPIU. It includes a maximum 72 MHz operating frequency with zero wait execution.

Nested Vector-Interrupt Controller (NVIC)

The ARM Nested Vectored Interrupt Controller (NVIC) on the ARM Cortex-M3 core is included, which handles all internal and external exceptions. When an interrupt condition is detected, the processor state is automatically stored to the stack and automatically restored from the stack at the end of the interrupt service routine. The vector is fetched in parallel to the state saving, which enables efficient interrupt entry. The processor supports tail-chaining, which allows back-to-back interrupts to be performed without the overhead of state saving and restoring.

384 KB Internal Code Flash Memory

The Z32F3841 MCU provides internal 384 KB code Flash memory and its controller. This is enough to program the motor algorithm and generally control the system. Self-programming is available and ISP and JTAG programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth Flash memory. The CPU can execute from Flash memory with zero wait state up to 72 MHz bus frequency.

16 KB Zero-wait Internal SRAM

On chip 16 KB zero-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

Boot Logic

The smart boot logic supports Flash programming. The Z32F3841 MCU can be accessed by an external boot pin and UART and SPI programming are available in boot mode.

System Control Unit (SCU)

The SCU block manages internal power, clock, reset, and operation mode. It also controls analog blocks (INTOSC, VDC and BOD).

32-bit Watchdog Timer (WDT)

The watchdog timer performs the system monitoring function. It generates an internal reset or interrupt when it notices abnormal status of the system.

Multi-purpose 16-bit Timer

10 16-bit general purpose timers channels support the following functions:

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

Free Run Timer

The 32-bit Free run timer has multiple clock sources (XTAL/16, IOSC/16, SXTAL).

Motor PWM Generator

Two channels of the 3-phase PWM generator are implemented. A 16-bit up/down counter with prescaler

supports both the triangular and saw tooth waveform.

The PWM generates an internal ADC trigger signal to measure the signal on time. Dead time insertion and emergency stop functionality ensure that the chip and system operate under safe conditions.

Serial Peripheral Interface (SPI)

Synchronous serial communication is provided with the SPI block. The Z32F3841 MCU has 2-channel SPI modules. It includes a DMA function supported by the DMA controller. Transfer data is moved to/from the memory area without CPU operation. Boot mode uses this SPI block to download the Flash program.

Inter-Integrated Circuit Interface (I^2C)

The Z32F3841 MCU has a 2-channel I^2C block and it supports up to 400 KHz I^2C communication. Master and slave modes are supported.

Universal Asynchronous Receiver/Transmitter (UART)

The Z32F3841 MCU has a 4-channel UART block. For accurate baud rate control, the fractional baud rate generator is provided. It includes a DMA function supported by the DMA controller. Transfer data is moved to/from the memory area without CPU operation.

General PORT I/Os

16-bit PA, PB, PC, PD, PE ports and 6-bit PF are available and provide multiple functionality:

- General I/O port
- Independent bit set/clear function
- External interrupt input port
- Pull-up/open-drain
- On chip debounce filter

12-bit Analog-to-Digital Converter (ADC)

2 built-in ADCs can convert analog signals up to 1usec conversion rate. A 16-channel analog mux provides various combinations from external analog signals.

Pin Description

The pin configurations are shown in Table 1.1. 16 pins are reserved for power/ground pair and dedicated pins.

Table1.1. Pin Description

Pin No	Pin Name	Type	Description	Remark
1	GND	P	Ground	
2	PD2	IOUS	PORT D Bit 2 Input/Output	
	MOSI1	I/O	SPI Channel 1 Master Out / Slave In	
3	PD3*	IOUS	PORT D Bit 3 Input/Output	
	MISO1	I/O	SPI Channel 1 Master In / Slave Out	
4	PE0	IOUS	PORT E Bit 0 input/Output	
	TXD1	Output	UART Channel 1 TXD output	2nd function
5	PE1	IOUS	PORT E Bit 1 input/Output	
	RXD1	Input	UART Channel 1 RXD input	2nd function
6	PE2	IOUS	PORT E Bit 2 input/Output	
	T4I	I/O	Timer 4 Input	2nd function
	T3O	I/O	Timer 3 Output	2nd function
7	PF2	IOUS	PORT F Bit 2 input/Output	
	AN20	IA	Analog Input 20	
8	PF3	IOUS	PORT F Bit 3 input/Output	
	AN21	IA	Analog Input 21	
9	PA0*	IOUS	PORT A Bit 0 Input/Output	
	AN0	IA	Analog Input 0	
10	PA1*	IOUS	PORT A Bit 1 Input/Output	
	AN1	IA	Analog Input1	
11	PA2*	IOUS	PORT A Bit 2 Input/Output	
	AN2	IA	Analog Input 2	
12	PA3*	IOUS	PORT A Bit 3 Input/Output	
	AN3	IA	Analog Input 3	
13	PA4*	IOUS	PORT A Bit 4 Input/Output	
	T0IO	IO	Timer 0 Input/Output	3rd function
	AN4	IA	Analog Input 4	
14	PA5*	IOUS	PORT A Bit 5 Input/Output	
	T1IO	IO	Timer 1 Input/Output	3rd function
	AN5	IA	Analog Input 5	
15	PA6*	IOUS	PORT A Bit 6 Input/Output	
	T2IO	IO	Timer 2 Input/Output	3rd function
	AN6	IA	Analog Input 6	
16	PA7*	IOUS	PORT A Bit 7 Input/Output	
	T3IO	IO	Timer 3 Input/Output	3rd function
	AN7	IA	Analog Input 7	
17	AGND	P	Analog Ground	
18	AVDD	P	Analog VDD	
19	PA8*	IOUS	PORT A Bit 8 Input/Output	
	AN8	IA	Analog Input 8	
20	PA9*	IOUS	PORT A Bit 9 Input/Output	
	AN9	IA	Analog Input 9	

21	PA10*	IOUS	PORT A Bit 10 Input/Output	
	AN10	IA	Analog Input 10	
22	PA11*	IOUS	PORT A Bit 10 Input/Output	
	AN11	IA	Analog Input 11	
23	PA12*	IOUS	PORT A Bit 12 Input/Output	
	SS0	I/O	SPI Channel 0 Slave Select signal	
	AN12	IA	Analog Input 12	
24	PD4	IOUS	PORT D Bit 4 Input/Output	
	SCL1	Output	I2C Channel 1 SCL In/Out	Open-drain
	AN16	IA	Analog Input 16	
25	PD5	IOUS	PORT D Bit 5 Input/Ouput	
	SDA1	Output	I2C Channel 1 SDA In/Out	Open-drain
	AN17	IA	Analog Input 17	
26	GND	P	Ground	
27	VDD	P	VDD	
28	PD6*	IOUS	PORT D Bit 6 Input/Ouput	
	TXD2	Output	UART Channel 2 TxD Output	
	AN18	IA	Analog Input 18	
29	PD7*	IOUS	PORT D Bit 7 Input/Ouput	
	RXD2	Input	UART Channel 2 RxD Input	
	AN19	IA	Analog Input 19	
30	PA13*	IOUS	PORT A Bit 13 Input/Output	
	SCK0	I/O	SPI Channel 0 Clock Input/Output	
	AN13	IA	Analog Input 13	
31	PA14*	IOUS	PORT A Bit 14 Input/Output	
	MOSI0	I/O	SPI Channel 0 Output(M)/Input(S) Data signal	
	AN14	IA	Analog Input 14	
32	PA15*	IOUS	PORT A Bit 15 Input/Output	
	MISO0	I/O	SPI Channel 0 Input(M)/Output(S) Data signal	
	AN15	IA	Analog Input 15	
33	PB0	IOUS	PORT B Bit 0 Input/Output	
	MP0UH	Output	PWM0 UH Output	
34	PB1	IOUS	PORT B Bit 1 Input/Output	
	MP0UL	Output	PWM0 UL Output	
35	PB2	IOUS	PORT B Bit 0 Input/Output	
	MP0VH	Output	PWM0 VH Output	
36	PB3	IOUS	PORT B Bit 1 Input/Output	
	MP0VL	Output	PWM0 VL Output	
37	PF4	IOUS	PORT F Bit 4 Input/Output	
38	PF5	IOUS	PORT F Bit 5 Input/Output	
39	PE3	IOUS	PORT E Bit 3 Input/Output	
	SCL0	Output	I2C Channel 0 SCL In/Out	Open-drain 2nd function
40	PE4	IOUS	PORT E Bit 4 Input/Output	
	SDA0	Output	I2C Channel 0 SDA In/Out	Open-drain 2nd function
41	PE5	IOUS	PORT E Bit 5 Input/Output	
	T5IO	I/O	Timer 5 Input/Output	
42	TEST	Input	Test-mode Input (Always 'L')	Pull-down
43	SCANMD	Input	Scan-mode Input (Always 'L')	Pull-down

44	PB4	IOUS	PORT B Bit 4 Input/Output	
	MP0WH	Output	PWM0 WH Output	
	T9IO	I/O	Timer 9 Input/Output	
45	PB5	IOUS	PORT B Bit 5 Input/Output	
	MP0WL	Output	PWM0 WL Output	
	T9IO	I/O	Timer 9 Input/Output	2nd function
46	PB6	IOUS	PORT B Bit 6 Input/Output	
	PRTIN0	Input	PWM0 Protection Input signal 0	
	WDTO	Output	WDT Output	
47	PB7	IOUS	PORT B Bit 7 Input/Output	
	OVIN0	Input	PWM0 Over-Current Input signal 1	
	STBYO	Output	Power-down mode indication signal	
48	PB8	IOUS	PORT B Bit 8 Input/Output	
	PRTIN1	Input	PWM1 Protection Input signal 0	
	RXD3	Output	UART Channel 3 RXD Input	
49	PD8	IOUS	PORT D Bit 8 Input/Output	
	WDTO	Output	WDT Output	2nd function
	T6IO	I/O	Timer 6 Input/Output	
50	PD9	IOUS	PORT D Bit 9 Input/Output	
	STBYO	Output	Power-down mode indication signal	2nd function
	T7IO	I/O	Timer 7 Input/Output	
51	GND	P	Ground	
52	VDD	P	VDD	
53	PB9	IOUS	PORT B Bit 9 Input/Output	
	OVIN1	Input	PWM1 Over-Current Input signal 1	
	TXD3	Output	UART Channel 3 TXD Output	
54	PB10	IOUS	PORT B Bit 10 Input/Output	
	MP1UH	Output	PWM Channel 1 UH Output	
55	PB11	IOUS	PORT B Bit 11 Input/Output	
	MP1UL	Output	PWM Channel 1 UL Output	
56	PB12	IOUS	PORT B Bit 12 Input/Output	
	MP1VH	Output	PWM Channel 1 VH Output	
57	PB13	IOUS	PORT B Bit 13 Input/Output	
	MP1VL	Output	PWM Channel 1 VL Output	
58	PB14	IOUS	PORT B Bit 14 Input/Output	
	MP1WH	Output	PWM Channel 1 WH Output	
59	PB15	IOUS	PORT B Bit 15 Input/Output	
	MP1WL	Output	PWM Channel 1 WL Output	
60	PF0	IOUS	PORT F Bit 0 Input/Output	
61	PF1	IOUS	PORT F Bit 1 Input/Output	
62	PC0	IOUS	PORT C Bit 0 Input/Output	
	TCK/SWCLK	Input	JTAG TCK, SWD Clock Input	
	RXD0	Input	UART Channel 0 RXD Input	2nd function
63	PC1	IOUS	PORT C Bit 1 Input/Output	
	TMS/SWDIO	I/O	JTAG TMS, SWD Data Input/Output	
	TXD0	Input	UART Channel 0 TXD Output	2nd function
64	PE6	IOUS	PORT E Bit 6 Input/Output	
	T5IO	I/O	Timer 5 Input/Output	2nd function
65	PE7	IOUS	PORT E Bit 7 Input/Output	

	T6IO	I/O	Timer 6 Input/Output	2nd function
66	PE8	IOUS	PORT E Bit 8 Input/Output	
	T7IO	I/O	Timer 7 Input/Output	2nd function
67	PE9	IOUS	PORT E Bit 9 Input/Output	
	T8IO	I/O	Timer 8 Input/Output	3rd function
68	PE10	IOUS	PORT E Bit 10 Input/Output	
	T9IO	I/O	Timer 9 Input/Output	3rd function
69	PD10	IOUS	PORT D Bit 10 Input/Output	
	AD0SOC	Output	ADC0 Start-of-Conversion	
	T0IO	IO	Timer 0 Input/Output	3rd function
70	PD11	IOUS	PORT D Bit 10 Input/Output	
	AD0EOC	Output	ADC0 End-of-Conversion	
	T1IO	IO	Timer 1 Input/Output	3rd function
71	NMI	Input	Non-maskable Interrupt Input	
72	PD12	IOUS	PORT D Bit 12 Input/Output	
	AD1SOC	Output	ADC1 Start-of-Conversion	
	T2IO	IO	Timer 2 Input/Output	3rd function
73	PD13	IOUS	PORT D Bit 13 Input/Output	
	AD1EOC	Output	ADC1 End-of-Conversion	
	T3IO	IO	Timer 3 Input/Output	3rd function
74	PC2	IOUS	PORT C Bit 2 Input/Output	
	TDO/SWO	Output	JTAG TDO, SWO Output	
75	PC3	IOUS	PORT C Bit 3 Input/Output	
	TDI	Input	JTAG TDI Input	
76	GND	P	Ground	
77	VDD	P	VDD	
78	PC4	IOUS	PORT C Bit 4Input/Output	
	nTRST	Input	JTAG nTRST Input	
	T0IO	IO	Timer 0 Input/Output	2nd function
79	PC5	IOUS	PORT C Bit 5Input/Output	
	RXD1	Input	UART Channel 1 RXD Input	
	T1IO	IO	Timer 1 Input/Output	2nd function
80	PC6	IOUS	PORT C Bit 6Input/Output	
	TXD1	Output	UART Channel 1 TXD Output	
	T2IO	IO	Timer 2 Input/Output	2nd function
81	PC7	IOUS	PORT C Bit 7Input/Output	
	SCL0	IO	I2C Channel 0 SCL In/Out	
	T3IO	IO	Timer 3 Input/Output	2nd function
82	PC8	IOUS	PORT C Bit 8 Input/Output	
	SDA0	IO	I2C Channel 0 SDA In/Out	
	T4IO	IO	Timer 4 Input/Output	
83	PC9	IOUS	PORT C Bit 9 Input/Output	
	CLKO	Output	System Clock Output	
	T8IO	IO	Timer 8 Input/Output	
84	PC10	IOUS	PORT C Bit 10 Input/Output	
	nRESET	Input	External Reset Input	Pull-up
85	PC11	IOUS	PORT C Bit 11 Input/Output	
	BOOT	Input	Boot mode Selection Input	
	T8IO	Input	Timer 8 Input/Output	2nd function
86	PE11	IOUS	PORT E Bit 11 Input/Output	
	T0IO	IO	Timer 0 Input/Output/Phase-A Input	4st function

	SCL1	IO	I2C Channel 1 SCL Input/Output	2nd function
87	PE12	IOUS	PORT E Bit 12 Input/Output	
	T1IO	IO	Timer 1 Input/Output/Phase-B Input	4st function
	SDA1	IO	I2C Channel 1 SDA input/Output	2nd function
88	PE13	IOUS	PORT E Bit 13 Input/Output	
	T2IO	IO	Timer 2 Input/Output/Phase-Z Input	4st function
	TXD2	Output	UART Channel 2 TXD Output	2nd function
89	PE14	IOUS	PORT E Bit 14 Input/Output	
	T3IO	IO	Timer 3 Input/Output	4st function
	RXD2	Input	UART Channel 2 RXD Input	2nd function
90	PE15	IOUS	PORT E Bit 15 Input/Output	
	T4IO	IO	Timer 4 Input/Output	2nd function
91	PD14	IOUS	PORT D Bit 14 Input/Output	
	SS0	IO	SPI Channel 0 Slave Select signal	2nd function
92	PD15	IOUS	PORT D Bit 15 Input/Output	
	SCK0	IO	SPI Channel 0 Clock Input/Output	2nd function
93	PC15	IOUS	PORT C Bit 14 Input/Output	
	TXD0	Output	UART Channel 0 TXD Output	
	MISO0	I/O	SPI Channel 0 Input(M)/Output(S)	2nd function
94	PC14	IOUS	PORT C Bit 14 Input/Output	
	RXD0	Input	UART0 RXD Input	
	MOSI0	I/O	SPI Channel 0 Output(M)/Input(S)	2nd function
	VMARGIN	OA	Not used. (test purpose)	
95	PC13	IOUS	PORT C Bit 13 Input/Output	
	XOUT	OA	External Crystal Oscillator Output	
96	PC12	IOUS	PORT C Bit 12 Input/Output	
	XIN	IA	External Crystal Oscillator Input	
97	PD0	IOUS	PORT D Bit 0 Input/Output	
	SS1	I/O	SPI Channel 1 Slave Select signal	
	SXIN	IA	Sub Crystal Oscillator Input	
98	PD1	IOUS	PORT D Bit 1 Input/Output	
	SCK1	I/O	SPI Channel 1 Clock Input/Output	
	SXOUT	OA	Sub Crystal Oscillator Output	
99	VDD	P	VDD	
100	GND	P	Ground	

*Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

Memory Map

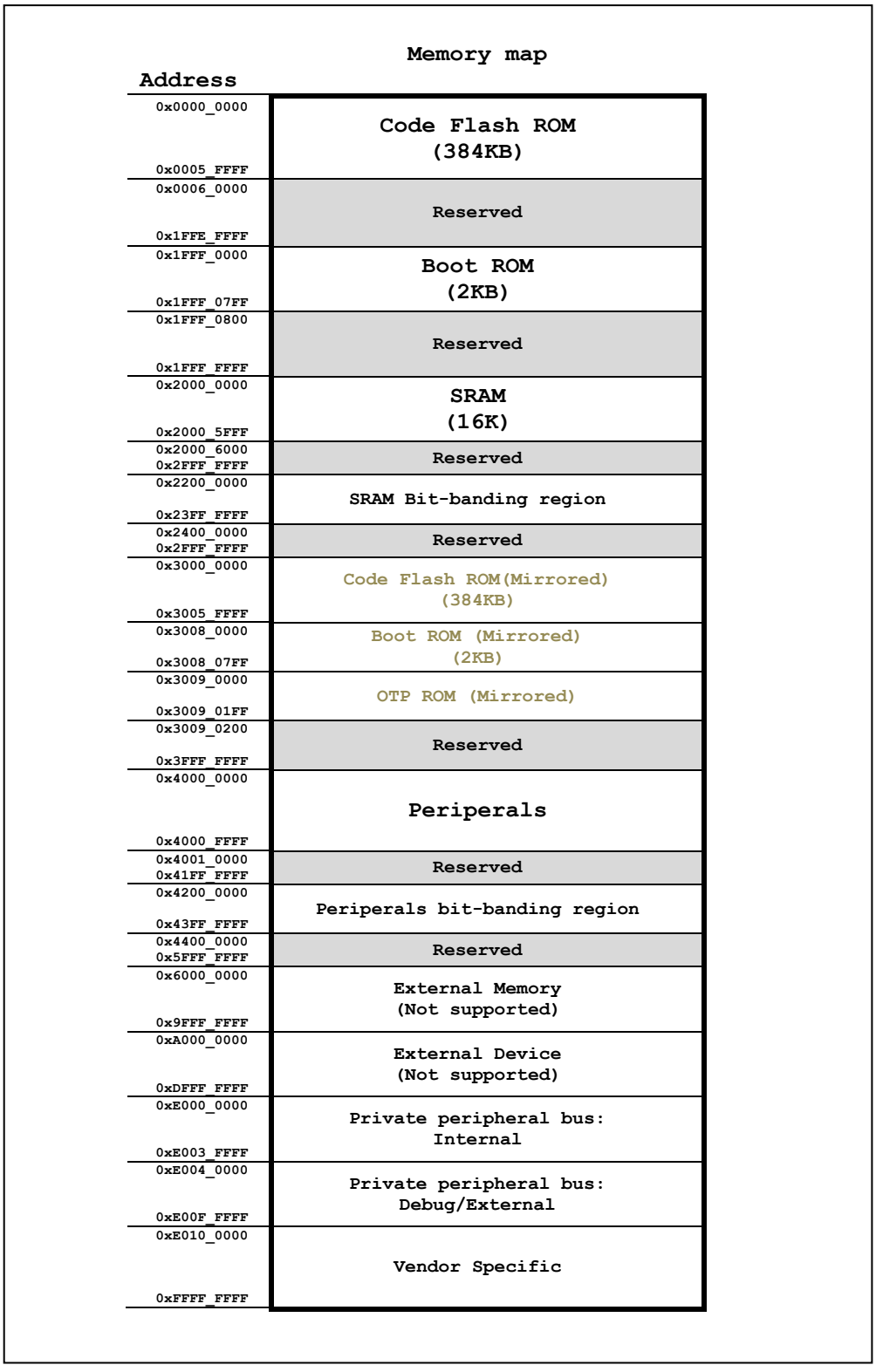

Figure1.4. Main Memory Map

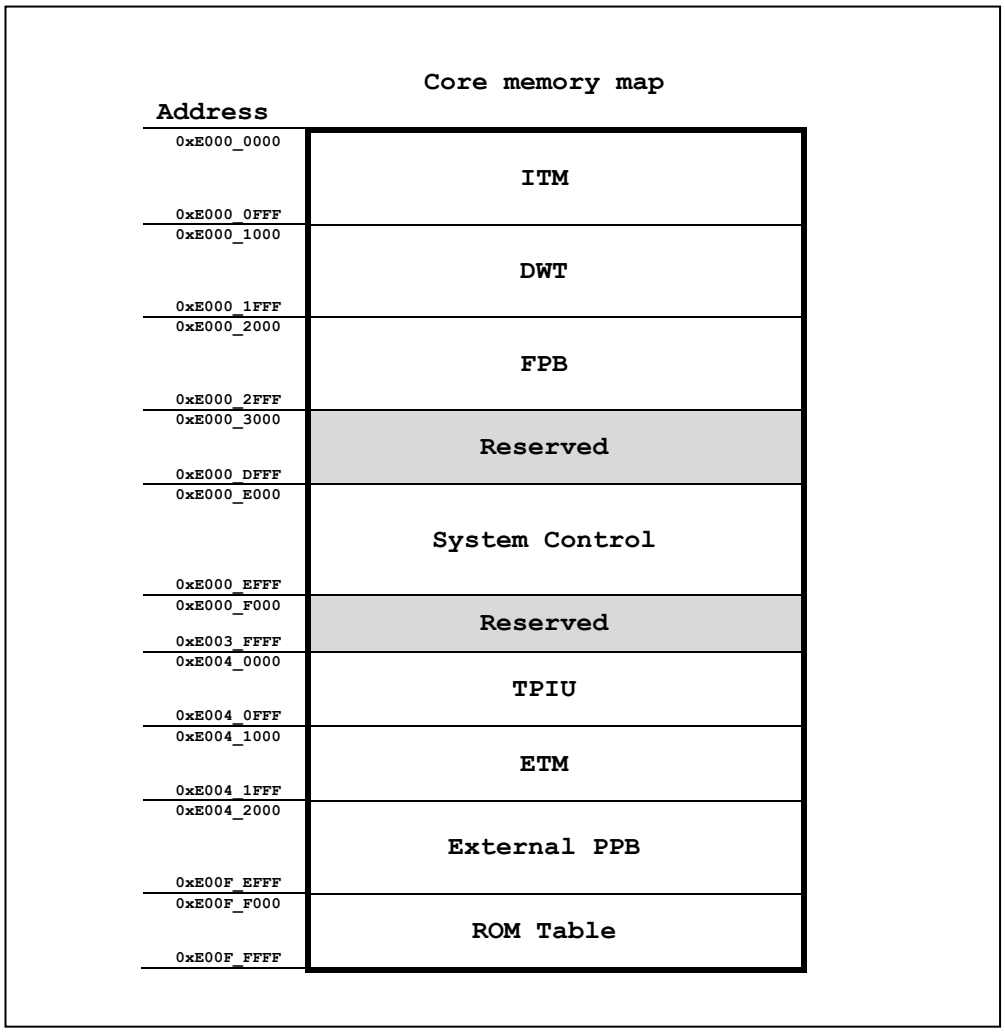

Figure1.5. Cortex-M3 Private Memory Map

Note: Please see document number DDI337 from ARM for more information about the Cortex-M3 memory map.

Address	Peripheral map
0x4000_0000	SCU
0x4000_0100	FMC
0x4000_0200	WDT
0x4000_0300	Reserved
0x4000_0400	DMAC(8)
0x4000_0500	Reserved
0x4000_0600	FRT
0x4000_1000	PCU
0x4000_2000	GPIO(A,B,C,D,E,F)
0x4000_3000	TIMER
0x4000_4000	MPWM0
0x4000_5000	MPWM1
0x4000_6000	Reserved
0x4000_8000	UART0
0x4000_8100	UART1
0x4000_8200	UART2
0x4000_8300	UART3
0x4000_8600	Reserved
0x4000_9000	SPI0
0x4000_9100	SPI1
0x4000_9200	Reserved
0x4000_A000	I^2C0
0x4000_A100	I^2C1
0x4000_A200	Reserved
0z4000_B000	ADC0
0x4000_B100	ADC1
0x4000_B200	Reserved
0x4000_B300	Reserved
0x4000_B400 0x4000_FFFF	Reserved

Figure1.6. Peripheral Memory Map

2. CPU

Cortex-M3 Core

The CPU core is supported from the ARM Cortex-M3 processor which provides a high-performance, low-cost platform.

Document DDI337 from ARM provides more information about the Cortex-M3.

System Timer

The System Timer (SYSTICK) is a 24-bit timer and is part of the Cortex-M3 core. The system timer can be configured either through the registers (see the Cortex-M3 Technical Reference Manual) or through the provided functions defined in `core_cm3.h`. There is an interrupt vector for the system timer. To configure the system timer, call `SysTickConfig()` with the number of system clocks in between Interrupt intervals (up to maximum of 24 bits).

Interrupt Controller

The Nested Vectored Interrupt Controller is part of the core Cortex-M3 MCU. The NVIC controls the system exceptions and peripheral interrupts and is closely coupled with the core to provide low latency and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the nested interrupts to enable tail-chaining of interrupts.

The Z32F3841 MCU supports 64 peripheral interrupts (although 25 are not used) and 16 system interrupts. The NVIC also allows for setting software interrupts as well as resetting the system.

Interrupts can be assigned a Priority Group (common interrupts with the same priorities) as well as individual priorities. Eight priority levels are available. For an interrupt to be active, you must enable it in the peripheral and the NVIC registers. For more information on NVIC, see the Cortex M3 Technical Reference Manual.

The system includes functions to set the NVIC registers, which are defined in the `core_cm3.h`.

Table2.1. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MPU Fault Handler
-11	0x0000_0014	BUS Fault Handler
-10	0x0000_0018	Usage Fault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	Reserved
-7	0x0000_0024	Reserved
-6	0x0000_0028	Reserved
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVDDETECT
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	XOSCFAIL
3	0x0000_004C	WDT
4	0x0000_0050	FRT
5	0x0000_0054	TIMER0
6	0x0000_0058	TIMER1
7	0x0000_005C	TIMER2
8	0x0000_0060	TIMER3
9	0x0000_0064	TIMER4
10	0x0000_0068	TIMER5
11	0x0000_006C	TIMER6
12	0x0000_0070	TIMER7
13	0x0000_0074	TIMER8
14	0x0000_0078	TIMER9
15	0x0000_007C	Reserved
16	0x0000_0080	GPIOAE
17	0x0000_0084	GPIOAO
18	0x0000_0088	GPIOBE
19	0x0000_008C	GPIOBO
20	0x0000_0090	GPIOCE
21	0x0000_0094	GPIOCO
22	0x0000_0098	GPIODE
23	0x0000_009C	GPIODO
24	0x0000_00A0	MPWM0
25	0x0000_00A4	MPWM0PROT

26	0x0000_00A8	MPWM0OVV
27	0x0000_00AC	MPWM1
28	0x0000_00B0	MPWM1PROT
29	0x0000_00B4	MPWM1OVV
30	0x0000_00B8	Reserved
31	0x0000_00BC	Reserved
32	0x0000_00C0	SPI0
33	0x0000_00C4	SPI1
34	0x0000_00C8	Reserved
35	0x0000_00CC	Reserved
36	0x0000_00D0	I2C0
37	0x0000_00D4	I2C1
38	0x0000_00D8	UART0
39	0x0000_00DC	UART1
40	0x0000_00E0	UART2
41	0x0000_00E4	UART3
42	0x0000_00E8	Reserved
43	0x0000_00EC	ADC0
44	0x0000_00F0	ADC1
45	0x0000_00F4	Reserved
46	0x0000_00F8	Reserved
47	0x0000_00FC	Reserved
48	0x0000_0100	Reserved
49	0x0000_0104	Reserved
50	0x0000_0108	GPIOEE
51	0x0000_010C	GPIOEO
52	0x0000_0110	GPIOFE
53	0x0000_0114	GPIOFO
54	0x0000_0118	Reserved
55	0x0000_011C	Reserved
56	0x0000_0120	Reserved
57	0x0000_0124	Reserved
58	0x0000_0128	Reserved
59	0x0000_012C	Reserved
60	0x0000_0130	Reserved
61	0x0000_0134	Reserved
62	0x0000_0138	Reserved
63	0x0000_013C	Reserved

3. Boot Mode

Boot Mode Pins

The Z32F3841 MCU has a boot mode option to program internal Flash memory. When the BOOT pin is pulled low, the system starts up in the BOOT area (0x1FFF_0000) instead of the default Flash area (0x0000_0000). This provides the ability to flash the part using either UART or SPI interfaces. The BOOT pin has an internal pull up resistor; therefore, when the BOOT pin is not connected, it rides high (normal state).

The boot mode uses the UART0 port and the SPI0 ports for the interface. JTAG and SW interfaces can also be used, which provides the ability to recover from a bad flash update that prevents the JTAG or SW debugger from attaching.

The pins for boot mode are listed in Table 3.1.

Table3.1. Boot Mode Pin List

Block	Pin Name	Dir	Description
SYSTEM	nRESET/PC10	I	Reset Input signal
	BOOT/PC11	I	'0' to enter Boot mode
UART0	RXD0/PC14	I	UART Boot Receive Data
	TXD0/PC15	O	UART Boot Transmit Data
SPI0	SS0/PA12	I	SPI Boot Slave Select
	SCK0/PA13	I	SPI Boot Clock Input
	MOSI0/PA14	I	SPI Boot Data Input
	MISO0/PA15	O	SPI Boot Data Output

Boot Mode Connections

Users can design the target board using either of the boot mode ports – UART or SPI.

Figures 3.1 and 3.2 show sample boot mode connection diagrams.

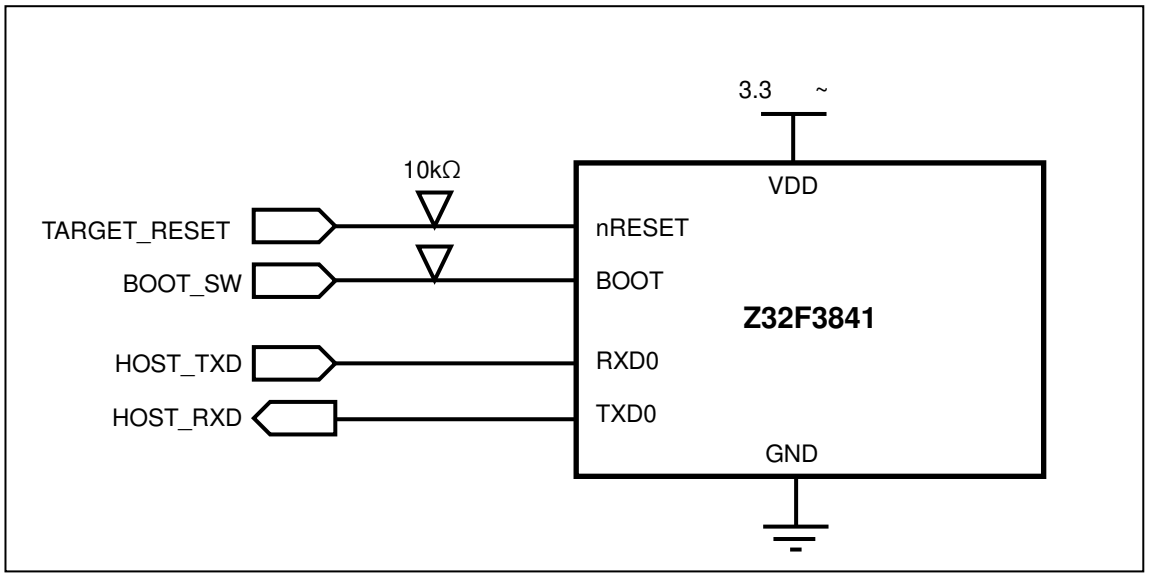

Figure3.1. UART Boot Connection Diagram

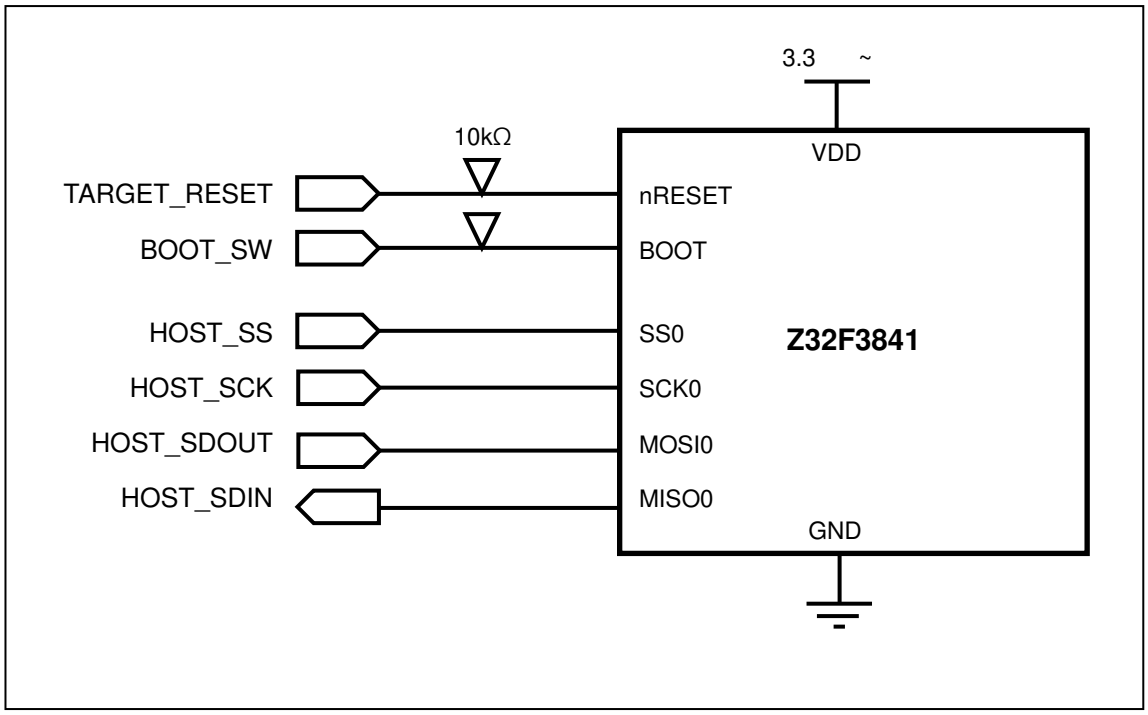

Figure3.2. SPI Boot Connection Diagram

4. System Control Unit

Overview

The Z32F3841 MCU has a built-in intelligent power control block which manages system analog blocks and operating modes. Internal reset and clock signals are controlled by SCU block to maintain optimize system performance and power dissipation.

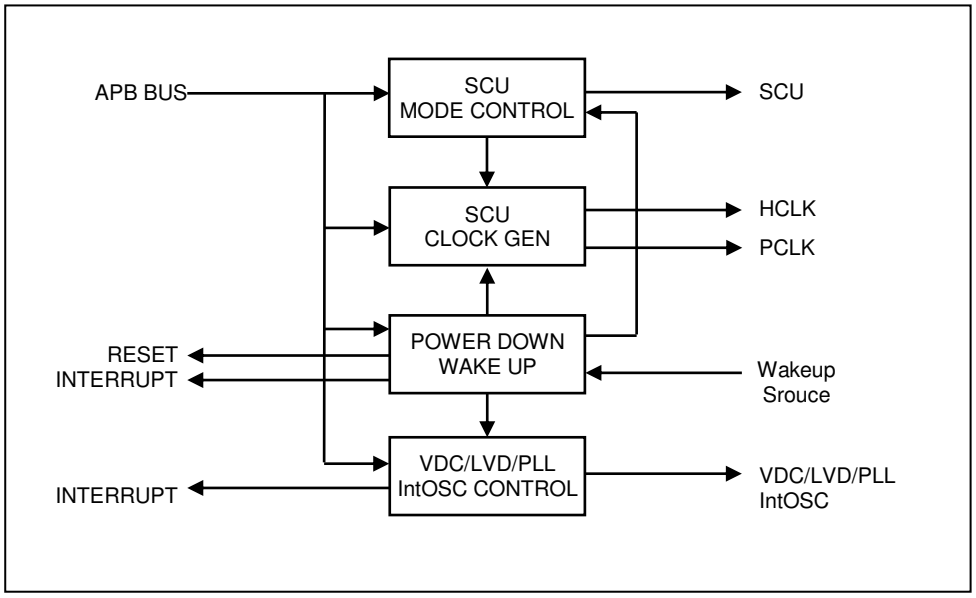

Figure 4.1. SCU Block Diagram

Clock System

The Z32F3841 MCU has two main clock systems. One is MCLK which supplies the clock to the HCLK_Free, CPU and AHB bus system. The PCLK clock is for the Peripheral clock and is supplied from MCLK. Some peripherals have the option to derive their clock from other clocks or the PCLK. User can control the clock system variation by software. Figure 4.2 shows the clock system of the chip, Table 4.1 lists the clock source descriptions.

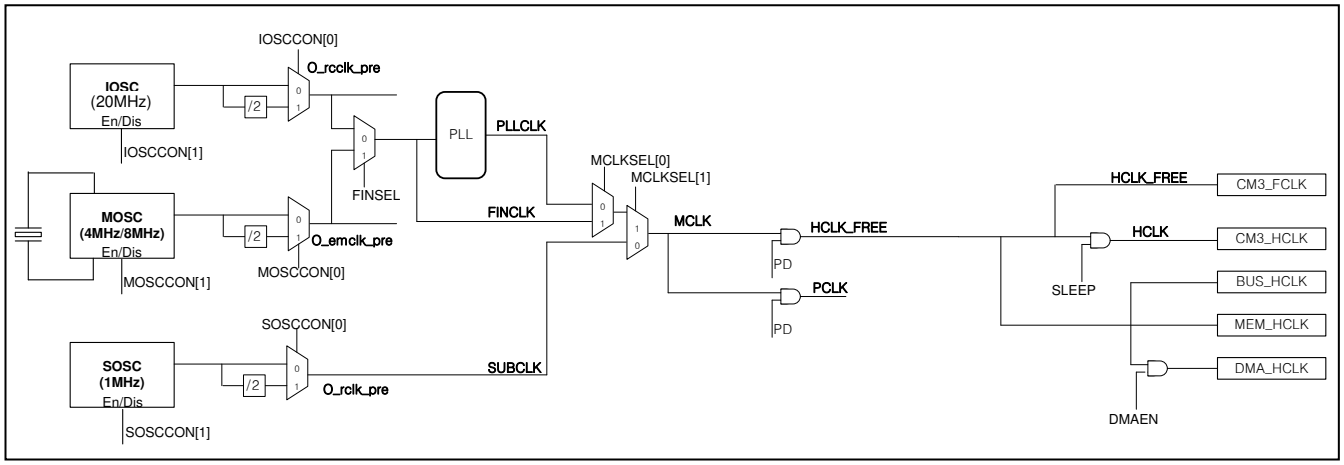

Figure 4.2. System Clock Configuration

Each of the mux to switch clock sources has a glitch-free circuit; therefore, the clock can be switched without a risk of glitches.

Table 4.1. Clock Sources

Clock name	Frequency	Description
IOSC20	20MHz	Internal OSC
Sub OSC	Sub X-TAL (32.768KHz)	Sub External Crystal OSC
MainOSC	X-TAL(4MHz~16MHz)	External Crystal OSC
PLL Clock	8MHz ~ 80MHz	On Chip PLL
ROSC	1MHz	Internal RING OSC

The PLL can synthesize the PLLCLK clock up to 80 MHz with either the Internal Oscillator or the External Crystal Oscillator reference clocks. It also has an internal pre-divider and post-divider.

HCLK Clock Domain

The HCLK clock feeds the clock to the CPU and AHB bus. The Cortex-M3 CPU requires two clocks related to the HCLK clock, FCLK and HCLK. FCLK is a free running clock and is always running except in power down mode. HCLK can be stopped in idle mode.

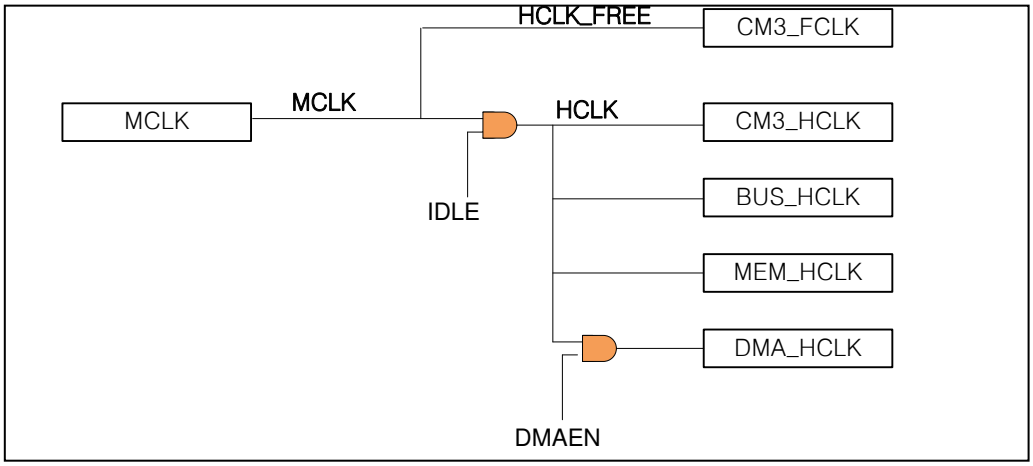

Figure 4.3. System Clock Configuration

Miscellaneous Clock Domain for Cortex-M3

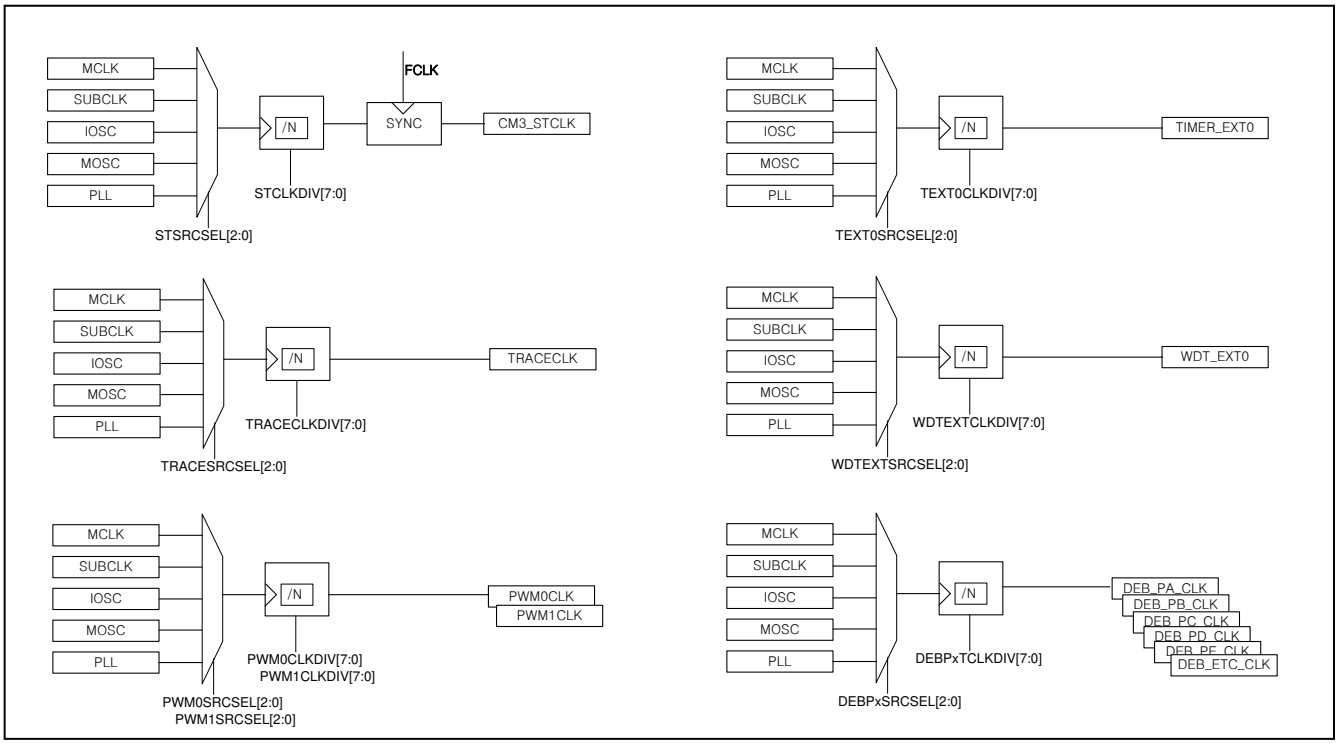

Figure 4.4. Miscellaneous Clock Configuration

PCLK Clock Domain

PCLK is the master clock of all the peripherals. It can be stopped in power down mode. Each peripheral clock is generated by the PCER register set.

Clock Configuration Procedure

After power up, the default system clock is fed by the RINGOSC (1 MHz) clock. RINGOSC is enabled by default during the power up sequence. The other clock sources are enabled by user controls with the RINGOSC system clock.

The MOSC clock can be enabled by the CSCR register. Prior to enabling the MOSC block, the pin mux configuration should be set for the XIN, XOUT function. PC12 and PC13 pins are shared with the MOSC's XIN and XOUT function; the PCCMR and PCCCR registers should be correctly configured. After enabling the MOSC block, you must wait for more than 1 msec to ensure stable crystal oscillation operation.

The PLL clock can be enabled by the PLLCON register. After enabling the PLL block, you must wait for the PLL lock, before you can select the PLL clock as the MCLK. Before changing the system clock, Flash access wait should be set to the maximum value. After the system clock is changed, you can set the desired Flash access wait value.