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Z8018x

Family MPU

User Manual

UM005003-0703

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MANUAL OBJECTIVES

This user manual describes the features of the Z8018x MPUs.This manual provides basic programming information for the Z80180/Z8S180/ Z8L180. These cores and base peripheral sets are used in a large family of ZiLOG products. Below is a list of ZiLOG products that use this class of processor, along with the associated processor family. This document is also the core user manual for the following products:

Part	Family
Z80180	Z80180
Z8S180	Z8S180
Z8L180	Z8L180
Z80181	Z80180
Z80182	Z80180, Z8S180*
Z80S183	Z8S180
Z80185/195	Z8S180
Z80189	Z8S180

* Part number-dependant

Intended Audience

This manual is written for those who program the Z8018x.

Manual Organization

The Z8018x User Manual is divided into five sections, seven appendices, and an index.

Sections

Z8018X MPU Operation

Presents features, a general description, pins descriptions, block diagrams, registers, and details of operating modes for the Z8018x MPUs.

Software Architecture

Provides instruction sets and CPU registers for the Z8018x MPUs.

DC Characteristics

Presents the DC parameters and absolute maximum ratings for the Z8X180 MPUs.

AC Characteristics

Presents the AC parameters for the Z8018x MPUs.

Timing Diagrams

Contains timing diagrams and standard test conditions for the Z8018x MPUs.

Appendices

The appendixes in this manual provide additional information applicable to the Z8018x family of ZiLOG MPUs:

- Instruction set
- Instruction summary table
- Op Code map
- Bus Control signal conditions in each machine cycle and interrupt conditions
- Operating mode summary
- Status signals
- I/O registers and ordering information

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Z80180, Z8S180, Z8L180 MPU Operation 1

Z80180, Z8S180, Z8L180 MPU Operation

FEATURES

- Operating Frequency to 33 MHz
- On-Chip MMU Supports Extended Address Space
- Two DMA Channels
- On-Chip Wait State Generators
- Two Universal Asynchronous Receiver/Transmitter (UART) Channels
- Two 16-Bit Timer Channels
- On-Chip Interrupt Controller
- On-Chip Clock Oscillator/Generator
- Clocked Serial I/O Port
- Code Compatible with ZiLOG Z80 CPU
- Extended Instructions

GENERAL DESCRIPTION

Based on a microcoded execution unit and an advanced CMOS manufacturing technology, the Z80180, Z8S180, Z8L180 (Z8X180) is an 8-bit MPU which provides the benefits of reduced system costs and low power operation while offering higher performance and maintaining compatibility with a large base of industry standard software written around the ZiLOG Z8X CPU.

Higher performance is obtained by virtue of higher operating frequencies, reduced instruction execution times, an enhanced instruction set, and an

on-chip memory management unit (MMU) with the capability of addressing up to 1 MB of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several *glue* functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Not only does the Z8X180 consume a low amount of power during normal operation, but processors with Z8S180 and Z8L180 class processors also provides two operating modes that are designed to drastically reduce the power consumption even further. The SLEEP mode reduces power by placing the CPU into a *stopped* state, thereby consuming less current, while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a *stopped* state, thereby reducing power consumption even further.

When combined with other CMOS VLSI devices and memories, the Z8X180 provides an excellent solution to system applications requiring high performance, and low power operation.

Figures 1 through 3 illustrate the three pin packages in the Z8X180 MPU family:

- 64-Pin Dual In-line Package (DIP), Figure 1
- 68-Pin Plastic Leaded Chip Carrier (PLCC), Figure 2
- 80-Pin Quad Flat Pack (QFP), Figure 3

Pin out package descriptions for other Z8X180-based products are covered in their respective product specifications.

Figure 4 depicts the block diagram that is shared throughout all configurations of the Z8X180.

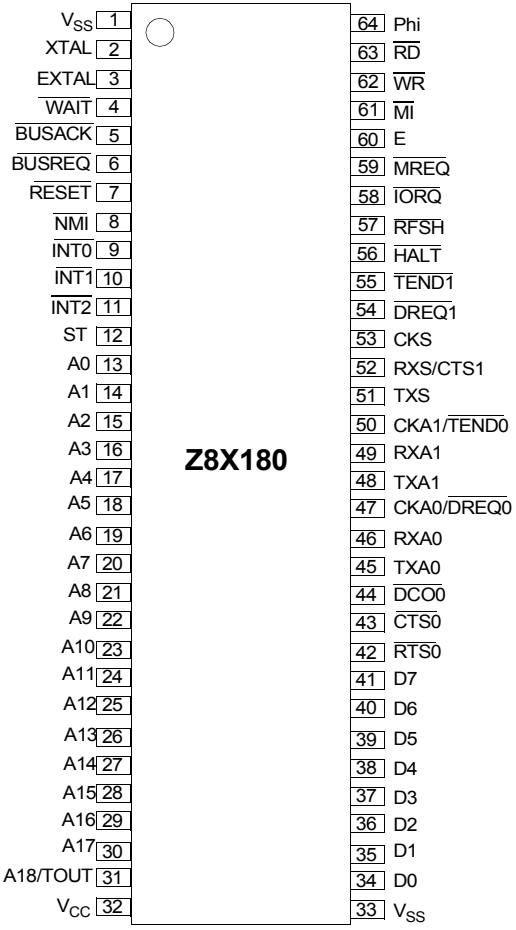

Figure 1. 64-Pin DIP

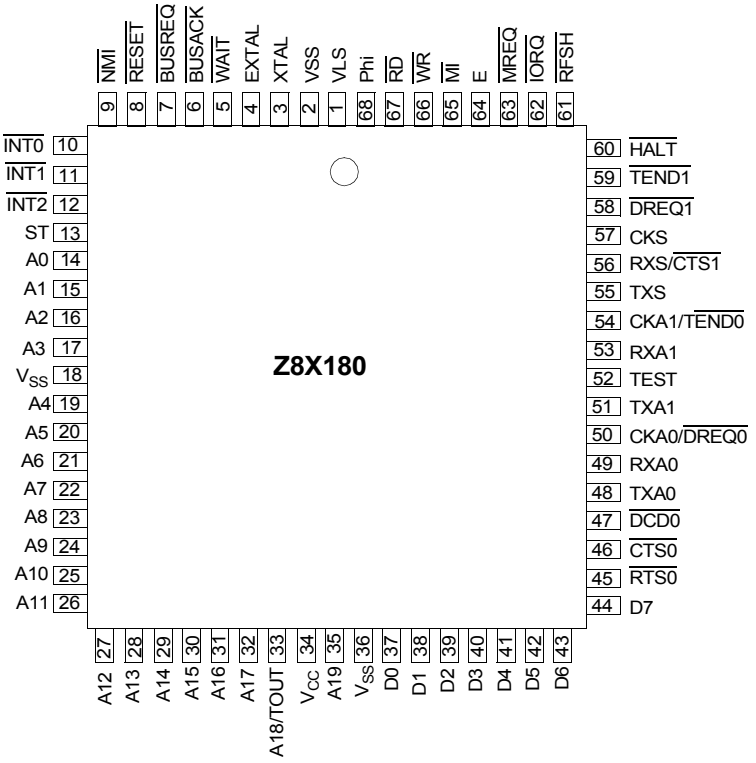

Figure 2. 68-Pin PLCC

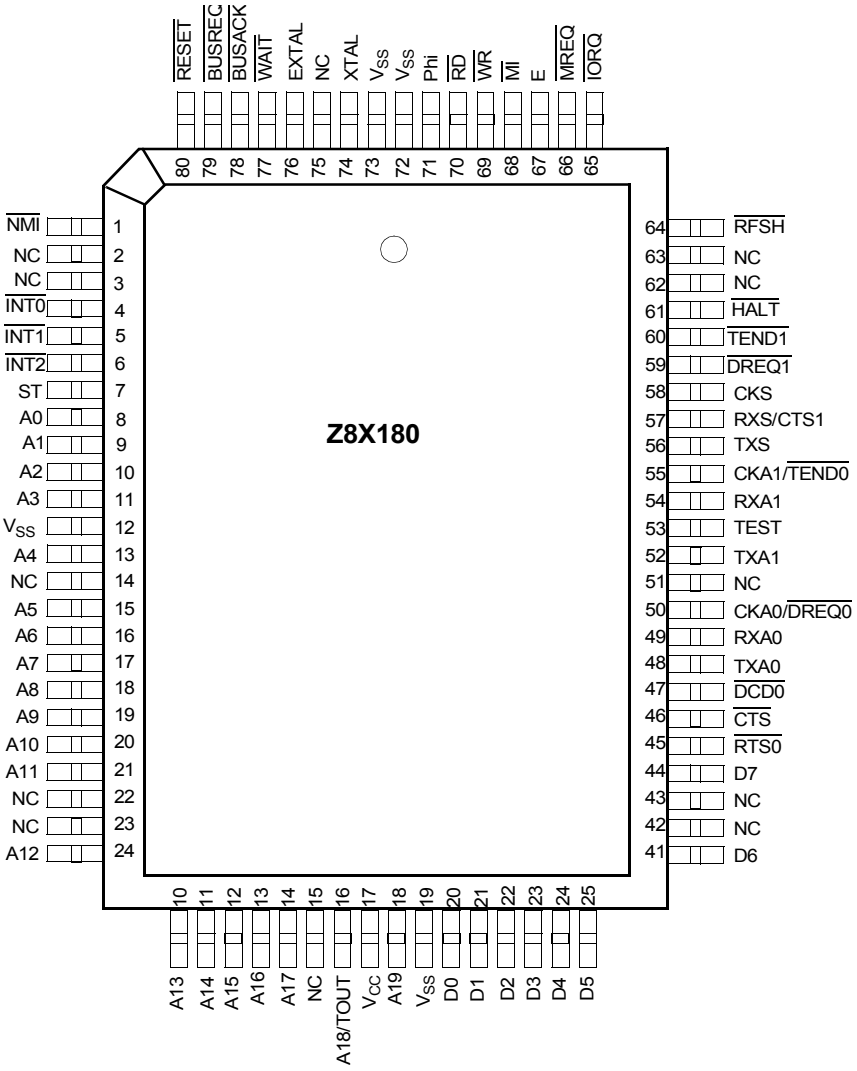

Figure 3. 80-Pin QFP

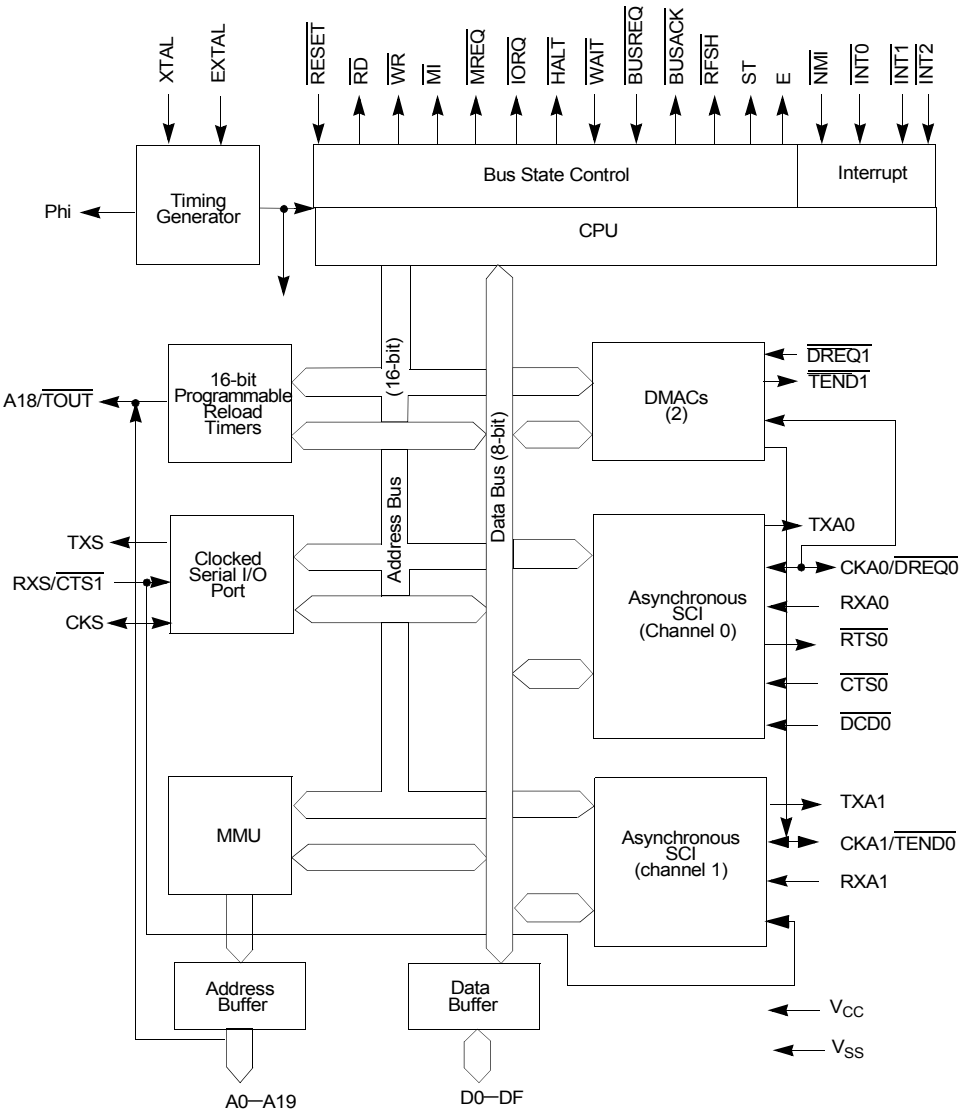

Figure 4. Z80180/Z8S180/Z8L180 Block Diagram

PIN DESCRIPTION

A0–A19. *Address Bus (Output, Active High, 3-state).* A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges, up to 1 MB, and I/O data bus exchanges, up to 64K. The address bus enters a high impedance state during RESET and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (TOUT, selected as address output on RESET) and address line A19 is not available in DIP versions of the Z8X180.

$\overline{\text{BUSACK}}$. *Bus Acknowledge (Output, Active Low).* $\overline{\text{BUSACK}}$ indicates that the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

$\overline{\text{BUSREQ}}$. *Bus Request (Input, Active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions and places the address and data buses, and other control signals, into the high impedance state.

CKA0, CKA1. *Asynchronous Clock 0 and 1 (Bidirectional, Active High).* These pins are the transmit and receive clocks for the ASCI channels. CKA0, is multiplexed with $\overline{\text{DREQ0}}$ and CKA1 is multiplexed with $\overline{\text{TEND0}}$.

CKS. *Serial Clock (Bidirectional, Active High).* This line is the clock for the CSIO channel.

CLOCK (PHI). *System Clock (Output, Active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.

$\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$. *Clear to Send 0 and 1 (Inputs, Active Low).* These lines are modem control signals for the ASCI channels. $\overline{\text{CTS1}}$ is multiplexed with RXS.

D0–D7. *Data Bus (Bidirectional, Active High, 3-state).* D0-D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during RESET and external bus acknowledge cycles.

$\overline{\text{DCD0}}$. *Data Carrier Detect 0 (Input, Active Low).* This input is a programmable modem control signal for ASCI channel 0.

$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$. *DMA Request 0 and 1 (Input, Active Low).* DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a read or write operation. These inputs can be programmed to be either level- or edge-sensed. $\overline{\text{DREQ0}}$ is multiplexed with CKA0.

E. *Enable Clock (Output, Active High).* Synchronous machine cycle clock output during bus transactions.

EXTAL. *External Clock/Crystal (Input, Active High).* Crystal oscillator connection. An external clock can be input to the Z8X180 on this pin when a crystal is not used. This input is Schmitt-triggered.

$\overline{\text{HALT}}$. *Halt/Sleep Status (Output, Active Low).* This output is asserted after the CPU has executed either the $\overline{\text{HALT}}$ or SLP instruction, and is waiting for either non-maskable or maskable interrupt before operation can resume. $\overline{\text{HALT}}$ is also used with the $\overline{\text{M1}}$ and ST signals to decode status of the CPU machine cycle.

$\overline{\text{INT0}}$. *Maskable Interrupt Request 0 (Input, Active Low).* This signal is generated by external I/O devices. The CPU honors this request at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become Active.

$\overline{\text{INT1}}$, $\overline{\text{INT2}}$. *Maskable Interrupt Requests 1 and 2 (Inputs, Active Low).* This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$,

$\overline{\text{BUSREQ}}$, and $\overline{\text{INT0}}$ signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{\text{INT0}}$, during this cycle neither the $\overline{\text{M1}}$ or $\overline{\text{IORQ}}$ signals become Active.

$\overline{\text{IORQ}}$. *I/O Request (Output, Active Low, 3-state).* $\overline{\text{IORQ}}$ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. $\overline{\text{IORQ}}$ is also generated, along with $\overline{\text{M1}}$, during the acknowledgment of the $\overline{\text{INT0}}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the $\overline{\text{IOE}}$ signal of the Z64180.

$\overline{\text{M1}}$. *Machine Cycle 1 (Output, Active Low).* Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the Op Code fetch cycle of an instruction execution. Together with $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is for an interrupt acknowledge. It is also used with the $\overline{\text{HALT}}$ and ST signal to decode status of the CPU machine cycle. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180.

$\overline{\text{MREQ}}$. *Memory Request (Output, Active Low, 3-state).* $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the $\overline{\text{ME}}$ signal of the Z64180.

$\overline{\text{NMI}}$. *Non-maskable Interrupt (Input, negative edge triggered).* $\overline{\text{NMI}}$ has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location `0066H`.

$\overline{\text{RD}}$. *Read (Output active Low, 3-state).* $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device must use this signal to gate data onto the CPU data bus.

$\overline{\text{RFSH}}$. *Refresh (Output, Active Low).* Together with $\overline{\text{MREQ}}$, $\overline{\text{RFSH}}$ indicates that the current CPU machine cycle and the contents of the address bus must be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7–A0) contain the refresh address.

This signal is analogous to the $\overline{\text{REF}}$ signal of the Z64180.

$\overline{\text{RTS0}}$. *Request to Send 0 (Output, Active Low).* This output is a programmable modem control signal for ASCI channel 0.

RXA0, RXA1. *Receive Data 0 and 1 (Inputs, Active High).* These signals are the receive data to the ASCI channels.

RXS. *Clocked Serial Receive Data (Input, Active High).* This line is the receiver data for the CSIO channel. RXS is multiplexed with the $\overline{\text{CTS1}}$ signal for ASCI channel 1.

ST. *Status (Output, Active High).* This signal is used with the $\overline{\text{M1}}$ and $\overline{\text{HALT}}$ output to decode the status of the CPU machine cycle. Table 1 provides status summary.

Table 1. Status Summary

ST	$\overline{\text{HALT}}$	$\overline{\text{M1}}$	Operation
0	1	0	CPU operation (1st Op Code fetch)
1	1	0	CPU operation (2nd Op Code and 3rd Op Code fetch)
1	1	1	CPU operation (MC[2] except for Op Code fetch)
0	X[1]	1	DMA operation
0	0	0	HALT mode
1	0	1	SLEEP mode (including SYSTEM STOP mode)

1. X = Don't care
2. MC = Machine cycle

$\overline{\text{TEND0}}$, $\overline{\text{TEND1}}$. *Transfer End 0 and 1 (Outputs, Active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{\text{TEND0}}$ in multiplexed with CKA1.

TEST. *Test (Output, not on DIP version).* This pin is for test and must be left open.