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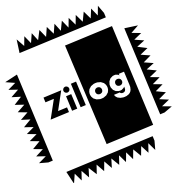
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# Z80182/Z8L182

## ZILOG INTELLIGENT PERIPHERAL CONTROLLER (ZIP™)

### FEATURES

- Z8S180 MPU
  - Code Compatible with Zilog Z80®/Z180™ CPU
  - Extended Instructions
  - Operating Frequency: 33 MHz/5V or 20 MHz/3.3V
  - Two DMA Channels
  - On-Chip Wait State Generators
  - Two UART Channels
  - Two 16-Bit Timer Counters
  - On-Chip Interrupt Controller
  - On-Chip Clock Oscillator/Generator
  - Clocked Serial I/O Port
  - Fully Static
  - Low EMI Option
- Two ESCC™ Channels with 32-Bit CRC
- Three 8-Bit Parallel I/O Ports
- 16550 Compatible MIMIC Interface for Direct Connection to PC, XT, AT Bus
- 100-Pin Package Styles (QFP, VQFP) (0.8 Micron CMOS 5120 Technology)
- Individual WSG for RAMCS and ROMCS

### GENERAL DESCRIPTION

The Z80182/Z8L182 is a smart peripheral controller IC for modem (in particular V. Fast applications), fax, voice messaging and other communications applications. It uses the Z80180 microprocessor (Z8S180 MPU core) linked with two channels of the industry standard Z85230 ESCC (Enhanced Serial Communications Controller), 24 bits of parallel I/O, and a 16550 MIMIC for direct connection to the IBM PC, XT, AT bus.

The Z80182/Z8L182 allows complete flexibility for both internal PC and external applications. Also current PC modem software compatibility can be maintained with the Z80182/Z8L182 ability to mimic the 16550 UART chip. The Z80180 acts as an interface between the ESCC™ and 16550 MIMIC interface when used in internal applications, and between the two ESCC channels in the external applications. This interface allows data compression and

error correction on outgoing and incoming data. In external applications, three 8-bit parallel ports are available for driving LEDs or other devices. Figure 1 shows the Z80182/Z8L182 block diagram, while the pin assignments for the QFP and the VQFP packages are shown in Figures 2 and 3, respectively. All references in this document to the Z80182, or Z182 refer to both the Z80182 and Z8L182.

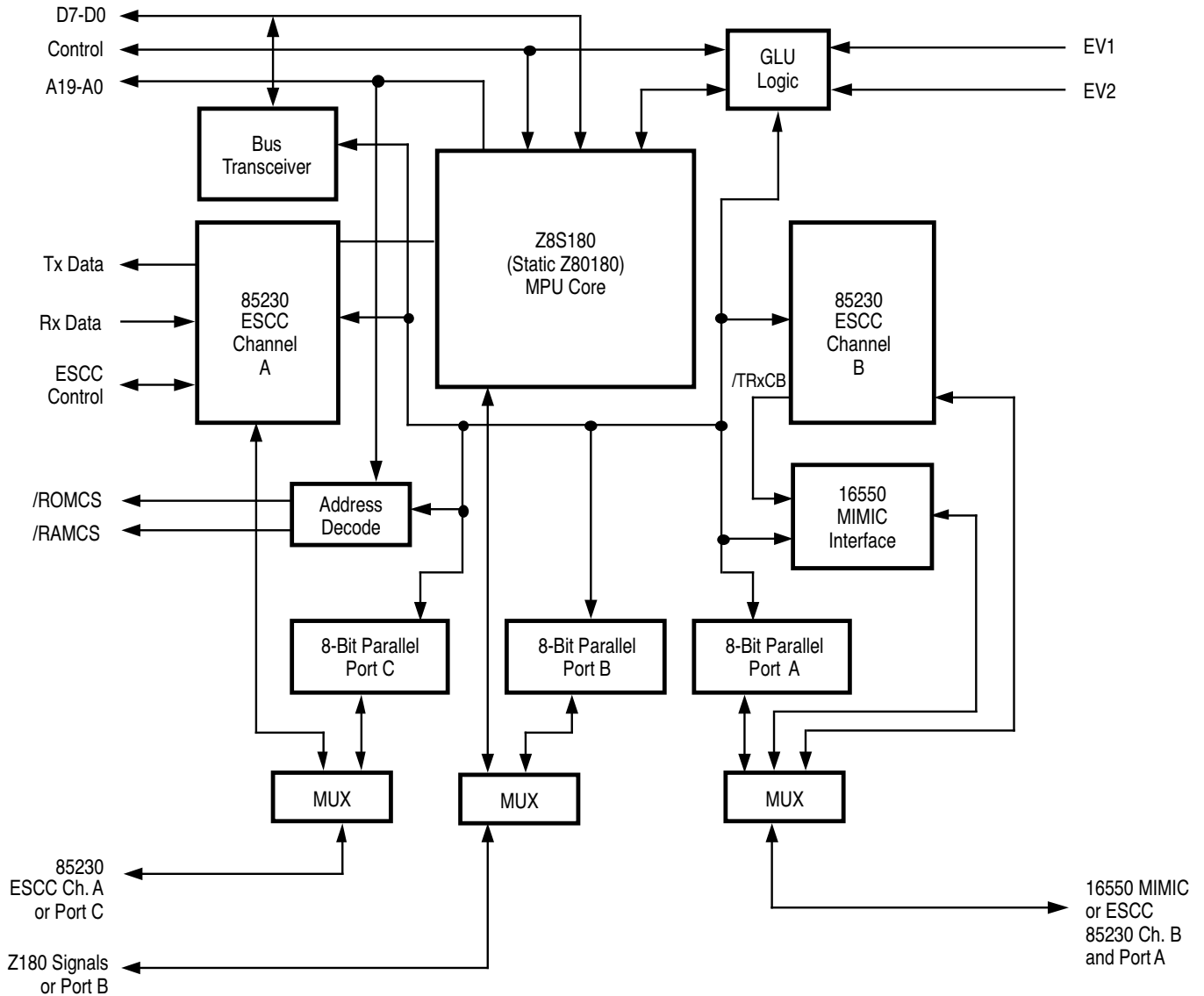
#### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	$V_{CC}$	$V_{DD}$
Ground	GND	$V_{SS}$

GENERAL DESCRIPTION (Continued)



**Note:** Conventional use of the term "MPU side" refers to all interface through the Z180 MPU core and "PC side" refers to all interface through the 16550 MIMIC interface.

**Figure 1. Z80182/Z8L182 Functional Block Diagram**

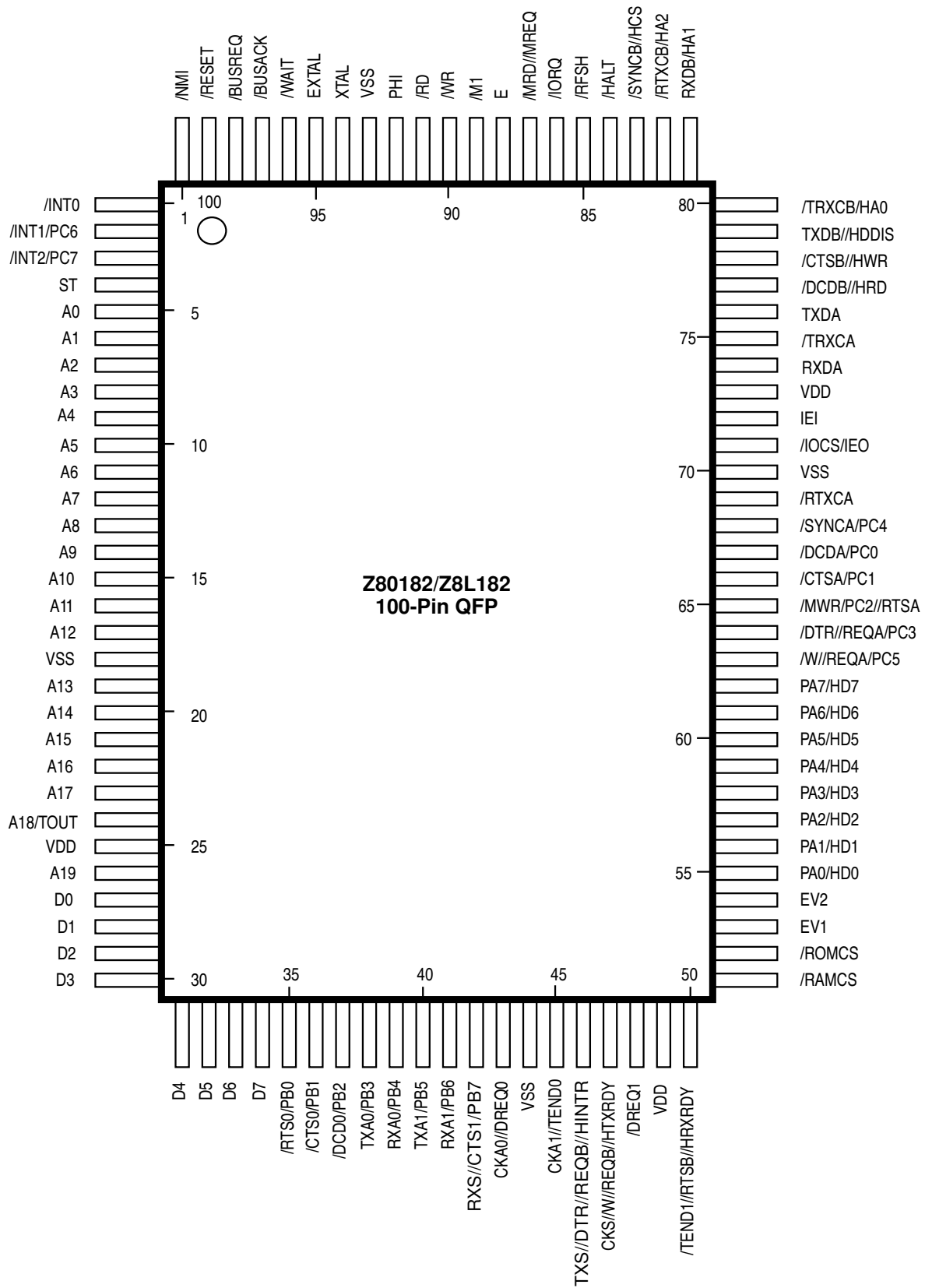
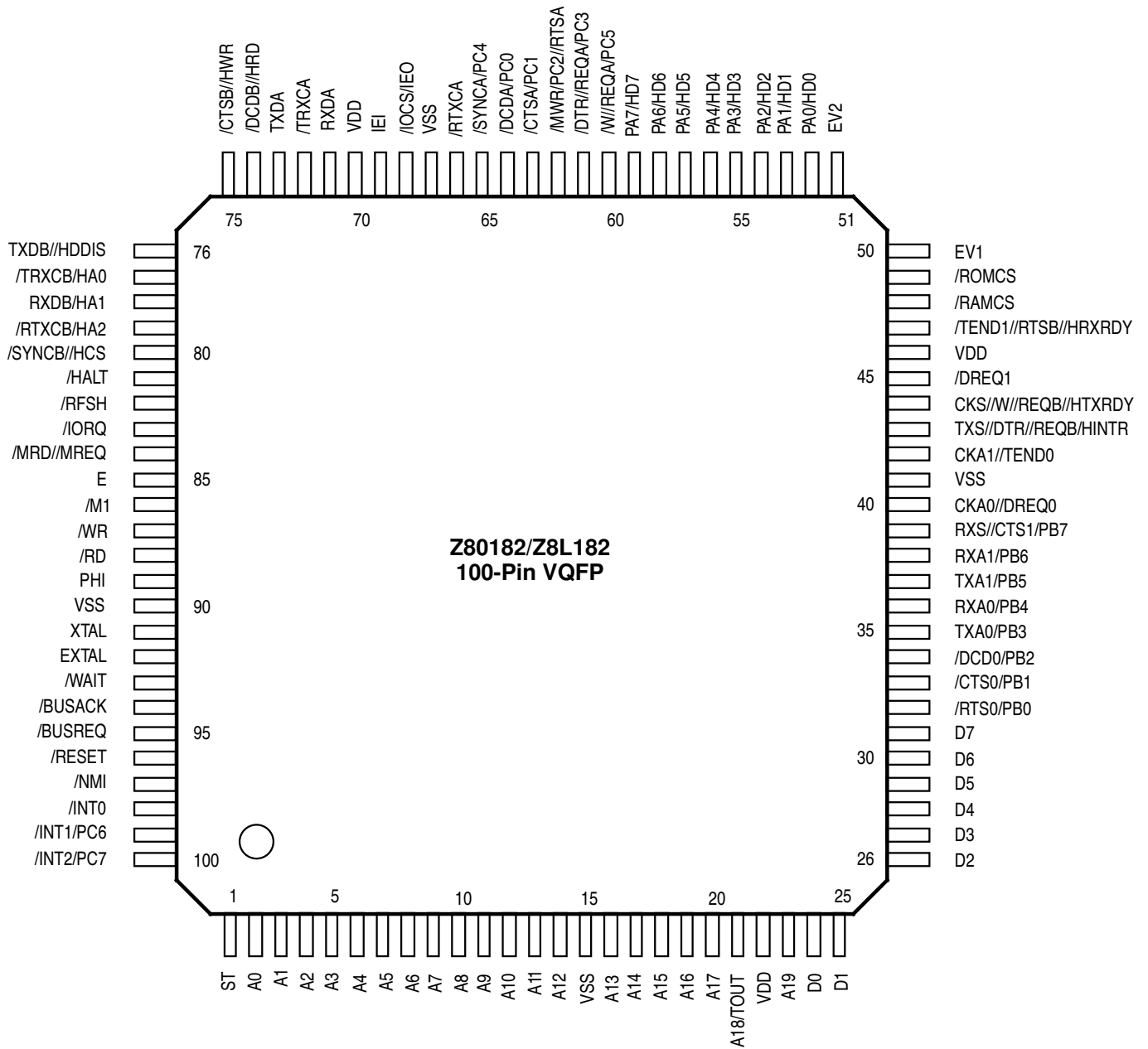


Figure 2. Z80182/Z8L182 100-Pin QFP Pin Configuration

**GENERAL DESCRIPTION** (Continued)



**Figure 3. Z80182/Z8L182 100-Pin VQFP Pin Configuration**

## Z180 CPU SIGNALS

**A19-A0.** *Address Bus (input/output, active High, tri-state).* A19-A0 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges up to 1 Mbyte, and I/O data bus exchanges up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states. This bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT channel 1 ( $T_{OUT}$ , selected as address output on reset).

**D7-D0.** *Data Bus (bi-directional, active High, tri-state).* D7-D0 constitute an 8-bit bi-directional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

**/RD.** *Read (input/output, active Low, tri-state).* /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

**/WR.** *Write (input/output, active Low, tri-state).* /WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

**/IORQ.** *I/O Request (input/output, active Low, tri-state).* /IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. /IORQ is also generated, along with /M1, during the acknowledgment of the /INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

**/M1.** *Machine Cycle 1 (input/output, active Low).* Together with /MREQ, /M1 indicates that the current cycle is the opcode fetch cycle of an instruction execution; unless /M1E bit in the OMCR is cleared to 0. Together with /IORQ, /M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the /HALT and ST signals to decode status of the CPU machine cycle. This signal is analogous to the /LIR signal of the Z64180.

**/MREQ.** *Memory Request (input/output, active Low, tri-state).* /MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the /ME signal of the Z64180. /MREQ is multiplexed with /MRD on the /MRD//MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if the /MREQ function is selected; and is inactive High if /MRD function is selected.

**/MRD.** *Memory Read (input/output, active Low, tri-state).* /MRD is active when both the internal /MREQ and /RD are active. /MRD is multiplexed with /MREQ on the /MRD //MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if /MREQ function is selected; and is inactive High if /MRD function is selected. The default function on power up is /MRD and may be changed by programming bit 3 of the Interrupt Edge/Pin MUX Register (xxDFH).

**/MWR.** *Memory Write (input/output, active Low, tri-state).* /MWR is active when both the internal /MREQ and /WR are active. This /RTSA or PC2 combination is pin multiplexed with /MWR on the /MWR/PC2//RTSA pin. The default function of this pin on power up is /MWR, which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

**/WAIT.** *(input/output active Low).* /WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The /WAIT input is sampled on the falling edge of T2 (and subsequent wait states). If the input is sampled Low, then additional wait states are inserted until the /WAIT input is sampled High, at which time execution will continue.

**/HALT.** *Halt/Sleep Status (input/output, active Low).* This output is asserted after the CPU has executed either the HALT or SLEEP instruction, and is waiting for either non-maskable or maskable interrupts before operation can resume. It is also used with the /M1 and ST signals to decode status of the CPU machine cycle. On exit of HALT/SLEEP mode, the first instruction fetch can be delayed by 16 clock cycles after the /HALT pin goes High, if HALT 16 feature is selected.

**/BUSACK.** *Bus Acknowledge (input/output, active Low).* /BUSACK indicates to the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

**/BUSREQ.** *Bus Request (input, active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address/data buses and other control signals, into the high impedance state.

## Z180 CPU SIGNALS (Continued)

**/NMI.** *Non-maskable interrupt (input, negative edge triggered).* /NMI has a higher priority than /INT and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.

**/INT0.** *Maskable Interrupt Request 0 (input/output active Low).* This signal is generated by external I/O devices. The CPU will honor this request at the end of the current instruction cycle as long as the /NMI and /BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the /M1 and /IORQ signals become active. The internal Z180 MPU's /INT0 source is: /INT0 or ESCC or the MIMIC. This input is level triggered. /INT0 is an open-drain output, so you can connect other open-drain interrupts onto the circuit in addition to having a pull-up to VCC.

**/INT1, /INT2.** *Maskable Interrupt Requests 1 and 2 (inputs, active Low).* This signal is generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the /NMI, /BUSREQ, and /INT0 signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for /INT0, during this cycle neither the /M1 or /IORQ signals become active. These pins may be programmed to provide an active Low level on rising or falling edge interrupts. The level of the external /INT1 and /INT2 pins may be read through bits PC6 and PC7 of parallel Port C. Pin /INT1/PC6 multiplexes /INT1 and PC6. Pin /INT2/PC7 multiplexes /INT2 and PC7.

**/RFSH.** *Refresh (input/output, active Low, tri-state).* Together with /MREQ, /RFSH indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7-A0) contain the refresh address. This signal is analogous to the /REF signal of the Z64180.

## Z180 MPU UART AND SIO SIGNALS

**CKA0, CKA1.** *Asynchronous Clocks 0 and 1 (bi-directional, active High).* These pins are the transmit and receive clocks for the synchronous channels. CKA0 is multiplexed with /DREQ0 on the CKA0//DREQ0 pin. CKA1 is multiplexed with /TEND0 on the CKA1//TEND0 pin.

**CKS.** *Serial Clock (bi-directional, active High).* This line is clock for the CSIO channel and is multiplexed with the ESCC signal (/W//REQB) and the 16550 MIMIC interface signal /HTxRDY on the CKS//W//REQB//HTxRDY pin.

**/DCD0.** *Data Carrier Detect 0 (input, active Low).* This is a programmable modem control signal for ASCII channel 0. /DCD0 is multiplexed with the PB2 (parallel Port B, bit 2) on the /DCD0/PB2 pin.

**/RTS0.** *Request to Send 0 (output, active Low).* This is a programmable modem control signal for ASCII channel 0. This pin is multiplexed with PB0 (parallel Port B, bit 0) on the /RTS0/PB0 pin.

**/CTS0.** *Clear to Send 0 (input, active Low).* This line is a modem control signal for the ASCII channel 0. This pin is multiplexed with PB1 (parallel Port B, bit 1) on the /CTS0/PB1 pin.

**TxA0.** *Transmit Data 0 (output, active High).* This signal is the transmitted data from the ASCII channel 0. This pin is multiplexed with PB3 (parallel Port B, bit 3) on the TxA0/PB3 pin.

**TxS.** *Clocked Serial Transmit Data (output, active High).* This line is the transmitted data from the CSIO channel. TxS is multiplexed with the ESCC signal (/DTR//REQB) and the 16550 MIMIC interface signal HINTR on the TxS//DTR//REQB//HINTR pin.

**RxA0.** *Receive Data 0 (input, active High).* This signal is the receive data to ASCII channel 0. This pin is multiplexed with PB4 (parallel Port B, bit 4) on the RxA0/PB4.

**RxS.** *Clocked Serial Receive Data (input, active High).* This line is the receive data for the CSIO channel. RxS is multiplexed with the /CTS1 signal for ASCII channel 1 and with PB7 (parallel Port B, bit 7) on the RxS//CTS1/PB7 pin.

**RxA1.** *Received Data ASCII channel 1 (input, active High).* This pin is multiplexed with PB6 (parallel Port B, bit 6) on the RxA1/PB6 pin.

**TxA1.** *Transmitted Data ASCII Channel 1 (output, active High).* This pin is multiplexed with PB5 (parallel Port B, bit 5) on the TxA1/PB5 pin.

## Z180 MPU DMA SIGNALS

**/TEND0.** *Transfer End 0 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND0 is multiplexed with CKA1 on the CKA1//TEND0 pin.

**/TEND1.** *Transfer End 1 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND1 is multiplexed with the ESCC signal /RTSB and the 16550 MIMIC interface signal /HRxRDY on the /TEND1//RTSB//HRxRDY pin.

**/DREQ0.** *DMA request 0 (input, active Low).* /DREQ0 is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. /DREQ0 is multiplexed with CKA0 on the CKA0//DREQ0 pin.

**/DREQ1.** *DMA request 1 (input, active Low).* /DREQ1 is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

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## Z180™ MPU TIMER SIGNALS

**T<sub>OUT</sub>.** *Timer Out (output, active High).* T<sub>OUT</sub> is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/T<sub>OUT</sub> pin.

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## Z85230 ESCC™ SIGNALS

**TxDA.** *Transmit Data (output, active High).* This output signal transmits channel A's serial data at standard TTL levels. This output can be tri-stated during power down modes.

**TxDB.** *Transmit Data (output, active High).* This output signal transmits channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface /HDDIS signal on the TxDB//HDDIS pin.

**RxDA.** *Receive Data (inputs, active High).* These inputs receive channel A's serial data at standard TTL levels.

**RxDB.** *Receive Data (input, active High).* These inputs receive channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB//HA1 pin.

**/TRxCA.** *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel A program control. /TRxCA may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

**/TRxCB.** *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel B program

control. /TRxCB may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in output mode. In Z80182/Z8L182 mode 1 /TRxCB is multiplexed with the 16550 MIMIC interface HA0 input on the /TRxCB//HA0 pin.

**/RTxCA.** *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel A program control. In channel A, /RTxCA may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCA pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

**/RTxCB.** *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel B program control. In channel B, /RTxCB may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCB pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182/Z8L182 mode 1 the /RTxCB signal is multiplexed with 16550 MIMIC interface HA2 input on the /RTxCB//HA2 pin.



**Z85230 ESCC SIGNALS** (Continued)

**/SYNCA, /SYNCB.** *Synchronization (inputs/outputs, active Low).* These pins can act as either inputs, outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to /CTS and /DCD. In this mode, transitions on these lines affect the state of the Sync /Hunt status bits in Read Register 0, but have no other function. /SYNCA is also multiplexed with PC4 (parallel Port C, bit 4) on the /SYNCA/PC4 pin.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode /SYNC must be driven Low two receive clock cycles after the last bit in the sync character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.

In the Internal Synchronization mode, (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync character is recognized (regardless of the character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. In Z80182/Z8L182 mode 1 the /SYNCB signal is multiplexed with the 16550 MIMIC interface /HCS input on the /SYNCB //HCS pin.

**/CTSA.** *Clear To Send (input, active Low).* If this pin is programmed as auto enable, a Low on this input enables the channel A transmitter. If not programmed as auto enable, it may be used as a general-purpose input. The input is Schmitt-trigger buffered to accommodate slow rise-time input. The ESCC™ detects transitions on this input and can interrupt the Z180™ MPU on either logic level transitions. /CTSA is multiplexed with PC1 (parallel Port C, bit 1) on the /CTSA/PC1 pin.

**/CTSB.** *Clear To Send (input, active Low).* This pin is similar to /CTSA's functionality but is applicable to the channel B transmitter. In Z80182/Z8L182 mode, the /CTSB signal is multiplexed with the 16550 MIMIC interface /HWR input on the /CTSB //HWR pin.

**/DCDA.** *Data Carrier Detect (input, active Low).* This pin functions as receiver enables if it is programmed as an auto enable bit; otherwise, it may be used as a general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects transitions on this pin and can interrupt the Z180 MPU on either logic level transitions. /DCDA is also multiplexed with PC0 (parallel Port C, bit 0) on the /DCDA/PC0 pin.

**/DCDB.** *Data Carrier Detect (input, active Low).* This pin's functionality is similar to /DCDA but applicable to the channel B receiver. In Z80182/Z8L182 mode 1, /DCDB is multiplexed with the 16550 MIMIC interface /HRD input on the /DCDB//HRD pin.

**/RTSA.** *Request to Send (output, active Low).* When the Request to Send (RTS) bit in Write Register 5 channel A is set, the /RTSA signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with auto enables off, the /RTSA pin strictly follows the state of the RTS bit. The pin can be used as general-purpose output. /RTSA is multiplexed with PC2 (parallel Port C bit 2). This /RTSA or PC2 combination is pin multiplexed with /MWR (active when both the internal /MREQ and /WR are active) on the /MWR/PC2//RTSA pin. The default function of this pin on power-up is /MWR which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

**/RTSB.** *Request to Send (output, active Low).* This pin is similar in functionality as /RTSA but is applicable on channel B. The /RTSB signal is multiplexed with the Z180 MPU /TEND1 signal and the 16550 MIMIC interface /HRxRDY signal on the /TEND1//RTSB//HRxRDY pin.

**/DTR//REQA.** *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. /DTR//REQA is also multiplexed with PC3 (parallel Port C, bit 3) on the /DTR//REQA /PC3 pin.

**/DTR//REQB.** *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. The /DTR//REQB signal is multiplexed with the Z180 MPU TxS signal and the 16550 MIMIC interface HINTR signal on the /TxS//DTR//REQB //HINTR pin.

**/W//REQA.** *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This dual-purpose output can be programmed as Request (receive) lines for a DMA controller or as Wait lines to synchronize the Z180 MPU to the ESCC data rate. The reset state is Wait. The ESCC allows full duplex DMA transfers. /W//REQA is also multiplexed with PC5 (parallel Port C, bit 5) on the /W//REQA/PC5 pin.

**/W//REQB.** *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on

channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

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## 16550 MIMIC INTERFACE SIGNALS

**HD7-HD0.** *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

**/HDDIS.** *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

**HA2-HA0.** *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

**/HCS.** *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

**/HWR.** *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

**/HRD.** *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

**HINTR.** *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

**/HTxRDY.** *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

**/HRxRDY.** *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

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## PARALLEL PORTS

**PA7-PA0.** *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

**PB7-PB0.** *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

**PC7-PC0.** *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

## EMULATION SIGNALS

**EV1, EV2.** *Emulation Select (input).* These two pins determine the emulation mode of the Z180 MPU (Table 1).

**Table 1. Evaluation Modes**

Mode	EV2	EV1	Description
0	0	0	Normal mode, on-chip Z180 bus master
1	0	1	Emulation Adapter Mode
2	1	0	Emulator Probe Mode
3	1	1	Reserved for Test

## SYSTEM CONTROL SIGNALS

**ST.** *Status (output, active High).* This signal is used with the /M1 and /HALT output to decode the status of the CPU machine cycle. If unused, this pin should be pulled to  $V_{DD}$ .

**/RESET.** *Reset Signal (input, active Low).* /RESET signal is used for initializing the MPU and other devices in the system. It must be kept in the active state for a period of at least three system clock cycles.

**IEI.** *Interrupt Enable Signal (input, active High).* IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.

**IEO.** *Interrupt Enable Output Signal (output, active High).* In the daisy-chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is 1 and the CPU is not servicing an interrupt from the on-chip peripherals. This pin is multiplexed with /IOCS on the /IOCS/IEO pin. The /IOCS function is the default on Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

**/IOCS.** *Auxiliary Chip Select Output Signal (output, active Low).* This pin is multiplexed with /IEO on the /IOCS/IEO pin. /IOCS is an auxiliary chip select that decodes A7, A6, /IORQ, /M1 and effectively decodes the address space xx80H to xxBFH for I/O transactions. A15 through A8 are not decoded so that the chip select is active in all pages of I/O address space. The /IOCS function is the default on the /IOCS/IEO pin after Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

**/RAMCS.** *RAM Chip Select (output, active Low).* Signal used to access RAM based upon the Address and the RAMLBR and RAMUBR registers and /MREQ.

**/ROMCS.** *ROM Chip Select (output, active Low).* Signal used to access ROM based upon the address and the ROMBR register and /MREQ.

**E.** *Enable Clock (output, active High).* Synchronous machine cycle clock output during bus transactions.

**XTAL.** *Crystal (input, active High).* Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

**EXTAL.** *External Clock/Crystal (input, active High).* Crystal oscillator connections to an external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

**PHI.** *System Clock (output, active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is reflective of the functional speed of the processor. In clock divide-by-two mode, the PHI frequency is half that of the crystal or input clock. If divide-by-one mode is enabled, the PHI frequency is equivalent to that of crystal or input frequency. The PHI frequency is also fed to the ESCC core. If running over 20 MHz (5V) or 10 MHz (3V) the PHI-ESCC frequency divider should be enabled to divide the PHI clock by two prior to feeding into the ESCC core.

## MULTIPLEXED PIN DESCRIPTIONS

**A18/T<sub>OUT</sub>**. During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, The T<sub>OUT</sub> function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/T<sub>OUT</sub>. Therefore, the selection of T<sub>OUT</sub> will not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

**CKA0//DREQ0**. During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, /DREQ0 function is always selected.

**CKA1//TEND0**. During Reset, this pin is initialized as CKA1 pin. If CKA1D bit in the ASCI control register Ch1(CNTLA1) is set to 1, /TEND0 function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

**RxS//CTS1**. During Reset, this pin is initialized as the RxS pin. If CTS1E bit in the ASCI status register Ch1 (STAT1) is set to 1, /CTS1 function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 2 specifies. On Reset, both bits 1 and 2 are 0, so /TEND1,TxS,CKS are selected.

**Table 2. Triple Multiplexed Pins**

Bit 1	Bit 2	Master Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/RTSB,/DTR//REQB,/W//REQB
1	0	/TEND1,TxS,CKS
1	1	/HRxRDY,//HTxRDY,HINTR

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is 0, then the Z80182/Z8L182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is 1, then Z80182/Z8L182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182/Z8L182 Mode 0 is always selected as shown in Table 3.

**Table 3. Mode 0 and Mode 1 Multiplexed Pins**

Z80182/Z8L182 Mode 0	Z80182/Z8L182 Mode 1
TxDB	/HDDIS
RxDB	HA1
/TRxCB	HA0
/RTxCB	HA2
/SYNCB	/HCS
/CTSB	/HWR
/DCDB	/HRD
PA7-PA0	HD7-HD0

## Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 4.

**Table 4. Multiplexed Port Pins**

Port Mode Function	ASCI/ESCC Mode Function
PB7	RxS,/CTS1
PB6 Select with bit 6=1	RxA1
PB5 System Config Reg.	TxA1
PB4	RxA0
PB3	TxA0
PB2 Select with bit 5=1	/DCD0
PB1 System Config Reg.	/CTS0 (Note 1)
PB0	/RTS0
PC7	Always Reads /INT2 Ext. Status
PC6	Always Reads /INT1 Ext. Status
PC5	/W//REQA
PC4	/SYNCA
PC3 Select with bit 7=1	/DTR//REQA
PC2 System Config Reg.	/RTSA (Note 2)
PC1	/CTSA
PC0	/DCDA

**Note 1:**

When the Port function (PB1) is selected, the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

**Note 2:**

Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functions.

Table 5. Primary, Secondary and Tertiary Pin Functions

Pin Number	1st Function	2nd Function	3rd Function	MUX Control
VQFP	QFP			
1	4	ST		
2	5	A0		
3	6	A1		
4	7	A2		
5	8	A3		
6	9	A4		
7	10	A5		
8	11	A6		
9	12	A7		
10	13	A8		
11	14	A9		
12	15	A10		
13	16	A11		
14	17	A12		
15	18	V <sub>SS</sub>		
16	19	A13		
17	20	A14		
18	21	A15		
19	22	A16		
20	23	A17		
21	24	A18/T <sub>OUT</sub>		
22	25	V <sub>DD</sub>		
23	26	A19		
24	27	D0		
25	28	D1		
26	29	D2		
27	30	D3		
28	31	D4		
29	32	D5		
30	33	D6		
31	34	D7		
32	35	/RTS0	PB0	SYS CONF REG Bit 5
33	36	/CTS0	PB1	SYS CONF REG Bit 5
34	37	/DCD0	PB2	SYS CONF REG Bit 5
35	38	TxA0	PB3	SYS CONF REG Bit 5
36	39	RxA0	PB4	SYS CONF REG Bit 5
37	40	TxA1	PB5	SYS CONF REG Bit 6
38	41	RxA1	PB6	SYS CONF REG Bit 6
39	42	RxS//CTS1	PB7	SYS CONF REG Bit 6
40	43	CKA0//DREQ0		

**MULTIPLEXED PIN DESCRIPTIONS** (Continued)**Table 5. Primary, Secondary and Tertiary Pin Functions** (Continued)

Pin Number	1st Function	2nd Function	3rd Function	MUX Control
VQFP	QFP			
41	44	V <sub>SS</sub>		
42	45	CKA1//TEND0		
43	46	TxS	/DTR//REQB	HINTR
44	47	CKS	/W//REQB	/HTxRDY
45	48	/DREQ1		
46	49	V <sub>DD</sub>		
47	50	/TEND1	/RTSB	/HRxRDY
48	51	/RAMCS		
49	52	/ROMCS		
50	53	EV1		
51	54	EV2		
52	55	PA0	HD0	
53	56	PA1	HD1	
54	57	PA2	HD2	
55	58	PA3	HD3	
56	59	PA4	HD4	
57	60	PA5	HD5	
58	61	PA6	HD6	
59	62	PA7	HD7	
60	63	/W//REQA	PC5	
61	64	/DTR//REQA	PC3	
62	65	/MWR	PC2	RTSA
63	66	/CTSA	PC1	
64	67	/DCDA	PC0	
65	68	/SYNCA	PC4	
66	69	/RTxCA		
67	70	V <sub>SS</sub>		
68	71	/IOCS	IEO	
69	72	IEI		
70	73	V <sub>DD</sub>		

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number	1st Function	2nd Function	3rd Function	MUX Control
VQFP	QFP			
71	74	RxDA		
72	75	/TRxCA		
73	76	TxDA		
74	77	/DCDB	/HRD	SYS CONF REG Bit 1
75	78	/CTSB	/HWR	SYS CONF REG Bit 1
76	79	TxDB	/HDDIS	SYS CONF REG Bit 1
77	80	/TRxCB	HA0	SYS CONF REG Bit 1
78	81	RxDB	HA1	SYS CONF REG Bit 1
79	82	/RTxCB	HA2	SYS CONF REG Bit 1
80	83	/SYNCB	/HCS	SYS CONF REG Bit 1
81	84	/HALT		
82	85	/RFSH		
83	86	/IORQ		
84	87	/MRD	/MREQ	INT EDG/PIN REG Bit 3
85	88	E		
86	89	/M1		
87	90	/WR		
88	91	/RD		
89	92	PHI		
90	93	V <sub>ss</sub>		
91	94	XTAL		
92	95	EXTAL		
93	96	/WAIT		
94	97	/BUSACK		
95	98	/BUSREQ		
96	99	/RESET		
97	100	/NMI		
98	1	/INT0		
99	2	/INT1	PC6**	
100	3	/INT2	PC7**	

**Notes:**

\* Also controlled by Interrupt Edge/Pin MUX Register

\*\* PC7 and PC6 are inputs only and can read values of /INT1 and /INT2.



### Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the

Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

### Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100%

software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

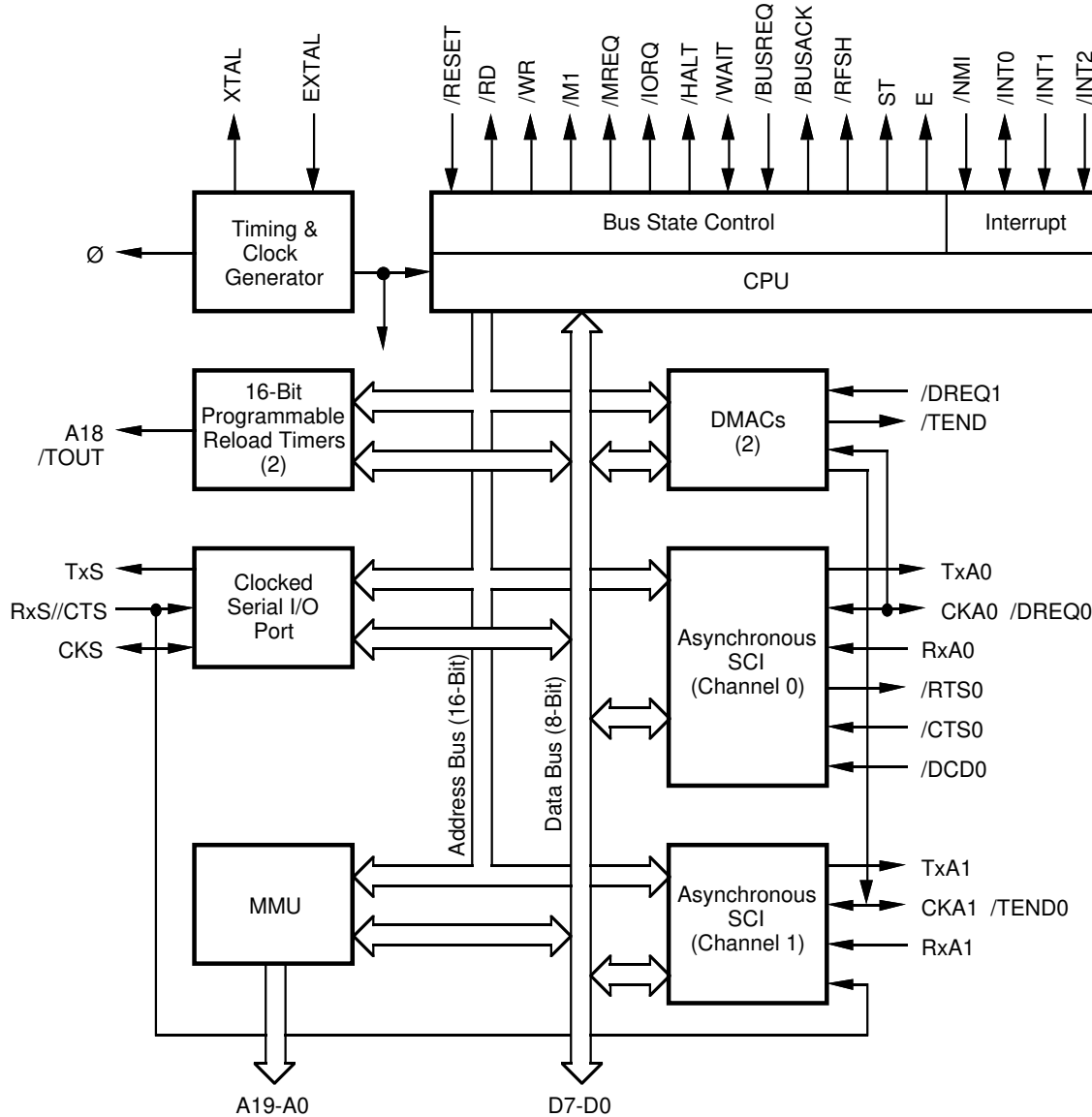


Figure 4. S180 MPU Block Diagram of Z182

**Z182 CPU**

The Z182 CPU is 100% software compatible with the Z80® CPU and has the following additional features:

**Faster Execution Speed.** The Z182 CPU is “fine tuned,” making execution speed, on average, 10% to 20% faster than the Z80 CPU.

**Enhanced DRAM Refresh Circuit.** Z182 CPU's DRAM refresh circuit does periodic refresh and generates an 8-bit refresh address. It can be disabled or the refresh period adjusted, through software control.

**Enhanced Instruction Set.** The Z182 CPU has seven additional instructions to those of the Z80 CPU, which include the MLT (Multiply) instruction.

**HALT and Low Power Modes of Operation.** The Z182 CPU has HALT and Low Power modes of operation, which are ideal for the applications requiring low power consumption like battery operated portable terminals.

**System Stop Mode.** When the Z182 is in System Stop mode, it is only the Z180 MPU that is in STOP mode.

**Standby and Idle Mode.** Please refer to the Z8S180 Product Specification for additional information on these two additional Low Power modes.

**Instruction Set.** The instruction set of the Z182 CPU is identical to the Z180. For more details about each transaction, please refer to the Product Specification/Technical Manual for the Z180/Z80 CPU.

**Z182 CPU Basic Operation**

Z182 CPU's basic operation consists of the following events. These are identical to the Z180 MPU. For more details about each operation, please refer to the Product Specification/Technical Manual for the Z180.

- Operation Code Fetch Cycle
- Memory Read/Write Operation
- Input/Output Operation
- Bus Request/Acknowledge Operation
- Maskable Interrupt Request Operation
- Trap and Non-Maskable Interrupt Request Operation
- HALT and Low Power Modes of Operation
- Reset Operation

**Memory Management Unit (MMU)**

The Memory Management Unit (MMU) allows the user to map the memory used by the CPU (64 Kbytes of logical addressing space) into 1 Mbyte of physical addressing space. The organization of the MMU allows object code compatibility with the Z80 CPU while offering access to an extended memory space. This is accomplished by using an effective common area-banked area scheme.

**DMA Controller**

The Z182 MPU has two DMA controllers. Each DMA controller provides high-speed data transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory-to/from-I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. The DMA can access the full 1 Mbytes addressing range with a block length up to 64 Kbytes and can cross over 64K boundaries.

**Asynchronous Serial Communication Interface (ASCI)**

This unit provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels also support a multiprocessor communication format.

**Programmable Reload Timer (PRT)**

The Z182 MPU has two separate Programmable Reload Timers, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is system clock divided by 20. PRT channel 1 provides an optional output to allow for waveform generation.

**Clocked Serial I/O (CSI/O)**

The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another CPU or MPU.

**Programmable Wait State Generator**

To ease interfacing with slow memory and I/O devices, the Z182 MPU unit has a programmable wait state generator. By programming the DMA/WAIT Control Register (DCNTL), up to three wait states are automatically inserted in memory and I/O cycles. This unit also inserts wait states during on-chip DMA transactions. When using RAMCS and ROMCS wait state generators, the wait state controller with the most programmed wait states will determine the number of wait states inserted.

## Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source
  - Up to 5 Mbits/sec at 20 MHz PCLK (ESCC).
- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit

- NRZ, NRZI or FM encoding/decoding. Manchester Code Decoding (Encoding with External Logic).
- Baud Rate Generator in each Channel
- Digital Phase-Locked Loop (DPLL) for Clock Recovery
- Crystal Oscillator

The following features are implemented in the ESCC™ for the Z80182/Z8L182 only:

- New 32-bit CRC-32 (Ethernet Polynomial)
- ESCC Programmable Clock
  - programmed to be equal to system clock divided by one or two
  - programmed by Z80182 Enhancement Register

**Note:** The ESCC™ programmable clock must be programmed to divide-by-two mode when operating above the following conditions:

- PHI > 20 MHz at 5.0V
- PHI > 10 MHz at 3.0V

### Z85230 ESCC™ BLOCK DIAGRAM

For a detailed description of the Z85230 ESCC, refer to the ESCC Technical Manual. The following figure is the block diagram of the discrete ESCC, which was integrated into the Z182. The /INT line is internally connected to "INTO of the Z182.

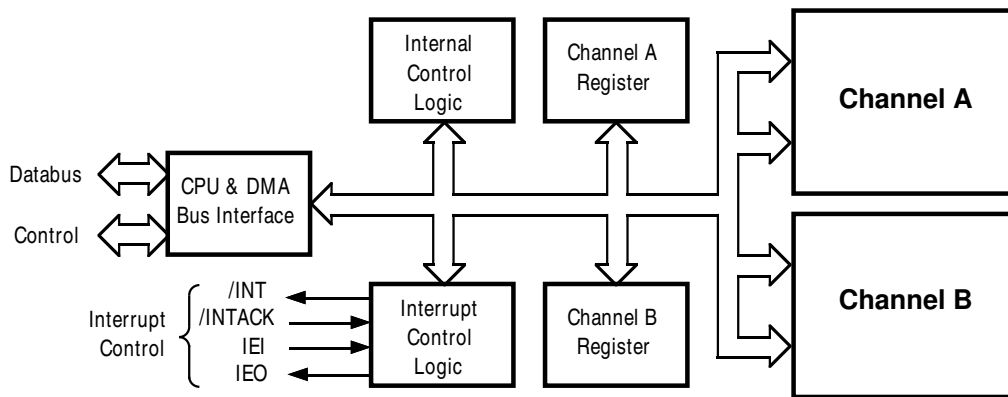
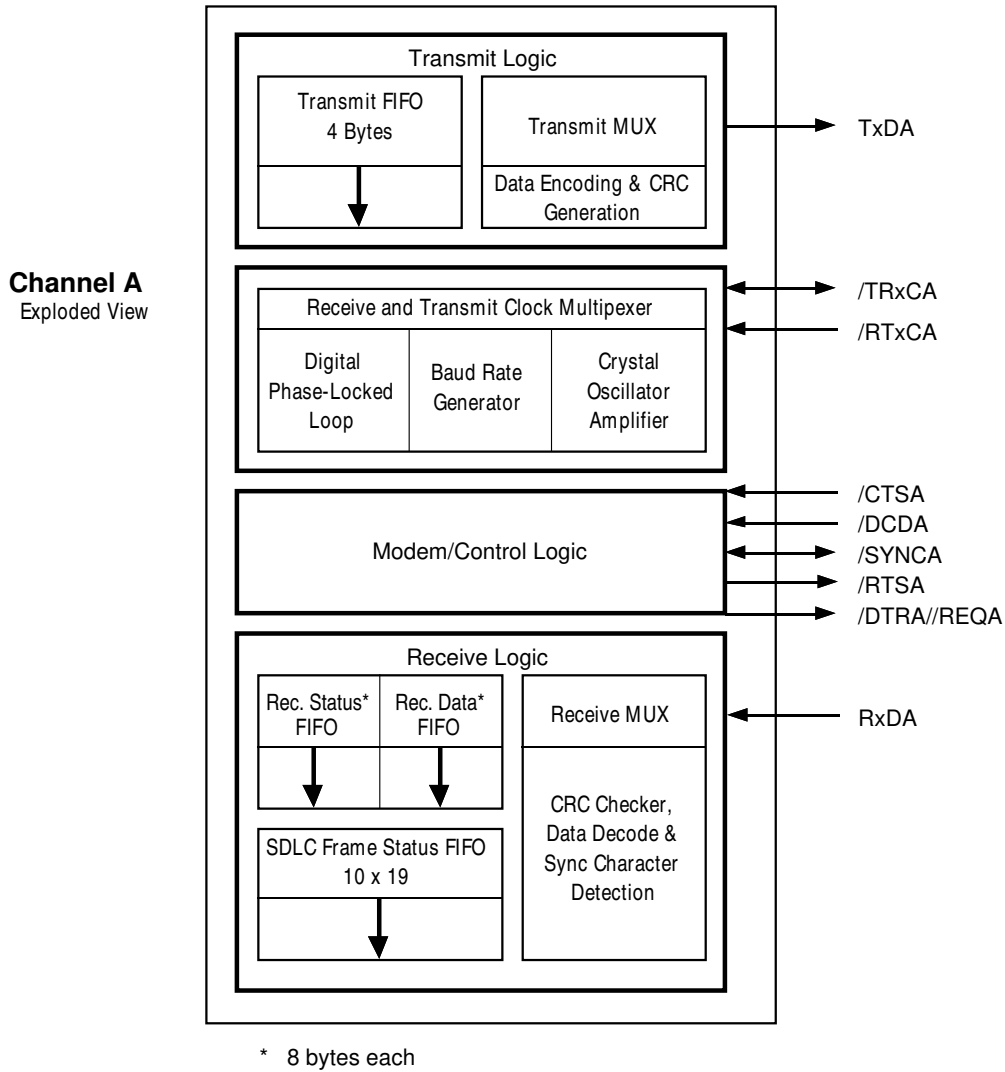


Figure 5. ESCC Block Diagram

## 16550 MIMIC INTERFACE FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has a 16550 MIMIC interface that allows it to mimic the 16550 device. It has all the interface pins necessary to connect to the PC/XT/AT bus. It contains the complete register set of the part with the same interrupt structure. The data path allows parallel transfer of data to and from the register set by the internal Z80180 of the Z80182/Z8L182. There is no shift register associated with the mimic of the 16550 UART. This interface saves the application from doing a serial transfer before performing data compression or error correction on the data.

Control of the register set is maintained by six priority encoded interrupts to the Z80182/Z8L182. When the PC/XT/AT writes to THR, MCR, LCR, DLL, DLM, FCR or reads the RBR, an interrupt to the Z80182/Z8L182 is generated. Each interrupt can be individually masked off or all interrupts can be disabled by writing a single bit. Both mode 0 and mode 2 interrupts are supported by the 16550 MIMIC interface.

Two eight-bit timers are also available to control the data transfer rate of the 16550 MIMIC interface. Their input is tied to the ESCC channel B divide clock, so a down count of 24 bits is possible. An additional two eight bit timers are available for programming the FIFO timeout feature (Four Character Time Emulation) for both Receive and Transmit FIFO's.

The 16550 MIMIC interface supports the PC/XT/AT interrupt structure as well as an additional mode that allows for a wired Logic AND interrupt structure.

The 16550 MIMIC interface is also capable of high speed parallel DMA transfers by using two control lines and the transmit and receive registers of the 16550 MIMIC interface.

All registers of the 16550 MIMIC interface are accessible in any page of I/O space since only the lowest eight address lines are decoded. See Figure 6 for a block diagram of the 16550 MIMIC interface.

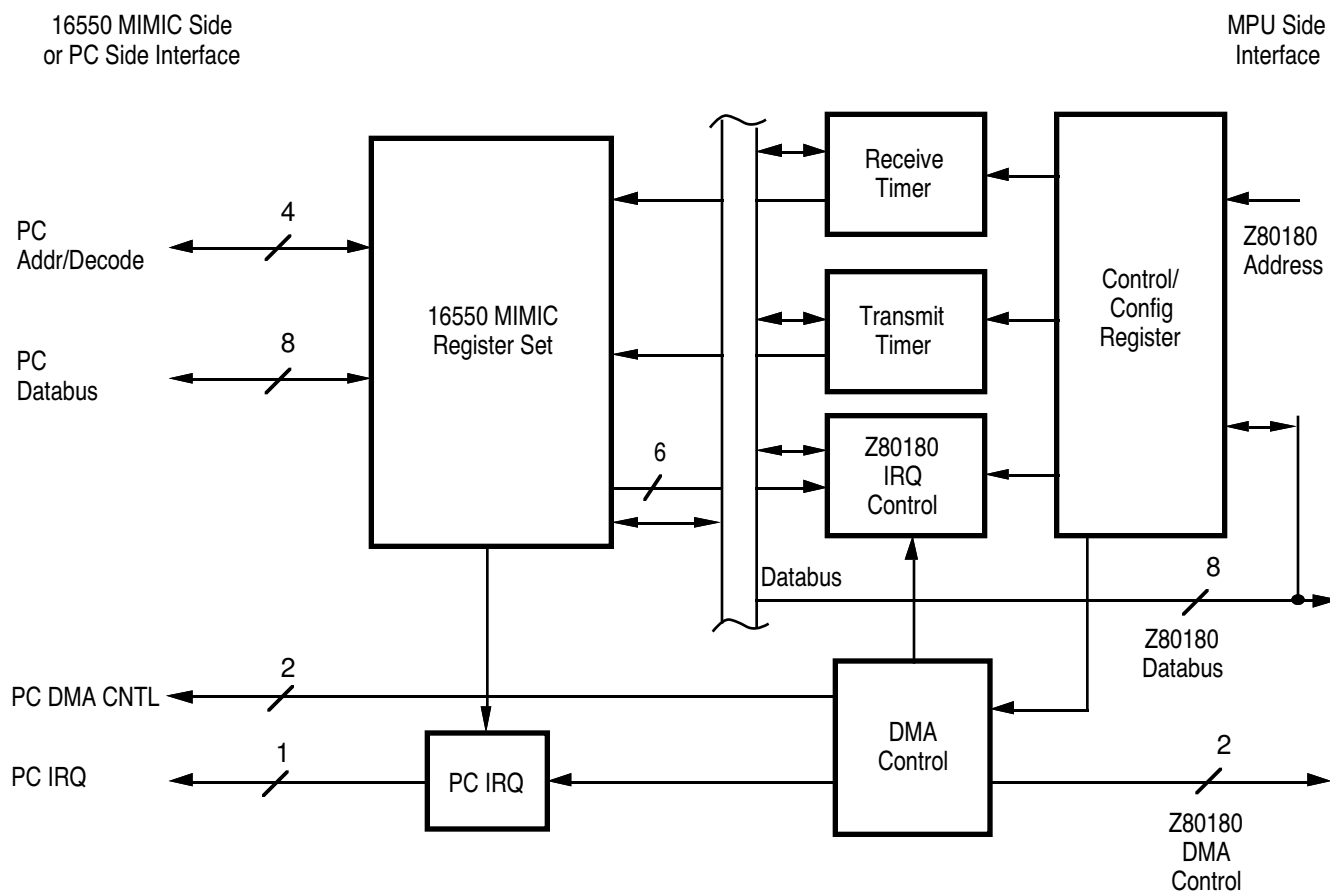


Figure 6. 16550 MIMIC Block Diagram

### 16550 MIMIC FIFO DESCRIPTION

The receiver FIFO consists of a 16-word FIFO capable of storing eight data bits and three error bits for each character stored (Figure 7). Parity error, Framing error and Break detect bits are stored along with the data bits by copying their value from three shadow bits that are Write Only bits for the Z80180 MPU LSR address. The three shadow bits are cleared after they are copied to the FIFO memory. In FIFO mode, to write error bits into the receiver FIFO, the MPU must first write the Parity, Framing and Break detect status to the Line Status Register (shadow bits) and then write the character associated into the receiver buffer. The data and error bits will then move into the same address in

the FIFO. The error bits become available to the PC side of the interface when that particular location becomes the next address to read (top of FIFO). At that time, they may either be read by the PC by accessing them in the LSR, or they may cause an interrupt to the PC interface if so enabled. The error bits are set by the error status of the byte at the top of the FIFO, but may only be cleared by reading the LSR. If successive reads of the receiver FIFO are performed without reading the LSR, the status bits will be set if any of the bytes read have the respective error bit set. See Table 6 for the setting and clearing of the Line Status Register bits.

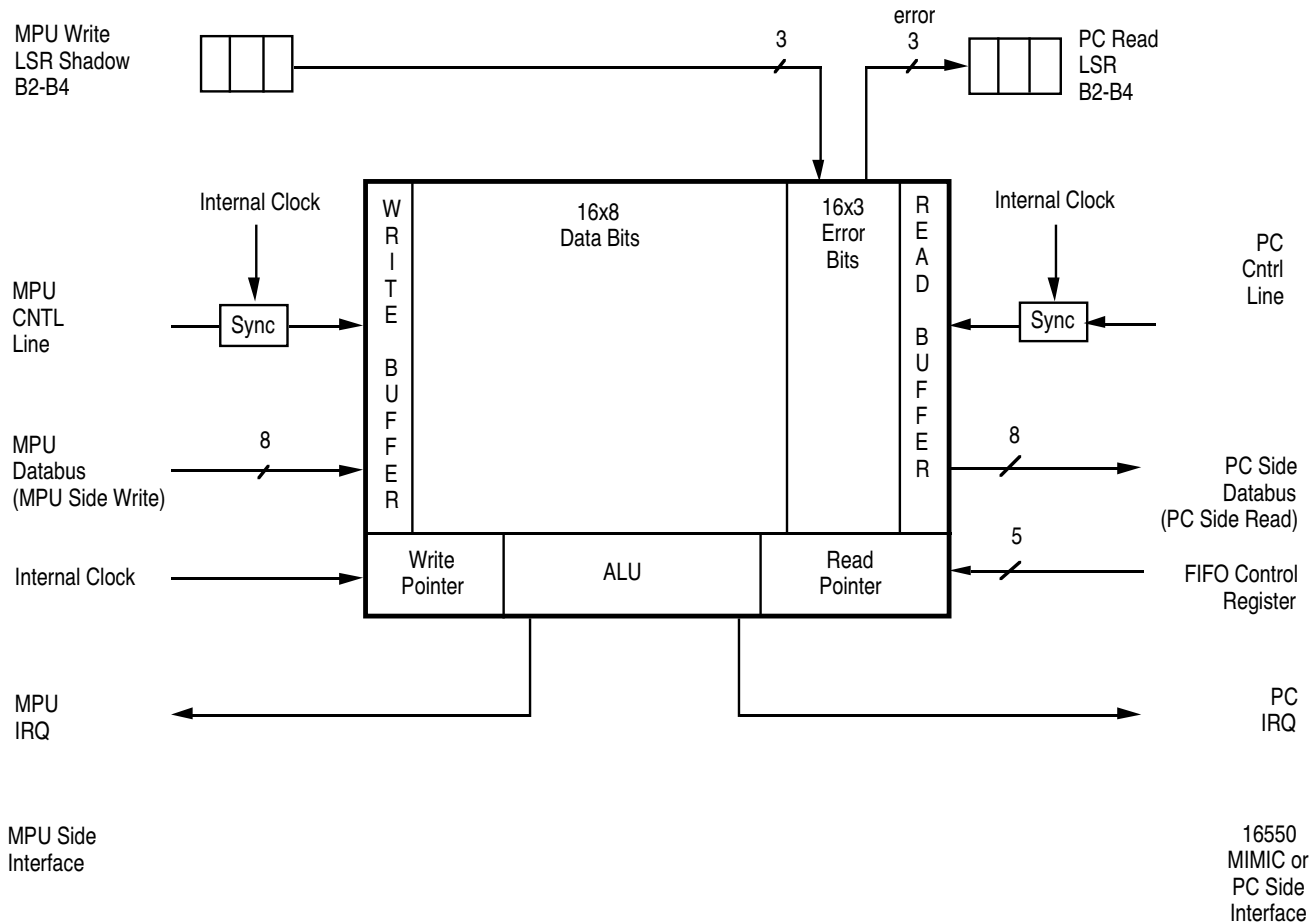


Figure 7. 16550 MIMIC Receiver FIFO Block Diagram

**Table 6. 16550 Line Status Register**

<b>Error</b>	<b>Description</b>	<b>How to Set</b>	<b>How to Clear</b>
Error in RCVR FIFO	At least one data byte available in FIFO with one error	At least one error in receiver FIFO	When there are no more errors
*TEMT	Transmitter empty	MPU writes a 1	MPU writes a 0
† *THRE	Transmitter holding register is empty	When MPU has read or emptied the holding register	When holding register is not empty
Break Detect	Break occurs when received data input is held in logic-0 for longer than a full word transmission	MPU writes 1	There is a PC-side read of the LSR
Framing Error	Received character did not have a valid stop bit	MPU writes 1	There is a PC-side read of the LSR
Parity Error	Received character did not have correct even or odd parity	MPU writes 1	There is a PC-side read of the LSR
Overrun Error	Overlapping received characters, thereby destroying the previous character	MPU makes two writes to receiver buffer register	There is a PC-side read of the LSR
†Data Ready	Indicates complete incoming data has been received	MPU writes to RCVR FIFO or receiver buffer register	Empty Receiver or Receiver FIFO

**Notes:**

- \* The TEMT and THRE bits take on different functions when TEMT/Double Buffer mode is enabled.
- † These signals are delayed to HOST when using character emulation delay.



**16550 MIMIC FIFO DESCRIPTION** (Continued)

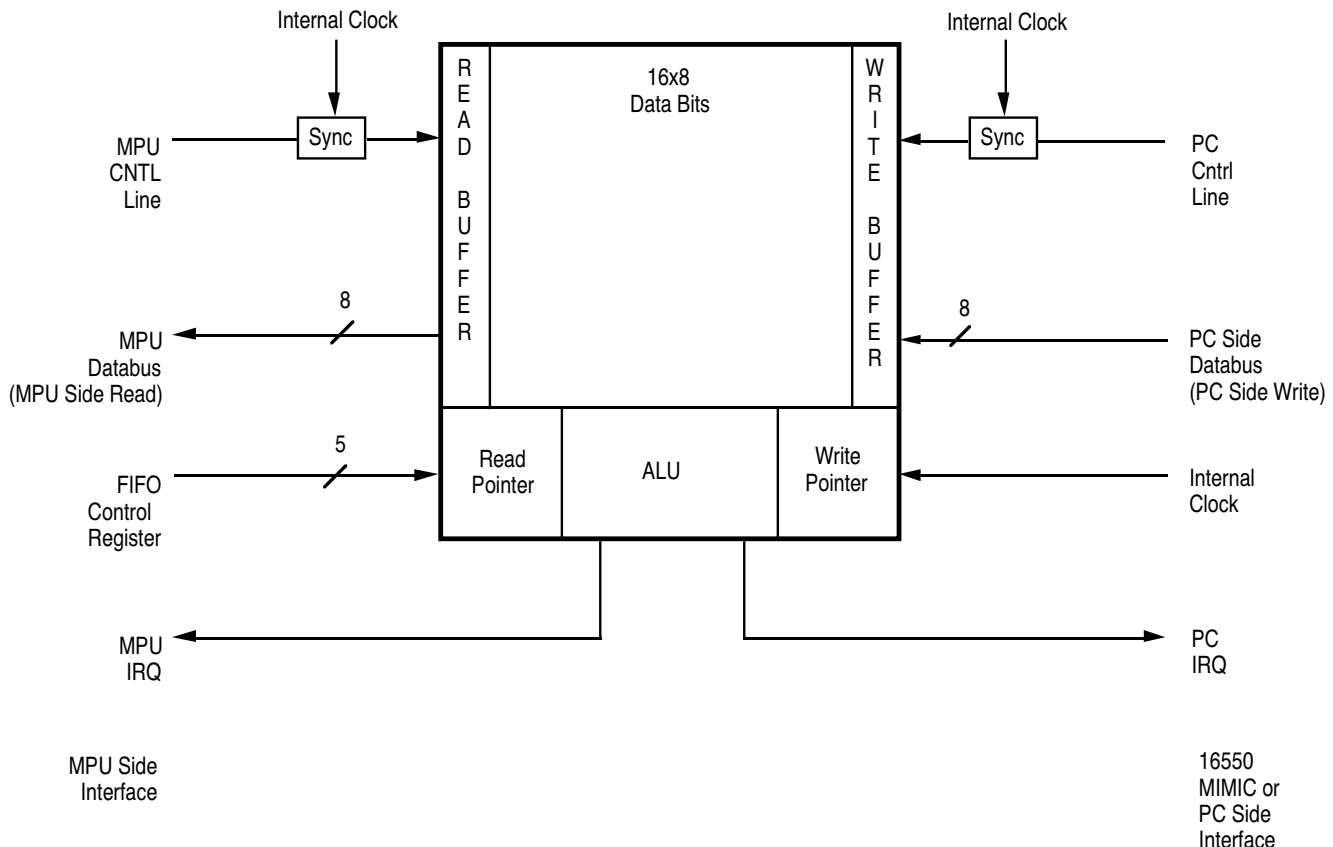
The PC interface may be interrupted when 1, 4, 8 or 14 bytes are available in the receiver FIFO by setting bits 6 and 7 in the FCR (FIFO Control Register, PC address 02H) to the appropriate value. If the FIFO is not empty, but below the above trigger value, a timeout interrupt is available if the receiver FIFO is not written by the MPU or read by the PC from an interval determined by the Character Timeout Timer. This is an additional Timer with MPU access only that is used to emulate the 16550 4 character timeout delay.

The Receive FIFO timeout timers are designed to reload and begin countdown after every read or write of the Rx FIFO, regardless of the Rx trigger level or number of bytes in the FIFO. Therefore, it is possible to get Timeout interrupts more often than Receive data interrupts. In order to closely emulate a 16550, a receive timeout timer enhancement is provided. When enabling this feature, the timeout timer will not begin counting down until the character emulation timer for each byte of data in the Rx FIFO has expired.  
**Note: Enabling this feature will facilitate increased 16550 compatibility but may impede throughput.** If the Receive Timeout interrupt occurs, the PC HOST will only be allowed to read up to 4-5 consecutive characters before the Data Ready bit is forced to zero (even if there is still more data in FIFO). This is required to maintain character pacing.

The timer receives the ESCC /TRxCB as its input clock. Software must determine the correct values to program into the Receiver Timeout register and the ESCC TRxCB to achieve the correct delay interval for timeout. These interrupts are cleared by the FIFO reaching the trigger point or by resetting the Timeout Interval Timer by FIFO MPU write or PC read access.

With FIFO mode enabled, the MPU is interrupted when the receiver FIFO is empty, corresponding to bit 5 being set in the IUS/IP register (MPU access only). This bit corresponds to a PC read of the receive buffer in non-FIFO (16450) mode. The interrupt source is cleared when the FIFO becomes non-empty or the MPU reads the IUS/IP register.

The transmitter FIFO is 16-byte FIFO with PC write and MPU read access (Figure 8). In FIFO mode, the PC receives an interrupt when the transmitter becomes empty corresponding to bit 5 being set in the LSR. This bit and the interrupt source are cleared when the transmit FIFO becomes non-empty or the Interrupt Identification Register (IIR) register is read by the PC.



**Figure 8. 16550 MIMIC Transmitter FIFO Block Diagram**

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer,

which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

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## Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.