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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Z80185/Z80195

SMART PERIPHERAL CONTROLLERS

FEATURES

Part	ROM (KB)	UART Baud Rate	Speed (MHz)
Z80185	32 x 8	512 KB	20, 33
Z80195	0	512 KB	20, 33

- 100-Pin QFP Package
- 5.0-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Temperature Range
- Enhanced Z8S180 MPU
- Four Z80 CTC Channels
- One Channel ESCC™ Controller
- Two 8-Bit Parallel I/O Ports
- Bidirectional Centronics Interface (IEEE 1284)
- Low-EMI Option

GENERAL DESCRIPTION

The Z80185 and Z80195 are smart peripheral controller devices designed for general data communications applications, and architected specifically to accommodate all input and output (I/O) requirements for serial and parallel connectivity. Combining a high-performance CPU core with a variety of system and I/O resources, the Z80185/195 are useful in a broad range of applications. The Z80195 is the ROMless version of the device.

The Z80185 and Z80195 feature an enhanced Z8S180 microprocessor linked with one enhanced channel of the Z85230 ESCC™ serial communications controller, and 25 bits of parallel I/O, allowing software code compatibility with existing software code.

Seventeen lines can be configured as bidirectional Centronics (IEEE 1284) controllers. When configured as a 1284 controller, an I/O line can operate in either the host or peripheral role in compatible, nibble, byte or ECP mode. In addition, the Z80185 includes 32 Kbytes of on-chip ROM.

These devices are well-suited for external modems using a parallel interface, protocol translators, and cost-effective WAN adapters. The Z80185/195 is ideal for handling all laser printer I/O, as well as the main processor in cost-effective printer applications.

Notes: All signals with a preceding front slash, "/", are active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

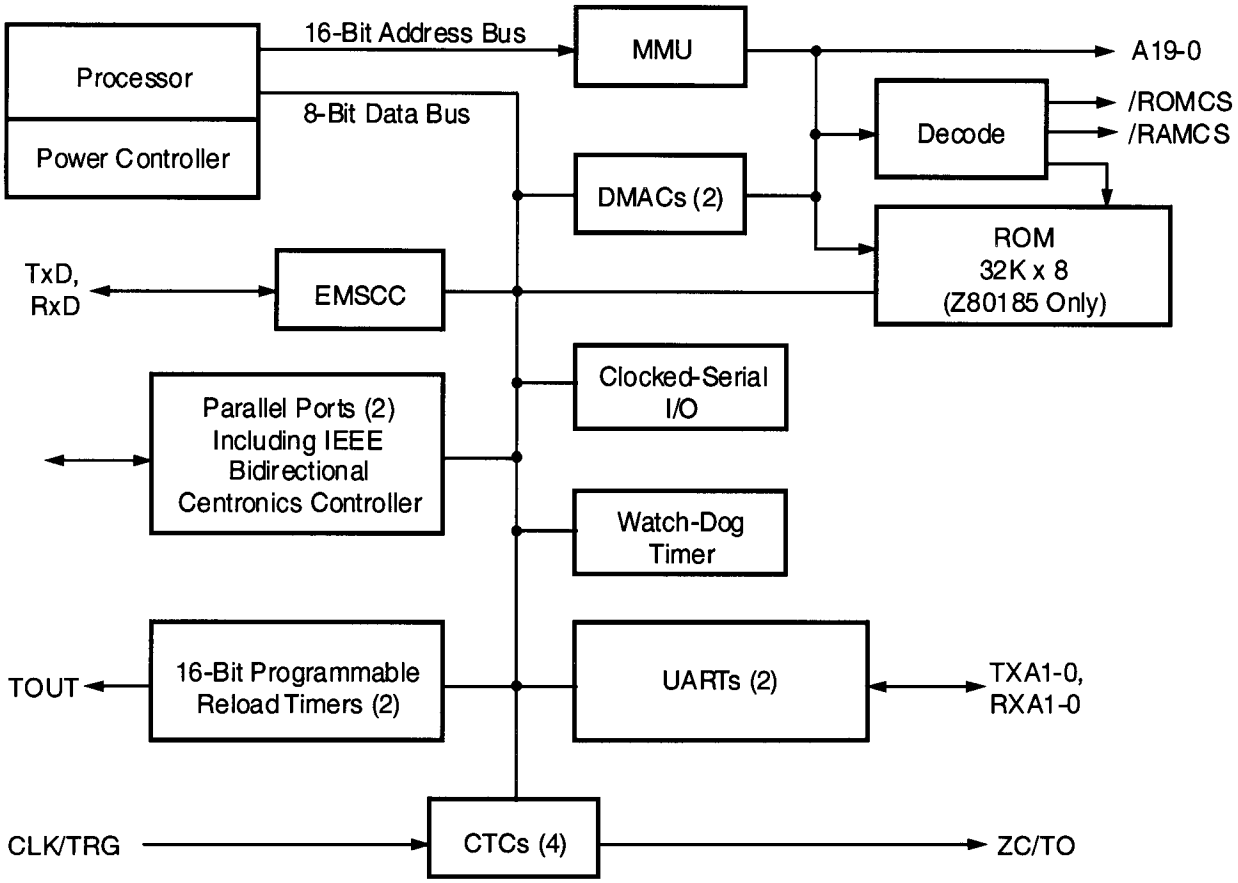


Figure 1. Z80185/195 Functional Block Diagram

PIN DESCRIPTION

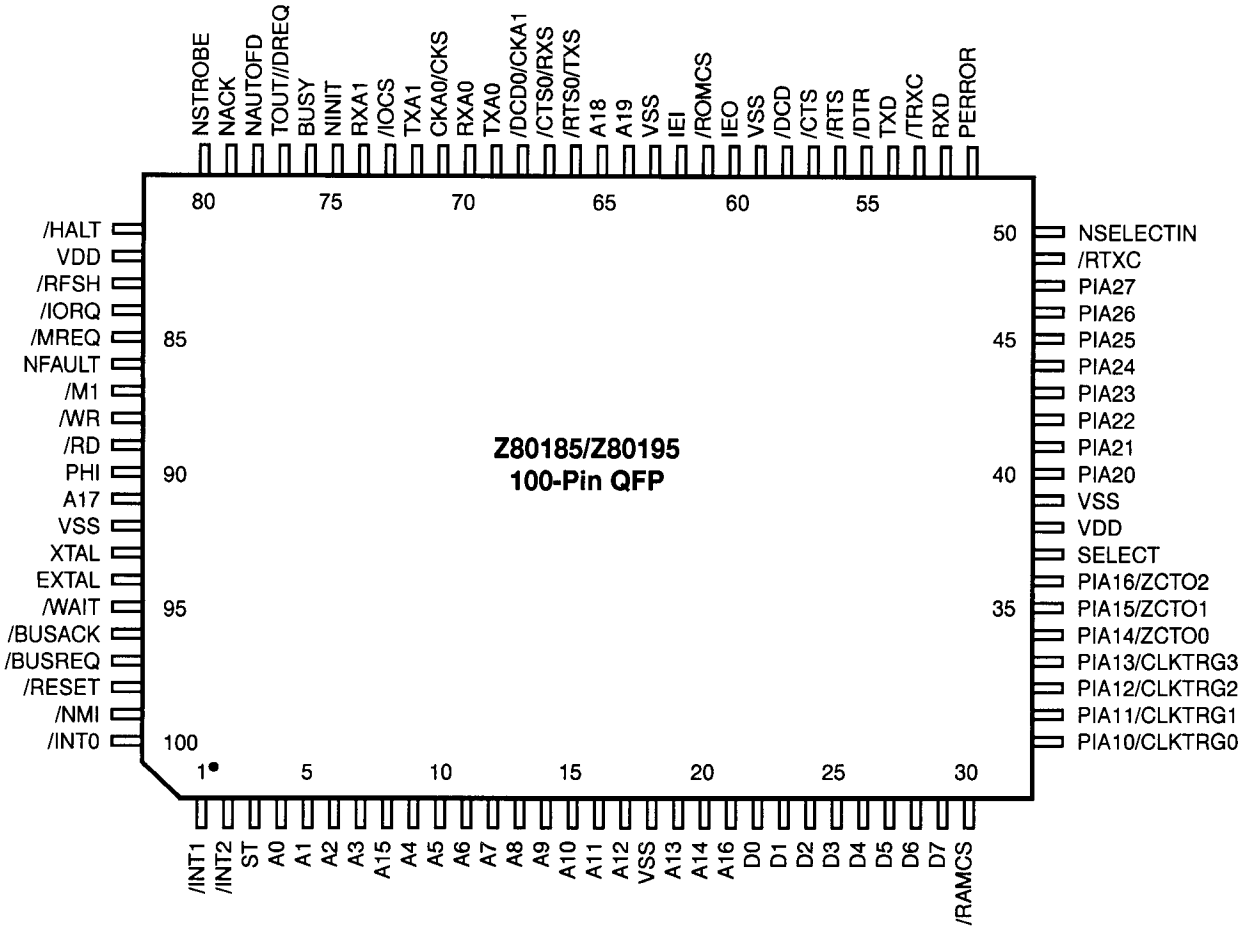


Figure 2. 100-Pin QFP Pin Assignments

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	+7.0	V
V_{IN}	Input Voltage	–0.3	V_{CC}+0.3	V
T_{OPR}	Operating Temp.	0	70	°C
T_{STG}	Storage Temp.	–55	+150	°C

Notes:

Voltage on all pins with respect to GND. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Test Load).

Operating Temperature Range:
S = 0°C to 70°C

Voltage Supply Range:
+4.5V ≤ V_{CC} ≤ +5.5V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for PHI is 125 pF.

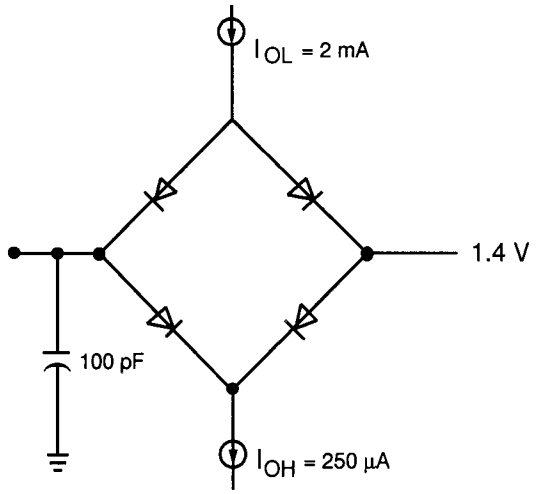


Figure 3. Test Load Diagram

DC CHARACTERISTICS

V_{DD} = 5.0V ±10%, V_{SS} = 0V over specified temperature range, unless otherwise noted.

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input "H" Voltage	†				V
V_{IL}	Input "L" Voltage	†				V
V_{OH}	Output "H" Voltage	†				V
V_{OL1}	Output "L" Voltage	†				V
I_{IL}	Input Leakage	V_{IN}=0.5 to				
	Current All Inputs	V_{DD}–0.5			1.0	
	Except XTAL,EXTAL					µA
I_{TL}	Tri-State Leakage	V_{IN}=0.5 to				
	Current	V_{DD}–0.5			1.0	µA
V_{DD}	Supply Current*					
	Normal Operation					
	For 5.0V:	f = 20 MHz		60	120	mA
	For 5.0V:	f = 33 MHz		68	132	mA
I_{CC}*	Power Dissipation*					
	System Stop Mode					
	For 5.0V:	f = 20 MHz		5	10	mA
	For 5.0V:	f = 33 MHz		7	13	mA

Notes:

† See Class Reference Table

* V_{IH} min = V_{DD} –1.0V, V_{IL} max = 0.8V (All output terminals are at no load.)

TIMING DIAGRAMS

Z8S180 MPU Timing

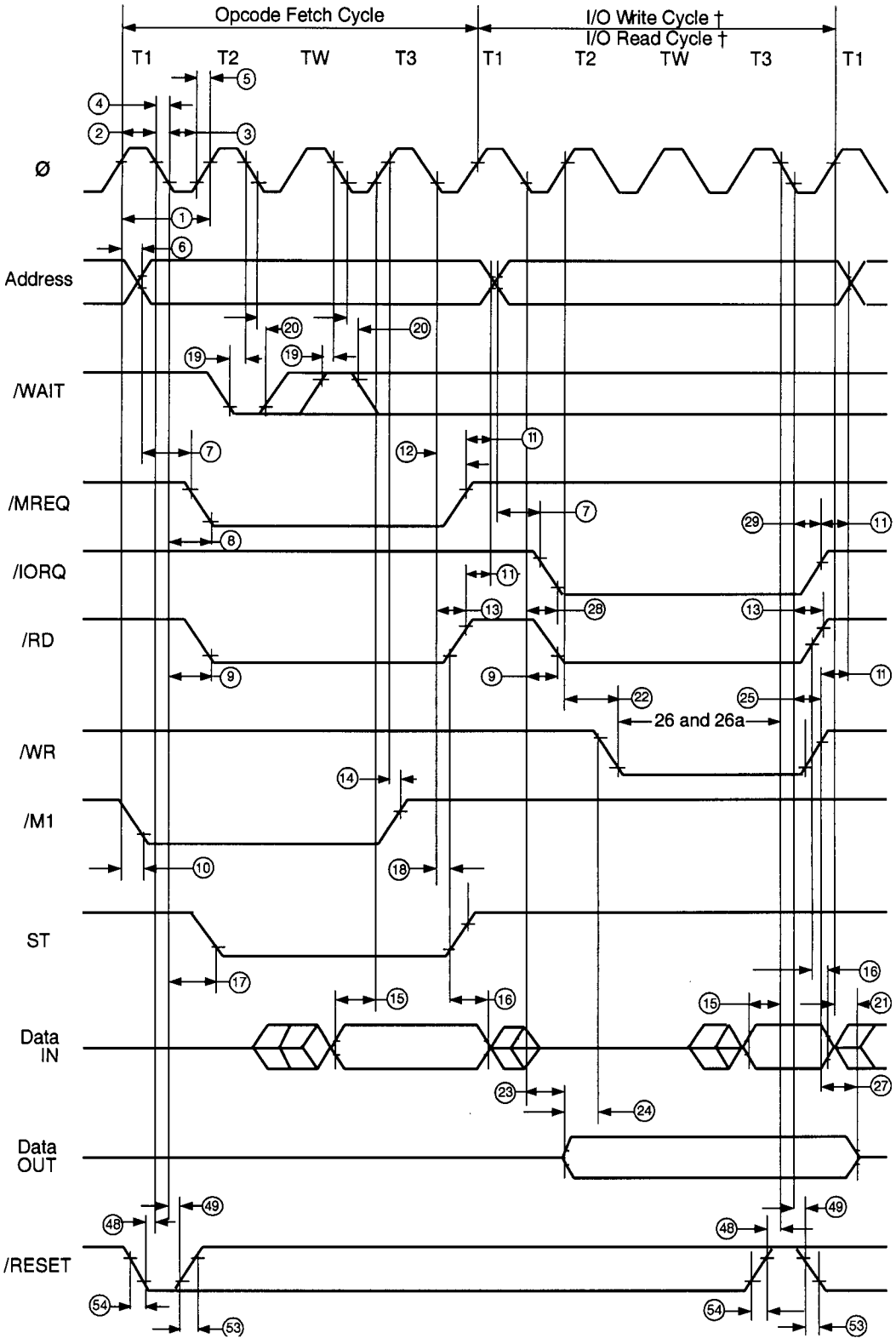


Figure 4. CPU Timing
(Opcode Fetch Cycle, Memory Read/Write Cycle
I/O Read/Write Cycle)

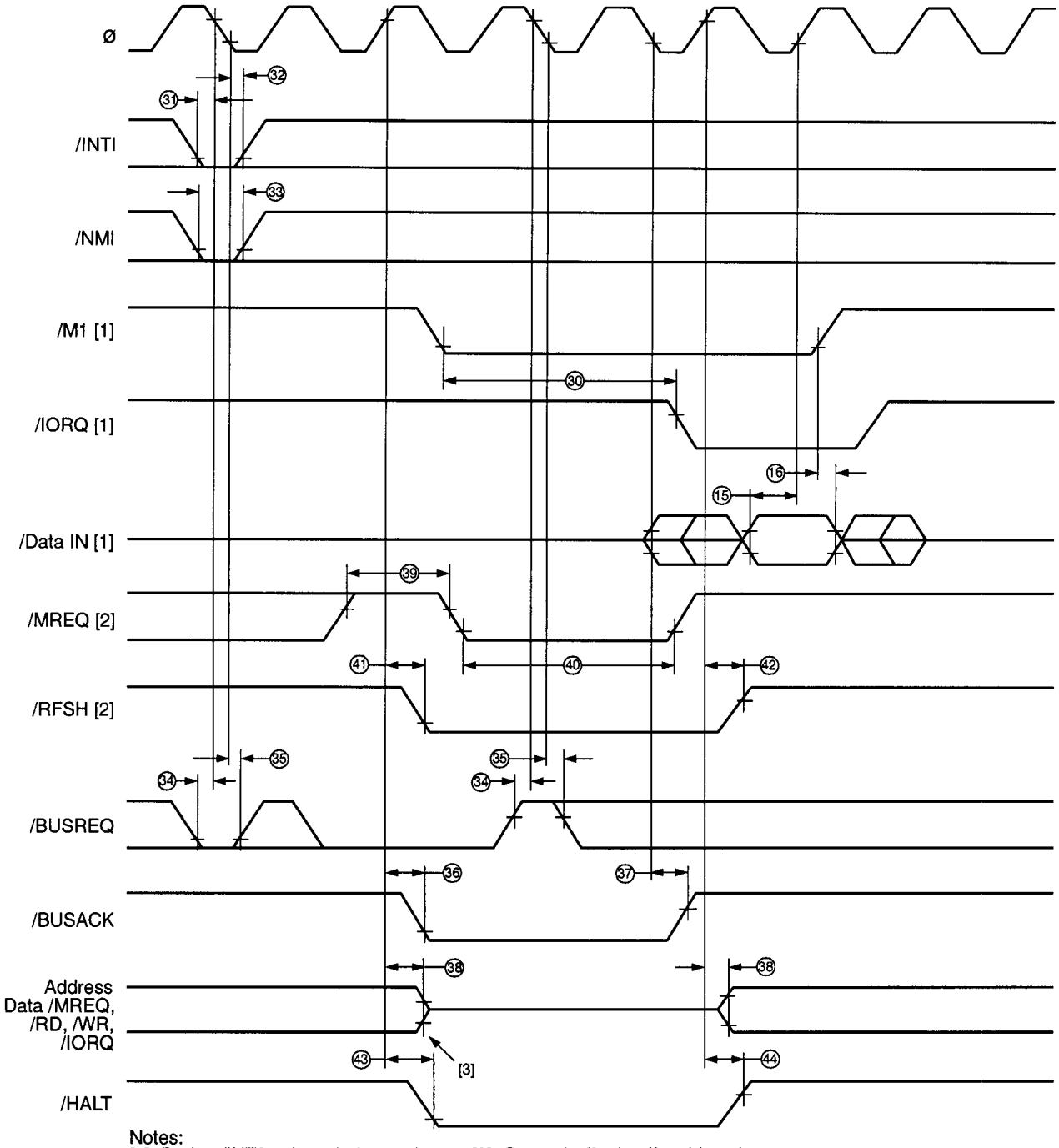


Figure 5. CPU Timing
(/INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE mode
HALT mode, SLEEP mode, SYSTEM STOP mode)

TIMING DIAGRAMS (Continued)

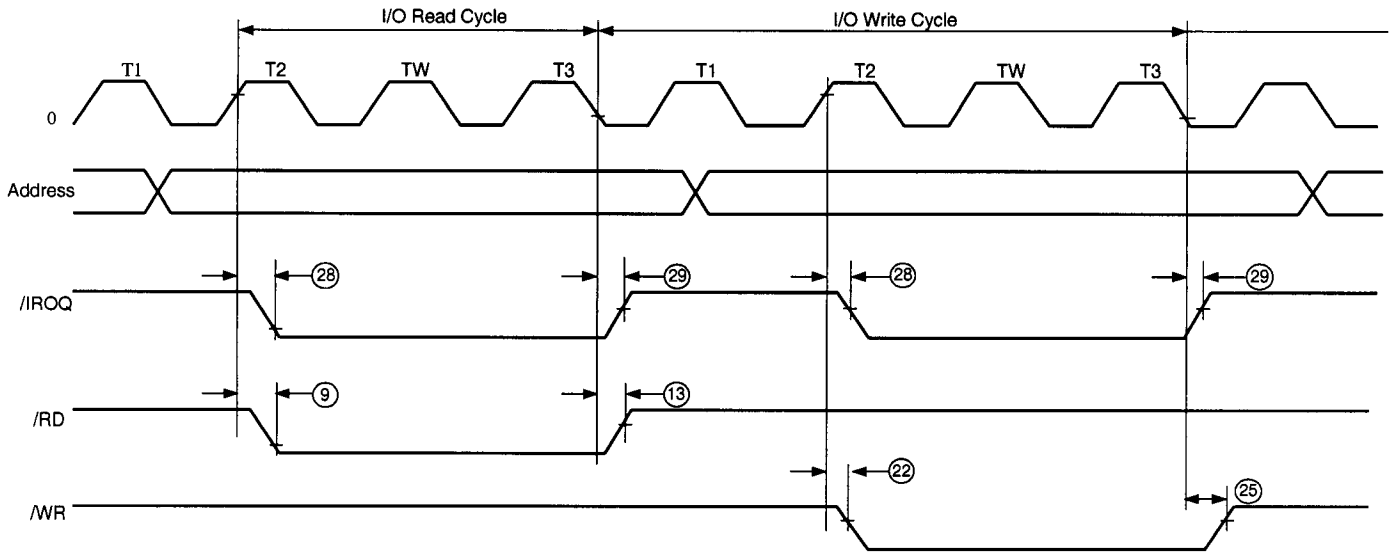
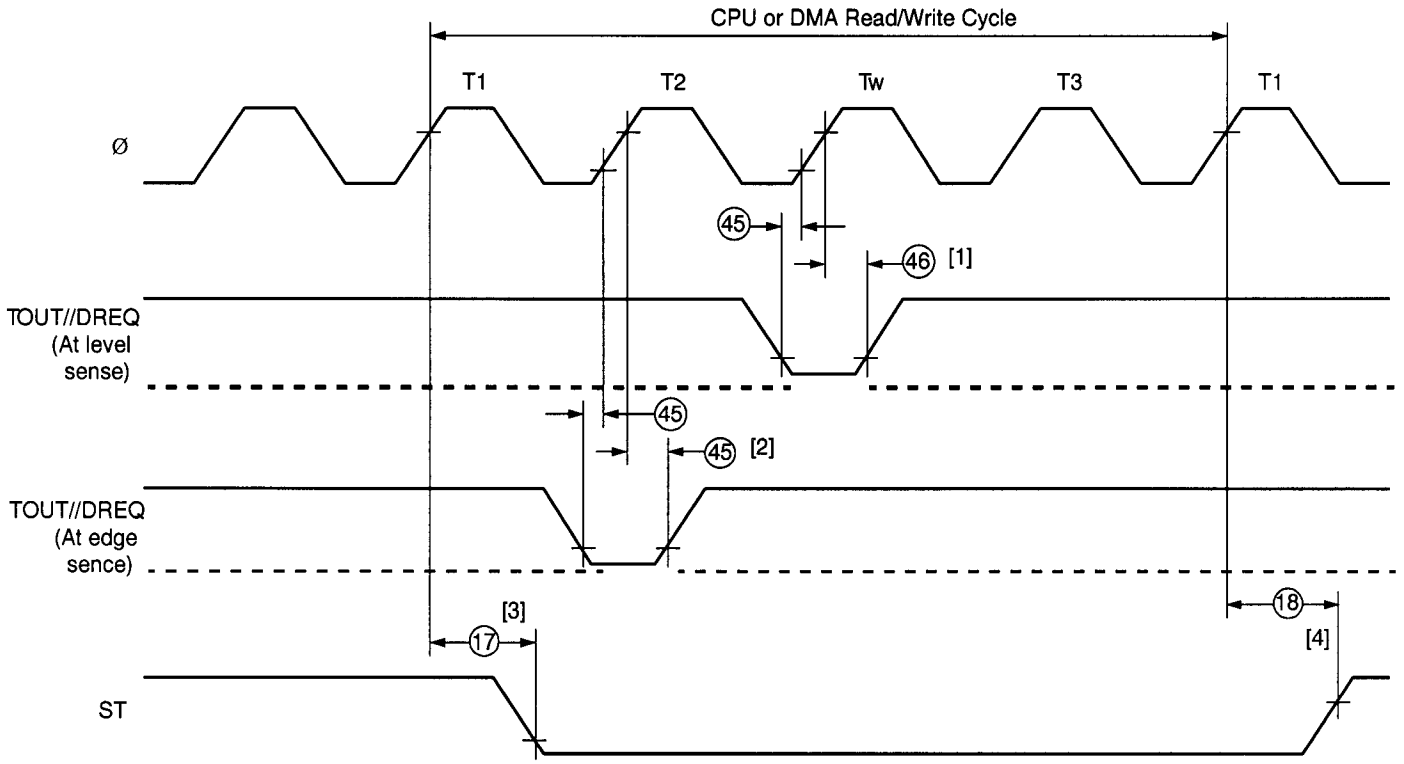


Figure 6. CPU Timing



DMA Control Signals
[1] tDRQS and tDRQH are specified for the rising edge of clock followed by
[2] tDRQS and tDRQH are specified for the rising edge of clock.
[3] DMA cycle starts.
[4] CPU cycle starts.

Figure 7. DMA Control Signals

TIMING DIAGRAMS (Continued)

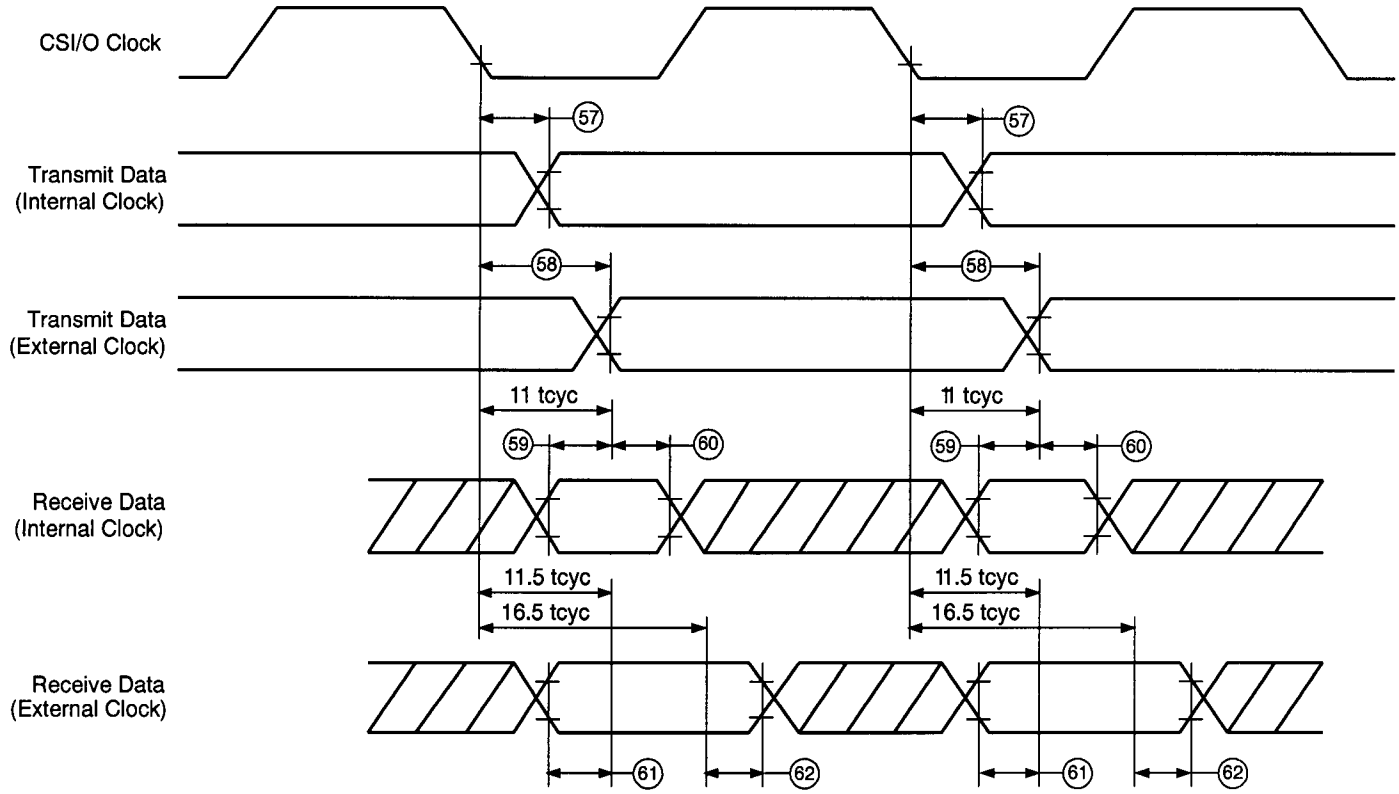


Figure 10. CSI/O Receive/Transmit Timing

TIMING DIAGRAMS (Continued)

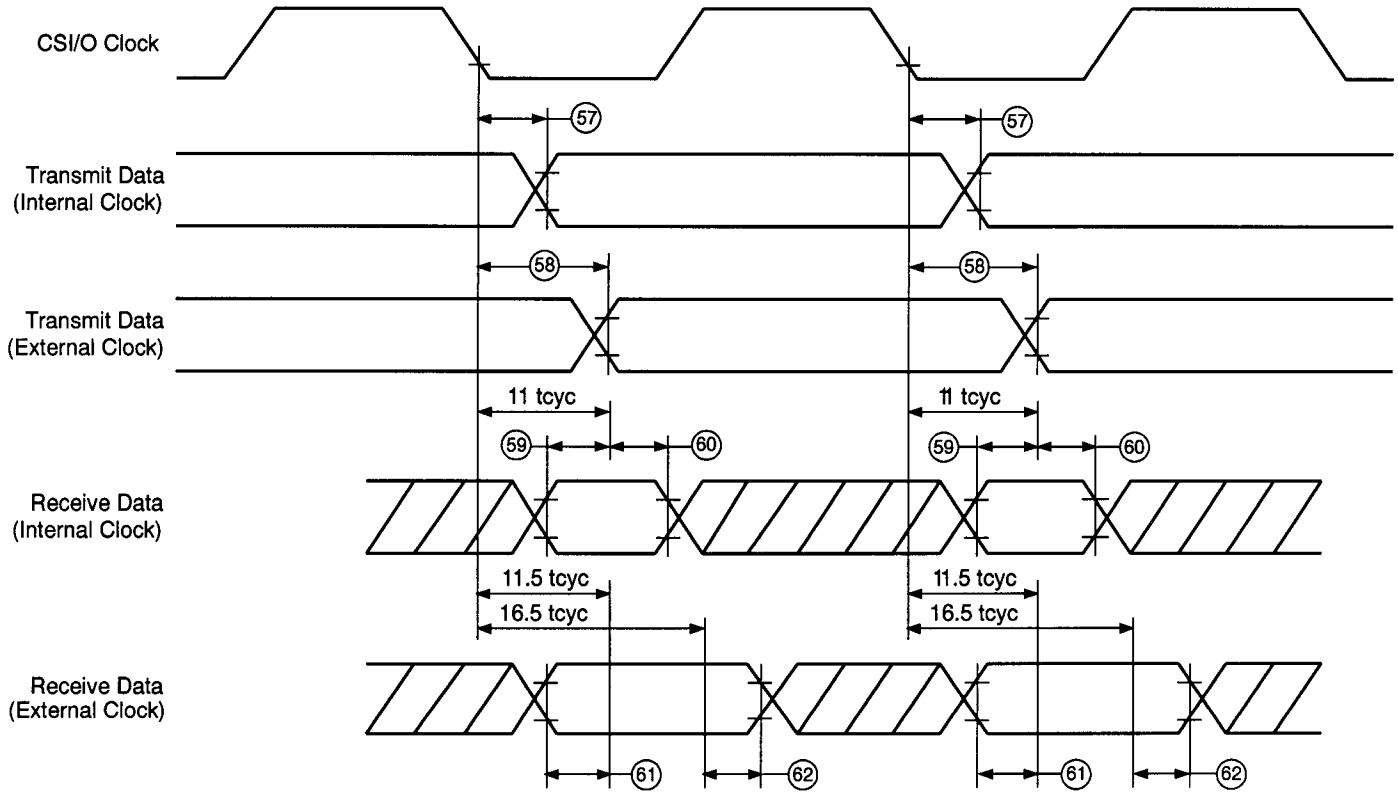


Figure 10. CSI/O Receive/Transmit Timing

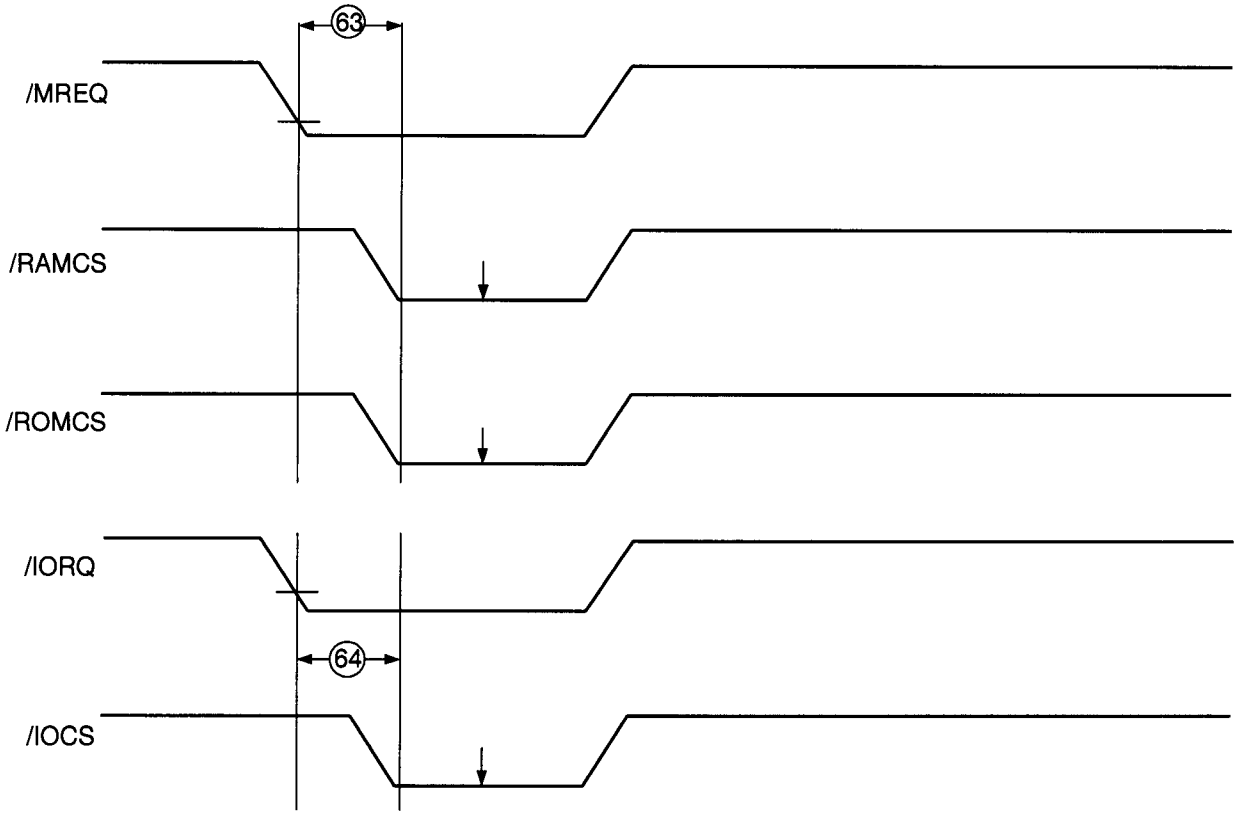


Figure 11. /ROMCS and /RAMCS Timing

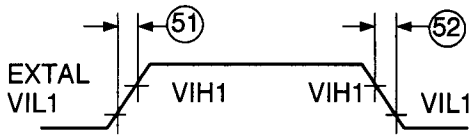


Figure 12. External Clock Rise Time and Fall Time

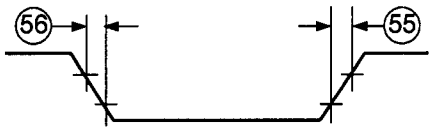


Figure 13. Input Rise and Fall Time
(Except EXTAL, /RESET)

AC CHARACTERISTICS

V_{DD} = 5V ±10%, V_{SS} = 0V, CL = 50 pF for outputs over specified temperature range, unless otherwise noted.

			Z80185 / Z80195 (20 MHz)		Z80185 / Z80195 (33 MHz)		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
1	tcy	Clock Cycle Time	50	(DC)	33	(DC)	ns
2	tCHW	Clock "H" Pulse Width	15		10		ns
3	tCLW	Clock "L" Pulse Width	15		10		ns
4	tcf	Clock Fall Time		10		5	ns
5	tcr	Clock Rise Time		10		5	ns
6	tAD	PHI Rising to Address Valid	30		15		ns
7	tAS	Address Valid to (MREQ Falling or IORQ Falling)	5		5		ns
8	tMED1	PHI Falling to MREQ Falling Delay		25		15	ns
9a	tRDD1	PHI Falling to RD Falling Delay (IOC=1)		25		15	ns
9b	tRDD1	PHI Rising to RD Falling Delay (IOC=0)		25		15	ns
10	tM1D1	PHI Rising to M1 Falling Delay		35		15	ns
11	tAH	Address Hold Time from (MREQ, IOREQ, RD, WR)	5		5		ns
12	tMED2	PHI Falling to MREQ Rising Delay		25		15	ns
13	tRDD2	PHI Falling to RD Rising Delay		25		15	ns
14	tM1D2	PHI Rising to M1 Rising Delay		40		15	ns
15	tDRS	Data Read Setup Time	10		5		ns
16	tDRH	Data Read Hold Time	0		0		ns
17	tSTD1	PHI Falling to ST Falling Delay		30		15	ns
18	tSTD2	PHI Falling to ST Rising Delay		30		15	ns
19	tWS	WAIT Setup Time to PHI Falling	15		10		ns
20	tWH	WAIT Hold Time from PHI Falling	10		5		ns
21	tWDZ	PHI Rising to Data Float Display		35		20	ns
22	tWRD1	PHI Rising to WR Falling Delay		25		15	ns
23	tWDD	PHI Rising to Write Data Delay Time		25		15	ns
24	tWDS	Write Data Setup Time to WR Falling	10		10		ns
25	tWRD2	PHI Falling to WR Rising Delay		25		15	ns
26	tWRP	Write Pulse Width (Memory Write Cycle)	75		45		ns
26a	tWRP	Write Pulse Width (I/O Write Cycle)	130		70		ns
27	WDH	Write Data Hold Time From (WR Rising)	10		5		ns
28a	tIOD	PHI Falling to IORQ Falling Delay IOC = 1)		25		15	ns
28b	tIOD	PHI Rising to IORQ Fallin g Delay (IOC =0)		25		15	ns
29	tIOD2	PHI Falling to IORQ Rising Delay		25		15	ns
30	tIOD3	M1 Falling to IORQ Falling Delay	100		80		ns
31	tINTS	INT Setup Time to PHI Falling	20		15		ns
32	tINTH	INT Hold Time from PHI Falling	10		10		ns

Note: Specifications 1 through 5 refer to an external clock input on EXTAL, and provisionally to PHI clock output. When a quartz crystal is used with the on-chip oscillator, a lower maximum frequency than that implied by spec. #1 may apply.

No.	Symbol	Parameter	Z80185 / Z80195 (20 MHz) Min	Z80185 / Z80195 (20 MHz) Max	Z80185 / Z80195 (33 MHz) Min	Z80185 / Z80195 (33 MHz) Max	Units
33	tNMIW	NMI Pulse Width	35		25		ns
34	tBRS	BUSREQ Setup Time to PHI Falling	10		10		ns
35	tBRH	BUSREQ Hold Time from PHI Falling	10		10		ns
36	tBAD1	PHI Rising to BUSACK Falling Delay		25		15	ns
37	tBAD2	PHI Falling to BUSACK Rising Delay		25		15	ns
38	tBZD	PHI Rising to Bus Floating Delay Time		40		30	ns
39	tMEWH	MREQ Pulse Width (High)	tcy –15		tcy –10		ns
40	tMEWL	MREQ Pulse Width (Low)	2tcy –15		2tcy–10		ns
41	tRFD1	PHI Rising to RFSH Falling Delay		20		15	ns
42	tRFD2	PHI Rising to RFSH Rising Delay		20		15	ns
43	tHAD1	PHI Rising to HALT Falling Delay		15		15	ns
44	tHAD2	PHI Rising to HALT Rising Delay		15		15	ns
45	tDRQS	DREQ Setup Time to PHI Rising	20		15		ns
46	tDRQH	DREQ Hold Time from PHI Rising	20		15		ns
47	tTOD	PHI Falling to Timer Output Delay		75	50		ns
48	tRES	RESET Setup Time to PHI Falling	40		25		ns
49	tREH	RESET Hold Time From PHI Falling	25		15		ns
50	tOSC	Oscillator Stabilization Time		20		20	ms
51	tEXr	External Clock Rise Time (EXTAL)		10		5	ns
52	tEXf	External Clock Fall Time (EXTAL)		10		5	ns
53	tRr	Reset Rise Time		50		50	ms
54	tRf	Reset Fall Time		50		50	ms
55	tIr	Input Rise Time (Except EXTAL, RESET)		50		50	ns
56	tIf	Input Fall Time (Except EXTAL, RESET)		50		50	ns
57	tSTDI	CSIO Transmit Data Delay Time		75		60	ns
		(Internal Clock Operation)					
58	tSTDE	CSIO Transmit Data Delay Time		7.5 tcy +75		7.5 tcy +60	ns
		(External Clock Operation)					
59	tSRSI	CSIO Receive Data Setup Time		75		60	ns
		(Internal Clock Operation)					
60	tSRHI	CSIO Receive Data Hold Time		75		60	ns
		(Internal Clock Operation)					
61	tSRSE	CSIO Receive Data Setup Time		75		60	ns
		(External Clock Operation)					
62	tSRHE	CSIO Receive Data Hold Time		75		60	ns
		(External Clock Operation)					
63	tdCS	MREQ Valid to RAMCS and ROMCS Valid Delay		15		15	ns
64	tdIOCS	Rising IORQ Valid to Rising IOCS Valid Delay		10		10	ns

Note: Specifications 1 through 5 refer to an external clock input on EXTAL, and provisionally to PHI clock output. When a quartz crystal is used with the on-chip oscillator, a lower maximum frequency than that implied by spec. #1 may apply.

AC CHARACTERISTICS (Continued)

Read/Write External Bus Master Timing

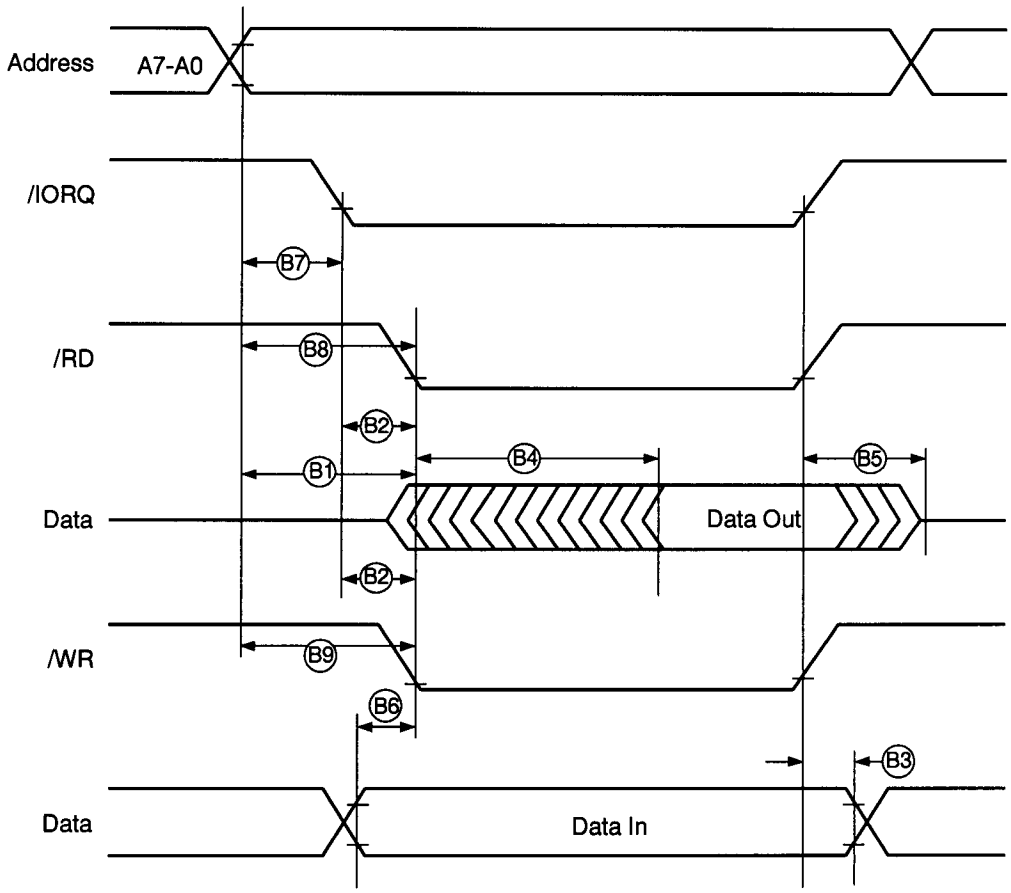


Figure 14. Read/Write External Bus Master Timing

General-Purpose I/O Timing Port Timing

Parameters referenced in Figure 15 appear in the following Tables.

Note: Port 2 timing is different, even when Bidirectional Centronics feature is not in active use.

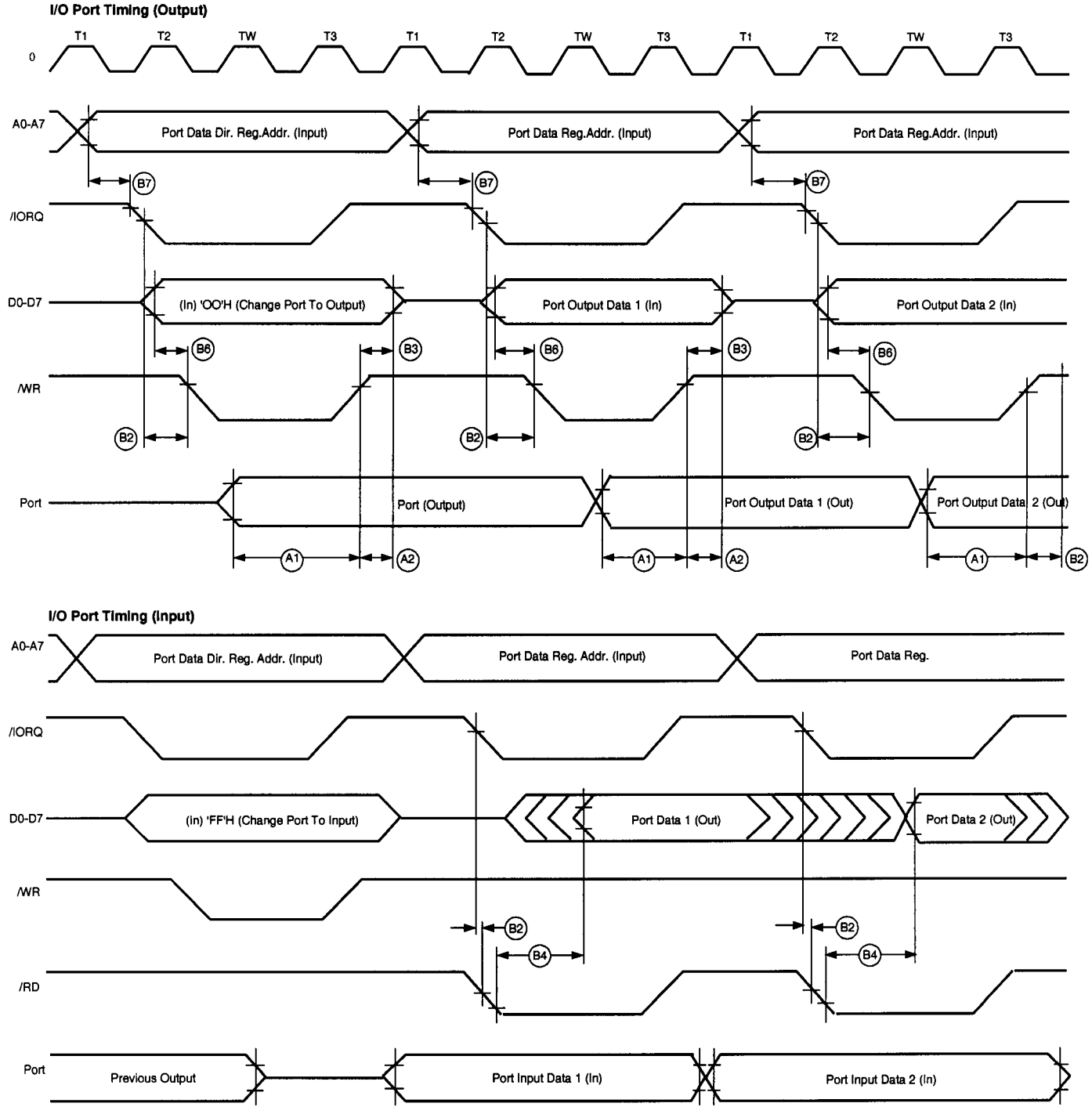


Figure 15. I/O Port Timing

AC CHARACTERISTICS (Continued)

I/O Port Timing

No.	Symbol	Parameter	Z80185 / Z80195 (20 MHz) Min	Z80185 / Z80195 (20 MHz) Max	Z80185 / Z80195 (33 MHz) Min	Z80185 / Z80195 (33 MHz) Max	Units
A1	TdWR (PIA)	Data Valid Delay from WR Rise		60		60	ns

External Bus Master Timing

No.	Symbol	Parameter	Z80185 / Z80195 (20 MHz) Min	Z80185 / Z80195 (20 MHz) Max	Z80185 / Z80195 (33 MHz) Min	Z80185 / Z80195 (33 MHz) Max	Units
B1	TsA(wf)	Address Valid to WR or (rf)	RD Fall Time	40		40	
B2	TsIO(wf)	IORQ Fall to WR or (rf)	RD Fall Time	20		20	
B3	Th	Data Hold Time (from WR Rise)	5		5		ns
B4	TdRD(DO)	RD Fall to Data Out Delay	35		35		ns
B5	TdRIr(DOz)	RD,IORQ Rise to Data Float Time	5		5		ns
B6	TsDI(WRf)	Data In to WR Fall Setup Time	20		20		ns
B7	TsA(IORQf)	Address to IORQ Fall Setup Time	20		20		ns
B8	TsA(RDf)	Address to RD Fall Setup Time	40		40		ns
B9	TsA(WRf)	Address to WR Fall Setup Time	40		40		ns

EMSCC Timing

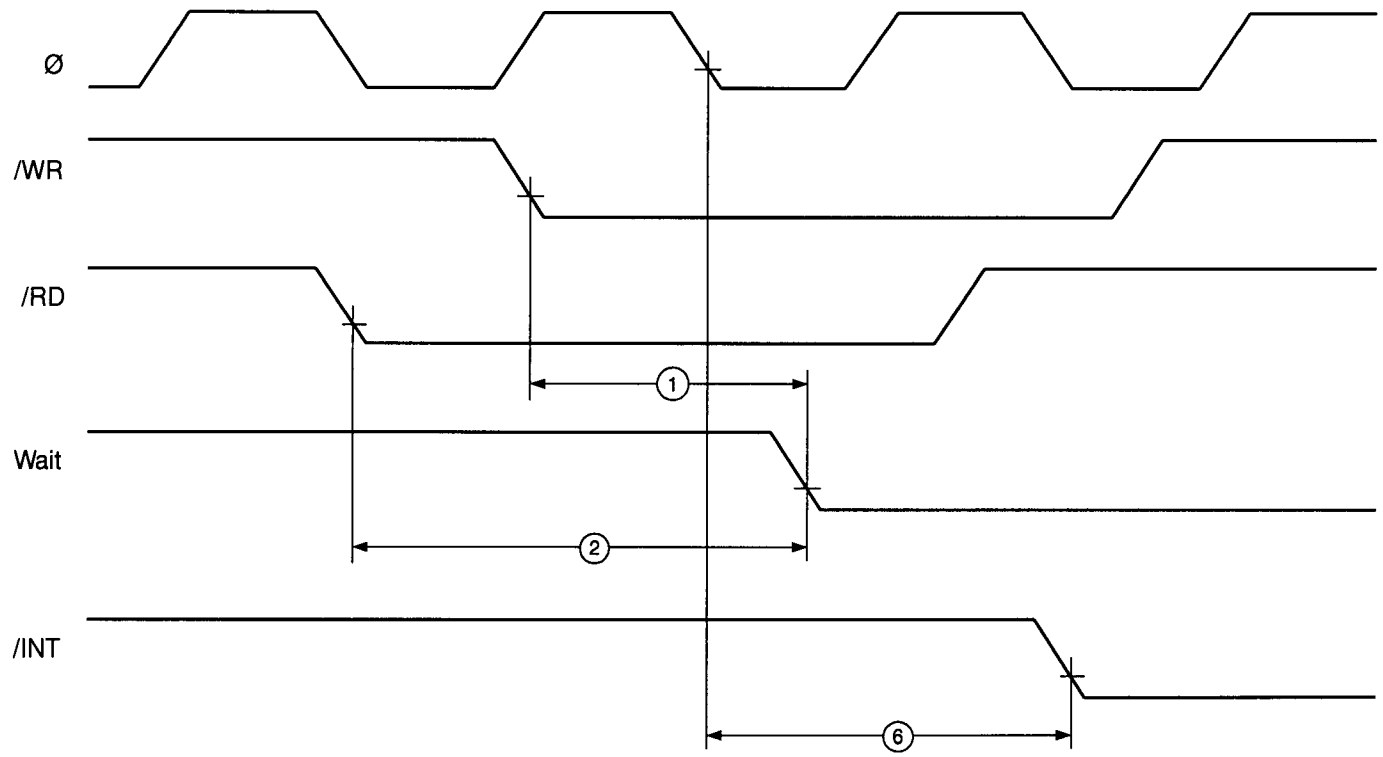


Figure 16. EMSCC AC Parameters

EMSCC Timing Parameters

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Unit
1	TdWR(W)	/WR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50	
6	TdPC(INT)	Clock to /INT Valid Delay		160	

AC CHARACTERISTICS (Continued)

EMSCC General Timing Diagram

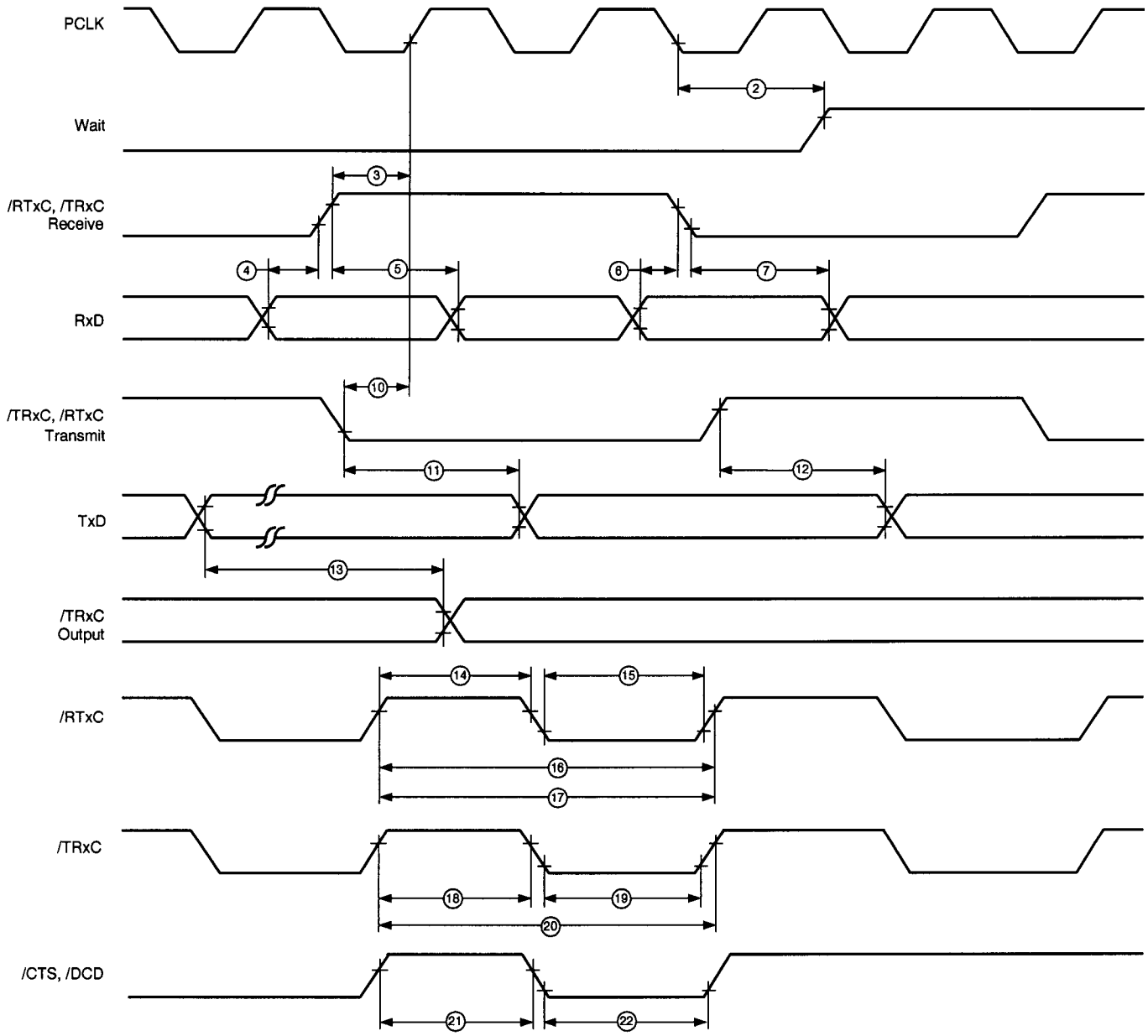


Figure 17. EMSCC General Timing Diagram

EMSCC General Timing

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Notes
2	TdPC(W)	/PCLK to Wait Inactive		170	
3	TsRxC(PC)	/RxC to /PCLK Setup Time	NA		(1,4)
4	TsRxD(RxCr)	RxD to /RxC Setup Time		0	(1)
5	ThRxD(RxCr)	RxD to /RxC Hold Time	45		(1)
6	TsRxD(RxCf)	RxD to /RxC Setup Time	0		(1,5)
7	ThRxD(RxCf)	RxD to /RxC Hold Time	45		(1,5)
10	TsTxC(PC)	/TxC to /PCLK Setup Time	NA		(2,4)
11	TdTxCf(TXD)	/TxC to TxD Delay		70	(2)
12	TdTxCr(TXD)	/TxC to TxD Delay		70	(2,5)
13	TdTxD(TRX)	TxD to TRxC Delay	80	70	
14	TwRTxh	RTxC High Width	70		(6)
15	TwRTxl	TRxC Low Width	70		(6)
16a	TcRTx	RTxC Cycle Time	200		(6,7)
16b	TxRx(DPLL)	DPLL Cycle Time Min	50		(7,8)
17	TcRTxx	Crystal OSC. Period	61	1000	(3)
18	TwTRxh	TRxC High Width	70		(6)
19	TwTRxl	TRxC Low Width	70		(6)
20	TcTRx	TRxC Cycle Time	200		(6,7)
21	TwExT	DCD or CTS Pulse Width	60		

Notes:

1. RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
2. TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
3. Both /RTxC and /SYNC have 30 pF capacitors to Ground connected to them.
4. Synchronization of RxC to PCLK is eliminated in divide-by-four operation.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
7. The maximum receive or transmit data rate is 1/4 PCLK.
8. Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock should have a 50% duty cycle.
9. These AC parameter values are preliminary and subject to change without notice.

AC CHARACTERISTICS (Continued)

EMSCC System Timing Diagram

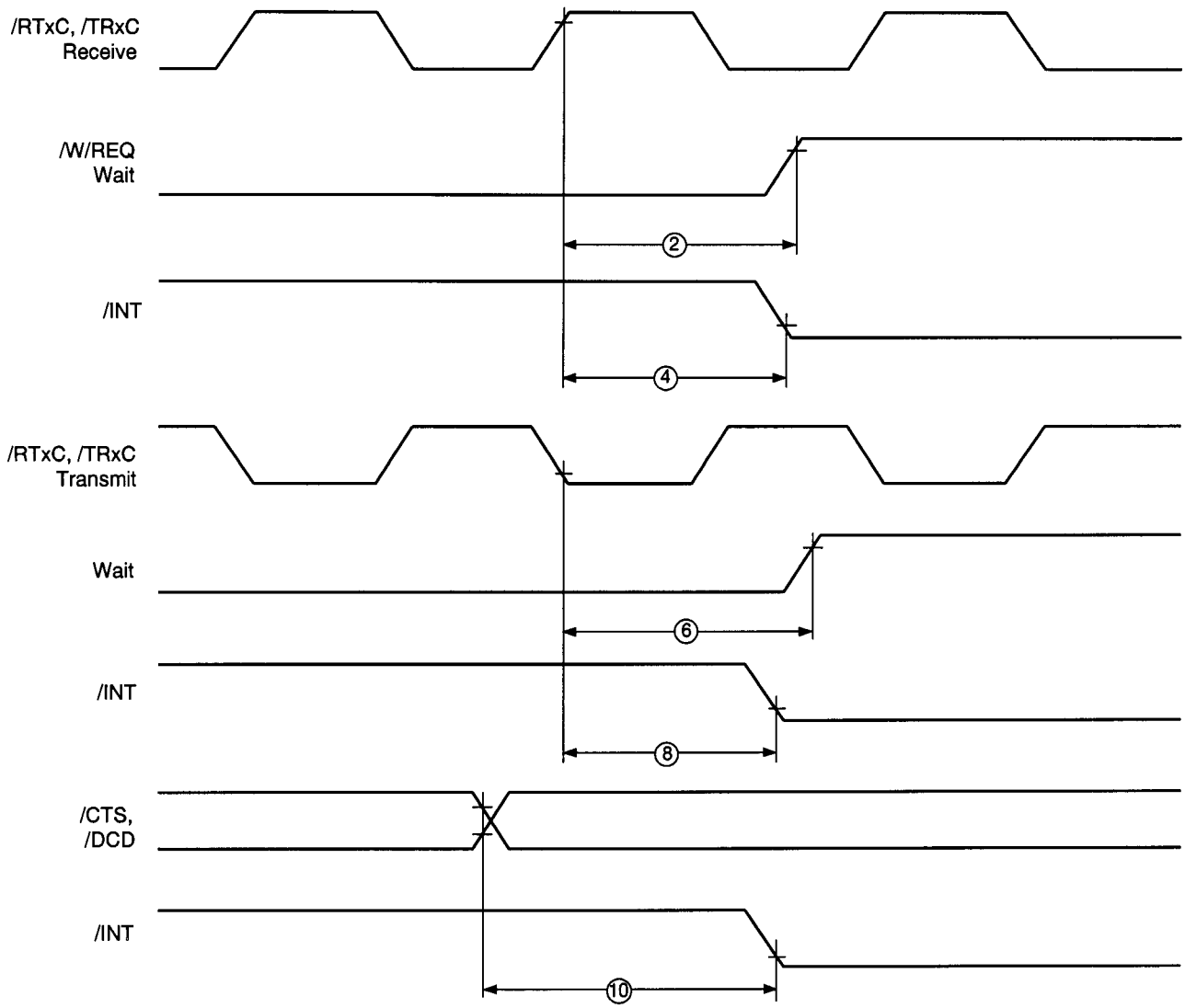


Figure 18. EMSCC System Timing

EMSCC System Timing

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Notes
2	TdRxC(W)	/RxC to /Wait Inactive	13	18	(1,2)
4	TdRxC(INT)	/RxC to /INT Valid	15	22	(1,2)
6	TdTxC(W)	/TxC to /Wait Inactive	8	17	(1,3)
8	TdTxC(INT)	/TxC to /INT Valid	9	17	(1,3)
10	TdExT(INT)	/DCD or /CTS to /INT Valid	3	9	(1)

Notes:
1. Open-drain output, measured with open-drain test load.
2. /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
3. /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
4. Units equal to TcPc

These AC parameter values are preliminary and subject to change without notice.

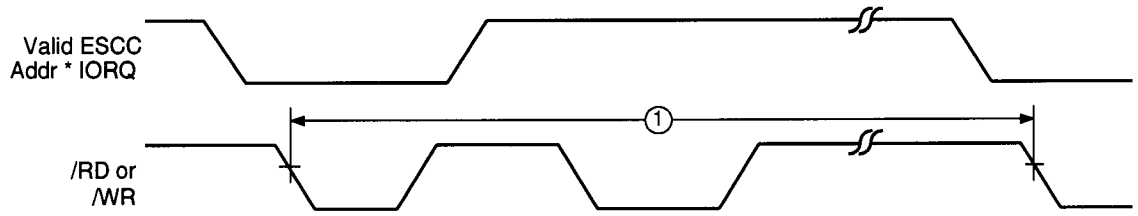


Figure 19. EMSCC External Bus Master Timing

External Bus Master Interface Timing (SCC Related Timing)

No	Symbol	Parameter	Z80185 / Z80195 (20 MHz) Min	Z80185 / Z80195 (20 MHz) Max	Z80185 / Z80195 (33 MHz) Min	Z80185 / Z80195 (33 MHz) Max	Unit	Notes
1	TrC	Valid Access Recovery Time	4TcC		4TcC		ns	(1)

Notes:
1. Applies only between transactions involving the EMSCC.

These AC parameter values are preliminary and subject to change without notice.

T_{CC} = EMSCC Clock Period Time

AC CHARACTERISTICS (Continued)

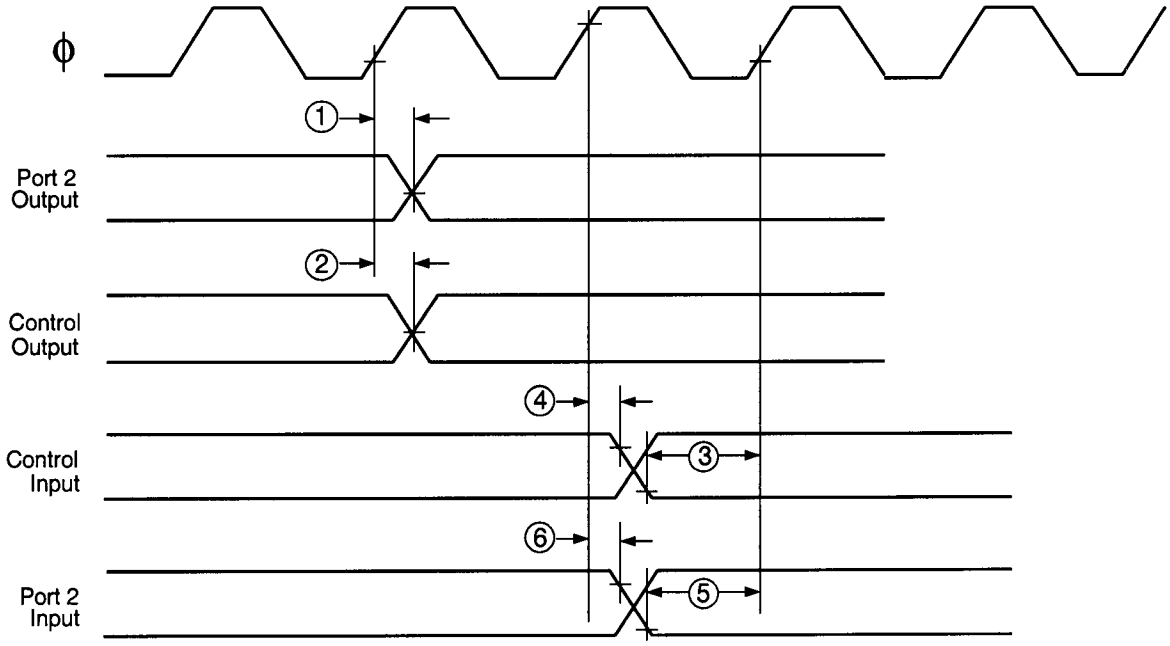


Figure 20. P1284 Bidirectional Centronics Interface Timing

P1284 Bidirectional Centronics Interface Timing

No.	Parameter	Min	Max	Units	Notes
1	CLK High to Port 2 Output		12	ns	
2	CLK High to Control Output		12	ns	(1)
3	Setup Time for Control Input to CLK High for Guaranteed Recognition	10		ns	(2)
4	Hold Time for Control Input from CLK High for Guaranteed Recognition	5		ns	(2)
5	Setup Time for Port 2 Inputs to CLK High for Guaranteed Recognition	10		ns	
6	Hold Time for Port 2 Inputs to CLK High for Guaranteed Recognition	5		ns	

Notes:

1. **Control Outputs**

Peripheral Mode	Host Mode
Busy/PtrBusy/PeriphAck	nStrobe/HostClk
nAck/PtrClk/PeriphClk	nAutoFd/HostBusy/HostAck
PError/AckDataReq/nAckReverse	nSelectIn/P1284Active
nFault/nDataAvail/nPeriphRequest	nInit/nReverseRequest
Select/Xflag	

2. **Control Inputs**

Peripheral Mode	Host Mode
Busy/PtrBusy/PeriphAck	nStrobe/HostClk
nAck/PtrClk/PeriphClk	nAutoFd/HostBusy/HostAck
PError/AckDataReq/nAckReverse	nSelectIn/P1284Active
nFault/nDataAvail/nPeriphRequest	nInit/nReverseRequest
Select/Xflag	

PIN DESCRIPTIONS

Z80185 CPU Signals

A0-A19. *Address Bus* (input/output, active High, tri-state). A0-A19 is a 20-bit address bus that provides the address for memory data bus cycles up to 1 Mbyte, and I/O data bus cycles up to 64 Kbytes. The address bus enters a High impedance state during reset and external bus acknowledge cycles. This bus is an input when /BUSACK is Low. No address lines are multiplexed with any other signals.

D0-D7. *Data Bus* (bidirectional, active High, tri-state). D0-D7 constitute an 8-bit bidirectional data bus, used to transfer information to and from I/O and memory devices. The data bus enters the High impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

/RD. *Read* (input/output, active Low, tri-state). /RD indicates that the CPU is ready to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus. This pin is tri-stated during bus acknowledge cycles.

/WR. *Write* (input/output, active Low, tri-state). /WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location. This pin is tri-stated during bus acknowledge cycles.

/IORQ. *I/O Request* (input/output, active Low, tri-state)./IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. /IORQ is also generated, along with /M1, during the acknowledgment of the /INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This pin is tri-stated during bus acknowledge cycles.

/M1. *Machine Cycle 1* (input/output, active Low). Together with /MREQ, /M1 indicates that the current cycle is the opcode fetch cycle of an instruction execution. Together with /IORQ, /M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the /HALT and ST signal to indicate the status of the CPU machine cycle. The processor can be configured so that this signal is compatible with the /M1 signal of the Z80, or with the /LIR signal of the Z64180. This pin is tri-stated during bus acknowledge cycles.

/MREQ. *Memory Request* (input/output, active Low, tri-state). /MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. It is included in the /RAMCS and /ROMCS signals, and because of this may not be needed in some applications. This pin is tri-stated during bus acknowledge cycles.

/WAIT. (input/open-drain output, active Low.) /WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. External devices should also drive this pin in an open-drain fashion. This results in a "wired OR" of the Wait indications produced by external devices and those produced by the two separate Wait State generators in the Z80185. If the wire-ORed input is sampled Low, then additional wait states are inserted until the /WAIT input is sampled High, at which time the cycle is completed.

/HALT. *Halt/Sleep Status* (output, active Low). This output is asserted after the CPU has executed either the HALT or SLP instruction, and is waiting for either non-maskable or maskable interrupt before operation can resume. It is also used with the /M1 and /ST signals to indicate the status of the CPU machine cycle. On exit of Halt/Sleep, the first instruction fetch is delayed 16 clock cycles after the /HALT pin goes High.

/BUSACK. *Bus Acknowledge* (output, active Low). /BUSACK indicates to the requesting device that the MPU address and data bus, as well as some control signals, have entered their High impedance state.

/BUSREQ. *Bus Request* (input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions and places the address and data buses, and other control signals, into the High impedance state.

/NMI. *Non-Maskable Interrupt* (input, negative edge triggered). /NMI has a higher priority than /INT and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.

/INT0. *Maskable Interrupt Request 0* (input/open-drain output, active Low). This signal is generated by internal and external I/O devices. External devices should also drive this signal in an open-drain fashion. The CPU will honor this request at the end of the current instruction cycle as long as it is enabled, and the /NMI and /BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the /M1 and /IORQ signals will become active.

PIN DESCRIPTIONS (Continued)

/INT1, /INT2. *Maskable Interrupt Requests* (1 and 2 inputs, active Low). These signals are generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the /NMI, /BUSREQ, and /INT0 signals are inactive. The CPU will acknowledge these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for /INT0 during this cycle, neither the /M1 nor the /IORQ signals will become active. These pins may be programmed to provide active Low level, rising or falling edge interrupts. The level of the external /INT1 and /INT2 pins may be read in the Interrupt Edge Register.

/RFSH. *Refresh* (output, active Low, tri-state). /RFSH and /MREQ active indicate that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order eight bits of the address bus (A7-A0) contain the refresh address.

Z80185 UART and CSIO Signals

CKA0/CKS. *Asynchronous Clock 0 or Serial Clock* (input/output). An optional clock input or output for ASCI channel 0 or the Clocked Serial I/O Port.

/DCD0/CKA1. *Data Carrier Detect 0 or Asynchronous Clock 1* (input/output). A Low-active modem status input for ASCI channel 0, or a clock input or output for ASCI channel 1.

/RTS0/TxS. *Request to Send 0 or Clocked Serial Transmit Data* (output). A programmable modem control output for ASCI channel 0, or the serial output from the CSIO channel.

/CTS0/RxS. *Clear to Send 0 or Clocked Serial Receive Data* (input). A Low-active modem control input for ASCI channel 0, or the serial data input to the CSIO channel.

TXA0. *Transmit Data 0* (output). This output transmits data from ASCI channel 0.

RXA0. *Receive Data 0* (input). This input receives data for ASCI channel 0.

RXA1. *Receive Data 1* (input). This input receives data for ASCI channel 1.

TXA1. *Transmit Data 1* (output). This output transmits data from ASCI Channel 1.

Multiplexed Signal

TOUT//DREQ. *Timer Out or External DMA Request* (input or output). This pin can be programmed to be either TOUT, the High-active pulse output from PRT channel 1, or a Low- active DMA Request input from an external peripheral.

Z80185 EMSCC Signals

TXD. *Transmit Data* (output). This output transmits serial data at standard TTL levels.

RXD. *Receive Data* (input). This input receives serial data at standard TTL levels.

/TRXC. *Transmit/Receive Clock* (input or output). This pin functions under program control. /TRXC may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/RTXC. *Receive/Transmit Clock* (input). This pin functions under program control. /RTXC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase-locked loop. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

/CTS. *Clear To Send* (input, active Low). If this pin is programmed as an "auto enable", a Low on it enables the EMSCC transmitter. If not programmed as an auto enable, it can be used as a general-purpose input. This pin is Schmitt-trigger buffered to accommodate slow rise-times. The EMSCC detects transitions on this input and can interrupt the processor on either logic level transition.

/DCD. *Data Carrier Detect* (input, active Low). This pin functions as an EMSCC receiver enable when programmed as an "auto enable"; otherwise it can be used as a general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-times. The EMSCC detects transitions on this pin and can interrupt the processor on either logic level transition.

EMSCC Signals

/RTS. *Request to Send* (output, active Low). When the Request to Send (RTS) bit in Write Register 5 is set, the/RTS signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode, or in Asynchronous mode with auto enables off, the /RTS pin strictly follows the state of the RTS bit. Thus the pin can be used as a general-purpose output. In a special "AppleTalk" mode on the Z80185, the pin is under hardware control.

/DTR. *Data Terminal Ready* (outputs, active Low). The"/DTR//REQ" functionality found in other SCC family members has been reconfigured internal to the EMSCC megacell. The /DTR output is routed to this pin, while the/REQ signal is routed to the DMA request multiplexing logic as described in a later section on the EMSCC. This pin follows the state of the DTR bit in WR5 of the EMSCC.

Note: The /W/REQ pin present on other SCC family members has its two possible functions reconfigured internal to the EMSCC, and both functions are handled internally to the Z80185. The Wait output of the EMSCC drives the/WAIT signal in a wire-ORed fashion with other internal and external peripherals. The /REQ component is routed to the DMA request multiplexing logic as described in a later section on the EMSCC.

Z80185 Parallel Ports

PIA16-14. *Port 1, Bits 6-4 or CTC ZC/TO2-0* (input/output). These lines can be configured as inputs or outputs, or as the "zero count/timeout" outputs of three of the four CTC channels, on a bit-by-bit basis.

PIA13-10. *Port 1, Bits 3-0 or CTC CLK/TRG3-0* (input/output). These lines can be configured as inputs or outputs, or as the "clock/trigger" inputs of the four CTC channels, on a bit-by-bit basis.

PIA27-20. *Port 2, Data, or Bidirectional* (input/output). These lines can be configured as inputs or outputs on a bit-by-bit basis when not used for Bidirectional Centronics operation. However, when used for Bidirectional Centronics operation, software and hardware controls the direction of all eight as a unit.