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Data Communications Family

Z380 Microprocessor

Product Specification

PS010002-0708

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
July 2008	02	Updated format to the latest PS template	All
March 2001	01	Original Issue	All

FEATURES

- Static CMOS Design with Low-Power Standby Mode Option
- 32-Bit Internal Data Paths and ALU
- Operating Frequency
  - DC-to-18 MHz at 5V
  - DC-to-10 MHz at 3.3V
- Enhanced Instruction Set that Maintains Object-Code Compatibility with Z80® and Z180 Microprocessors
- 16-Bit (64K) or 32-Bit (4G) Linear Address Space
- 16-Bit Data Bus with Dynamic Sizing
- Two-Clock Cycle Instruction Execution Minimum
- Four Banks of On-Chip Register Files
- Enhanced Interrupt Capabilities, Including 16-Bit Vector
- Undefined Opcode Trap for Z380™ Instruction Set
- On-Chip I/O Functions:
  - Six-Memory Chip Selects with Programmable Waits
  - Programmable I/O Waits
  - DRAM Refresh Controller
- 100-Pin QFP Package

GENERAL DESCRIPTION

The Z380 Microprocessor is an integrated high-performance microprocessor with fast and efficient throughput and increased memory addressing capabilities. The Z380 offers a continuing growth path for present Z80-or Z180-based designs, while maintaining Z80® CPU and Z180 MPU object-code compatibility. The Z380 MPU enhancements include an improved 280 CPU, expanded 4-Gbyte space and flexible bus interface timing.

An enhanced version of the Z80 CPU is key to the Z380 MPU. The basic addressing modes of the Z80 microprocessor have been augmented as follows: Stack Pointer Relative loads and stores, 16-bit and 24-bit indexed offsets, and more flexible Indirect Register addressing, with all of the addressing modes allowing access to the entire 32-bit address space. Additions made to the instruction set, include a full complement of 16-bit arithmetic and logical operations, 16-bit I/O operations, multiply and divide, plus a complete set of register-to-register loads and exchanges.

The expanded basic register file of the Z80 MPU microprocessor includes alternate register versions of the IX and IY registers. There are four sets of this basic Z80 microprocessor register file present in the Z380 MPU, along with the necessary resources to manage switching between the different register sets. All of the register-pairs and index registers in the basic Z80 microprocessor register file are expanded to 32 bits.

The Z380 MPU expands the basic 64 Kbyte Z80 and Z180 address space to a full 4 Gbyte (32-bit) address space. This address space is linear and completely accessible to the user program. The I/O address space is similarly expanded to a full 4 Gbyte (32-bit) range and 16-bit I/O, and both simple and block move are added.

Some features that have traditionally been handled by external peripheral devices have been incorporated in the design of the Z380 microprocessor. The on-chip peripherals reduce system chip count and reduce interconnection on the external bus. The Z380 MPU contains a refresh controller for DRAMs that employs a /CAS-before-/RAS refresh cycle at a programmable rate and burst size.

Six programmable memory-chip selects are available, along with programmable wait-state generators for each chip-select address range.

The Z380 MPU provides flexible bus interface timing, with separate control signals and timing for memory and I/O. The memory bus control signals provide timing references suitable for direct interface to DRAM, static RAM, EPROM, or ROM. Full control of the memory bus timing is possible because the /WAIT signal is sampled three times during a memory transaction, allowing complete user control of edge-to-edge timing between the reference signals provided by the Z380 MPU. The I/O bus control signals allow direct interface to members of the Z80 family of peripherals, the Z8000 family of peripherals, or the Z8500 series of peripherals. Figure 1 shows the Z380 block diagram; Figure 2 shows the pin assignments.

Note: All signals with a preceding front slash, "/", are active Low e.g., B//W (WORD is active Low); B/W is active Low, only)

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

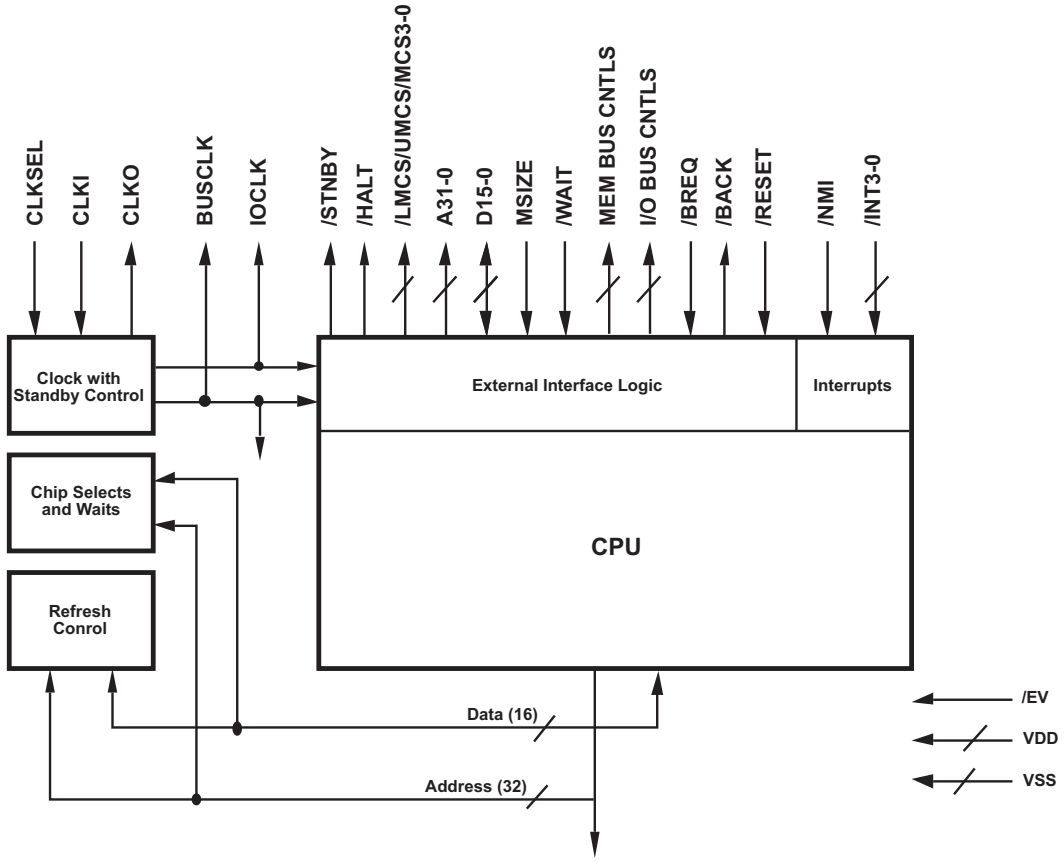

Figure 1. Z380 Functional Block Diagram

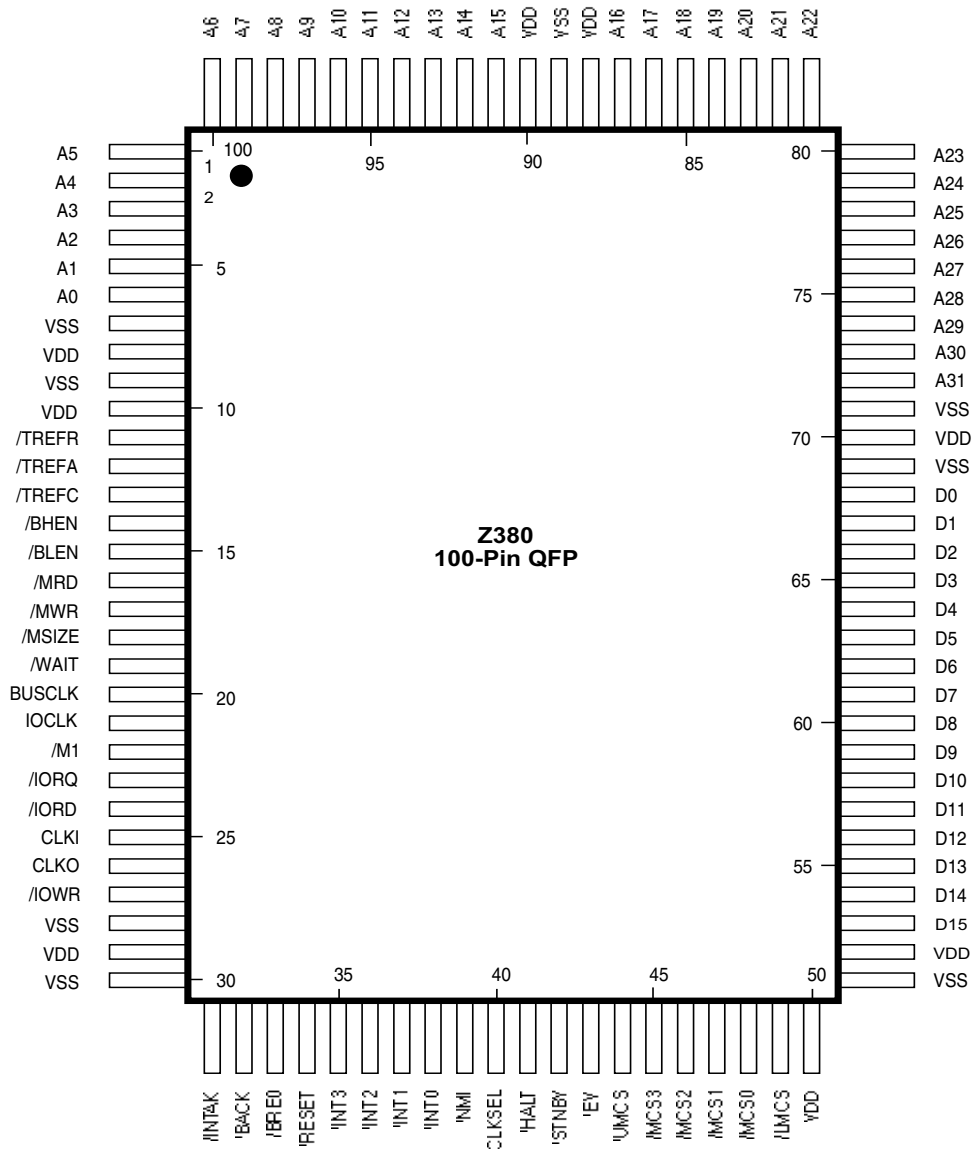

Figure 2. 100-Pin QFP Pin Assignments

PIN DESCRIPTION

A31-A0 Address Bus (outputs, activeHigh, tri-state).These non-multiplexed address signals provide a linear memory address space of four gigabytes. The 32-address signals are also used to access I/O devices.

/BACK Bus Acknowledge (output, active Low, tri-state). This signal, when asserted, indicates that the Z380 MPU has accepted an external bus request and has tri-stated its output drivers for the address bus, data bus and the bus control signals /TREFR, /TREFA, /TREFC, /BHEN, /BLEN, /MRD, /MWR, /IORQ, /IORD, and /IOWR. Note that the Z380 MPU cannot provide any DRAM refresh transactions while it is in the bus acknowledge state.

/BHEN Byte High Enable (output, active Low, tri-state). This signal is asserted at the beginning of a memory, or refresh transaction to indicate that an operation on D15-D8 is requested. For a 16-bit memory transaction, if /MSIZE is asserted, indicating a byte-wide memory, another memory transaction is performed to transfer the data on D15-D8, this time through D15-D8.

/BLEN Byte Low Enable (output, active Low, tri-state). This signal is asserted at the beginning of a memory or refresh transaction to indicate that an operation on D7-D0 is requested. For a 16-bit memory transaction, if /MSIZE is asserted, indicating a byte-wide memory, only the data on D7-D0 will be transferred during this transaction, and another transaction will be performed to transfer the data on D15-D8, this time through D7-D0.

/BREQ Bus Request (input, active Low). When this signal is asserted, an external bus master is requesting control of the bus. /BREQ has higher priority than all nonmaskable and maskable interrupt requests.

BUSCLK Bus Clock (output, active High, tri-state). This signal, output by the Z380 MPU, is the reference edge for the majority of other signals generated by the Z380 MPU. BUSCLK is a delayed version of the CLK input.

CLKI Clock/Crystal (input, active High). An externally generated direct clock can be input at this pin and the Z380 MPU would operate at the CLKI frequency. Alternatively, a crystal up to 20 MHz can be connected across CLKI and CLKO, and the Z380 MPU would operate at half of the crystal frequency. The two clocking options are controlled by the CLKsel input.

CLKO Crystal (output, active High). Crystal oscillator connection. This pin should be left open if an externally generated direct clock is input at the CLKI pin.

CLKsel Clock Option Select (input, active High). This input should be connected to VDD to select the direct clock option and should be connected to V_{SS} for the crystal option.

D15-D0 Data Bus (input/outputs, active High, tri-state). This bi-directional 16-bit data bus is used for data transfer between the Z380 MPU and memory or I/O devices. Note that for a memory word transfer, the even-addressed (A0 = 0) byte is generally transferred on D15-D8, and the odd-addressed (A0 = 1) byte on D7-D0 (see the /MSIZE pin description).

/EV Evaluation Mode (input, active Low). This input should be left unconnected for normal operation. When it is driven to logic 0, the Z380 MPU conditions itself in the reset mode and tri-states all of its output pin drivers.

/HALT Halt Status (output, active Low, tri-state). If the Z380 MPU standby mode option is not selected, a Sleep instruction is executed no different than a Halt instruction, and the one HALT signal goes active to indicate the CPU's HALT state. If the standby mode option is selected, this signal goes active only at the Halt instruction execution.

/STNBY Standby Status (output, active Low, tri-state). If the Z380 MPU standby mode is selected, executing a sleep instruction stops clocking within the Z380 MPU and at BUSCLK and IOCLK after which this signal is asserted. The Z380 MPU is then in the low power standby mode, with all operations suspended.

/INT3-0 Interrupt Requests (inputs, active Low). These signals are four asynchronous maskable interrupt inputs.

IOCLK I/O Clock (output, active High, tri-state). This signal is a program controlled divided-down version of BUSCLK. The division factor can be two, four, six or eight with I/O transactions and interrupt-acknowledge transactions occurring relative to IOCLK.

/INTAK Interrupt Acknowledge Status (output, active Low, tri-state). This signal is used to distinguish between I/O and interrupt acknowledge transactions. This signal is High during I/O read and I/O write transactions and Low during interrupt acknowledge transactions.

/IORQ Input/Output Request (output, active Low, tri-state). This signal is active during all I/O read and write transactions and interrupt acknowledge transactions.

/M1 Machine Cycle One (output, active Low, tri-state). This signal is active during interrupt acknowledge and RETI transactions.

/IORD Input, Output Read Strobe (output, active Low, tri-state). This signal is used strobe data from the peripherals during I/O read transactions. In addition, /IORD is active during the special RETI transaction and the I/O heartbeat cycle in the Z80 protocol case.

/IOWR Input/Output Write Strobe (output, active Low, tri-state). This signal is used to strobe data into the peripherals during I/O write transactions.

/LMCS Low Memory Chip Select (output, active Low, tri-state). This signal is activated during a memory read or memory write transaction when accessing the lower portion of the linear address space within the first 16 Mbytes, but only if this chip select function is enabled.

/MCS3-/MCS0 Mid-range Memory Chip Selects (output, active Low, tri-state). These signals are individually active during memory read or write transactions when accessing the mid-range portions of the linear address space within the first 16 Mbytes. These signals can be individually enabled or disabled.

/MRD Memory Read (output, active Low, tri-state). This signal indicates that the addressed memory location should place its data on the data bus as specified by the /

BHEN and /BLEN control signals. /MRD is active from the end of T1 until the end of T4 during memory read transactions.

/MSIZE Memory Size (input, active Low). This input, from the addressed memory location, indicates if it is word size (logic High) or byte size (logic Low). In the latter case, the addressed memory should be connected to the D15-D8 portion of the data bus, and an additional memory transaction will automatically be generated to complete a word size data transfer.

/MWR Memory Write (output, active Low, tri-state). This signal indicates that the addressed memory location should store the data on the data bus, as specified by the /BHEN and /BLEN control signals. /MWR is active from the end of T2 until the end of T4 during memory write transactions.

/NMI Nonmaskable Interrupt(input, falling edge-triggered). This input has higher priority than the maskable interrupt inputs /INT3-INT0.

/RESET Reset (input, active Low). This input must be active for a minimum of five BUSCLK periods to initialize the Z380 MPU. The effect of /RESET is described in detail in the Reset section.

/TREFA Timing Reference A (output, active Low, tri-state). This timing reference signal goes Low at the end of T2 and returns High at the end of T4 during a memory read, memory write or refresh transaction. It can be used to control the address multiplexer for a DRAM interface or as the /RAS signal at higher processor clock rates.

/TREFC Timing Reference C (output, activeLow, tri-state). This timing reference signal goes Low at the end of T3 and returns High at the end of T4 during a memory read, memory write or refresh transaction. It can be used as the /CAS signal for DRAM accesses.

/TREFR Timing Reference R (output, active Low, tri-state). This timing reference signal goes Low at the end of T1 and returns High at the end of T4 during a memory read, memory write or refresh transaction. It can be used as the /RAS signal for DRAM accesses.

/UMCS Upper Memory ChipSelect (output, active Low, tri-state). This signal is activated during a memory read, memory write, or optionally a refresh transaction when accessing the highest portion of the linear address space within the first 16 Mbytes, but only if this chip select function is enabled.

V_{DD} Power Supply. These eight pins carry power to the device. They must be tied to the same voltage externally.

V_{SS} Ground. These eight pins are the ground references for the device. They must be tied to the same voltage externally.

/WAIT Wait (input, active Low). This input is sampled by BUSCLK or IOCLK, as appropriate, to insert Wait states into the current bus transaction.

The conditioning and characteristics of the Z380 MPU pins under various operation modes are defined in Table 1.

Table 1. Z380 MPU Pin Conditioning Characteristics Operation Mode Conditions

Pin Names	Normal /BREQ=1,/BACK=1, /EV=NC	Bus Relinquish /BREQ=0,/BACK=0, /EV=NC	Evaluation
CLKI	Input	Input	Input
CLKO	Output/No Connection	Output/No Connection	No Connection
CLKSEL	Input	Input	Input
BUSCLK	Output	Output	Tri-state
IOCLK	Output	Output	Tri-state
A31-A0	Output	Tri-state	Tri-state
D15-D0	Input/Output	Tri-state	Tri-state
/TREFR,/TREFA, /TREFC	Output	Tri-state	Tri-state
/MRD,/MWR	Output	Tri-state	Tri-state
/BHEN,/BLEN	Output	Tri-state	Tri-state
/LMCS,/UMCS, /MCS3-MCS0	Output	Tri-state	Tri-state
/MSIZE,/WAIT	Input	Input	Input
/HALT,/STNBY	Output	Output	Tri-state
/M1,/INTAK	Output	Output	Tri-state
/IORQ,/IORD, /IOWR	Output	Tri-state	Tri-state
/BREQ	Input	Input	Input
/BACK	Output	Output	Tri-state
/NMI,/INT3-/INT0	Input	Input	Input
/RESET	Input	Input	Input
/EV	No Connection	No Connection	Input
V_{DD}	Power	Power	Power
V_{SS}	Ground	Ground	Ground

EXTERNAL INTERFACE

Two kinds of operations can occur on the system bus: transactions and requests. At any given time, one device (either the CPU or a bus master) has control of the bus and is known as the bus master.

This section shows all of the transaction and request timing for the device. For the sake of clarity, there are more figures than are actually necessary. This should aid the reader rather than confuse. In all of the timing diagram figures, the row labelled STATUS encompasses /BHEN, /BLEN, and the chip select signals.

Transactions

A transaction is initiated by the bus master and is responded to by some other device on the bus. Only one transaction can proceed at a time; six kinds of transactions can occur: Memory, Refresh, I/O, Interrupt Acknowledge, RETI (Return from Interrupt), and Halt. The Z380 MPU is unique in that memory and I/O bus transactions use separate control signals. This allows the memory interface to be optimized independently of the I/O interface.

Memory Transactions

Memory transactions move instructions or data to or from memory when the Z380 MPU performs a memory access. Thus, they are generated during program execution to fetch instructions from memory and to fetch and store memory data. They are also generated to store old program status and fetch new program status during interrupt and trap handling, and are used by DMA peripherals to transfer information. A memory transaction is two clock cycles long unless extended with wait states. Wait states may be inserted between each of the four T states in a memory transaction and are one BUSCLK cycle long per wait state. The external /WAIT input is sampled only after any internally-generated wait states are inserted. Memory transactions may transfer either bytes or words. If the Z380 MPU attempts to transfer a word to a byte-wide memory, the /MSIZE signal should be asserted Low to force this transaction to be byte-wide dynamically. The Z380 MPU will then perform another memory transaction to transfer the byte that was not transferred during the first transaction.

Read memory transactions are shown without wait states, with wait states between T1 and T2, between T2 and T3, and between T3 and T4 (Figures 3 - 6). The data bus is driven by the memory being addressed, and the memory data is latched immediately before the rising edge of BUSCLK which terminates T4.

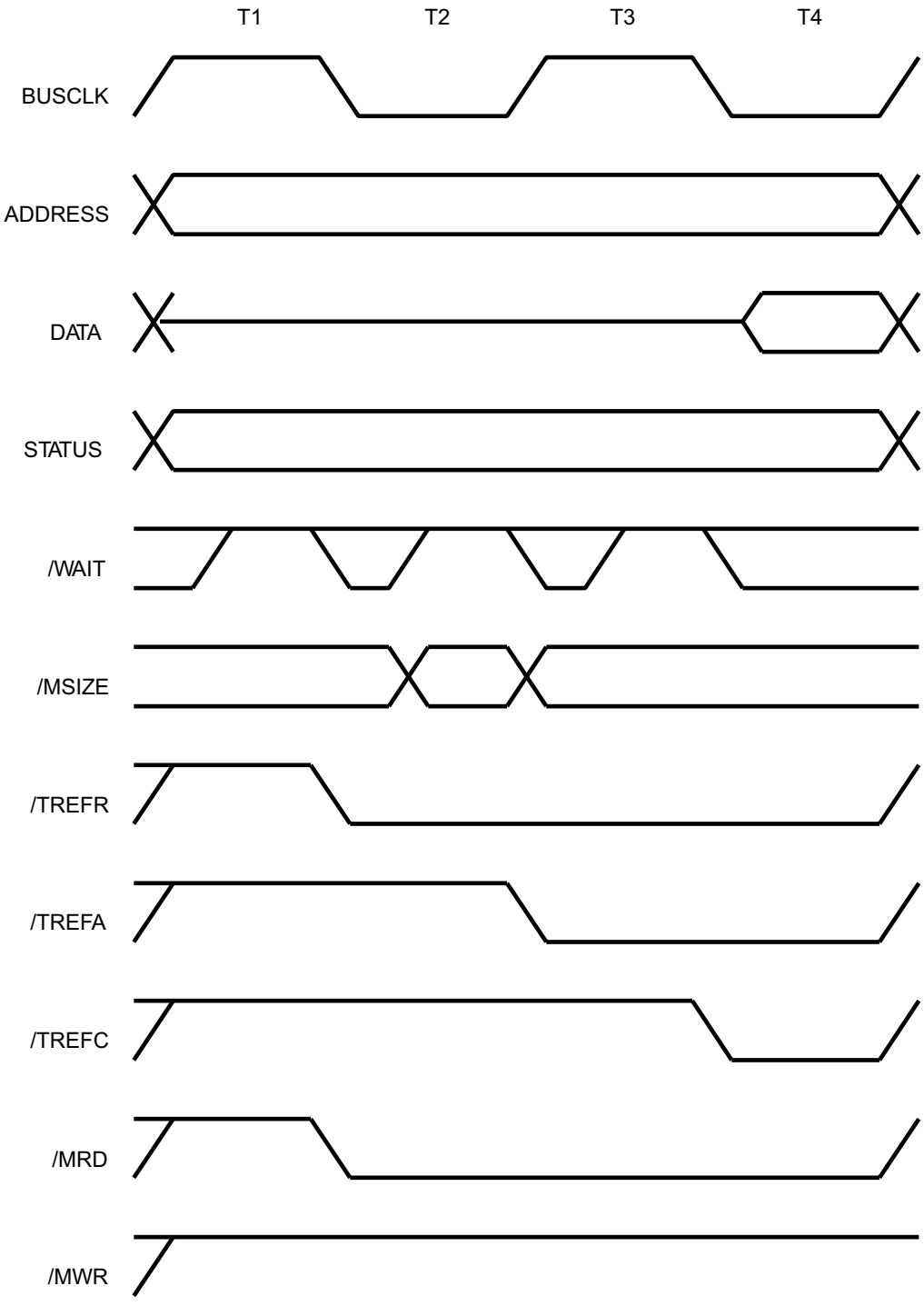

Figure 3. Read Cycle, No Waits

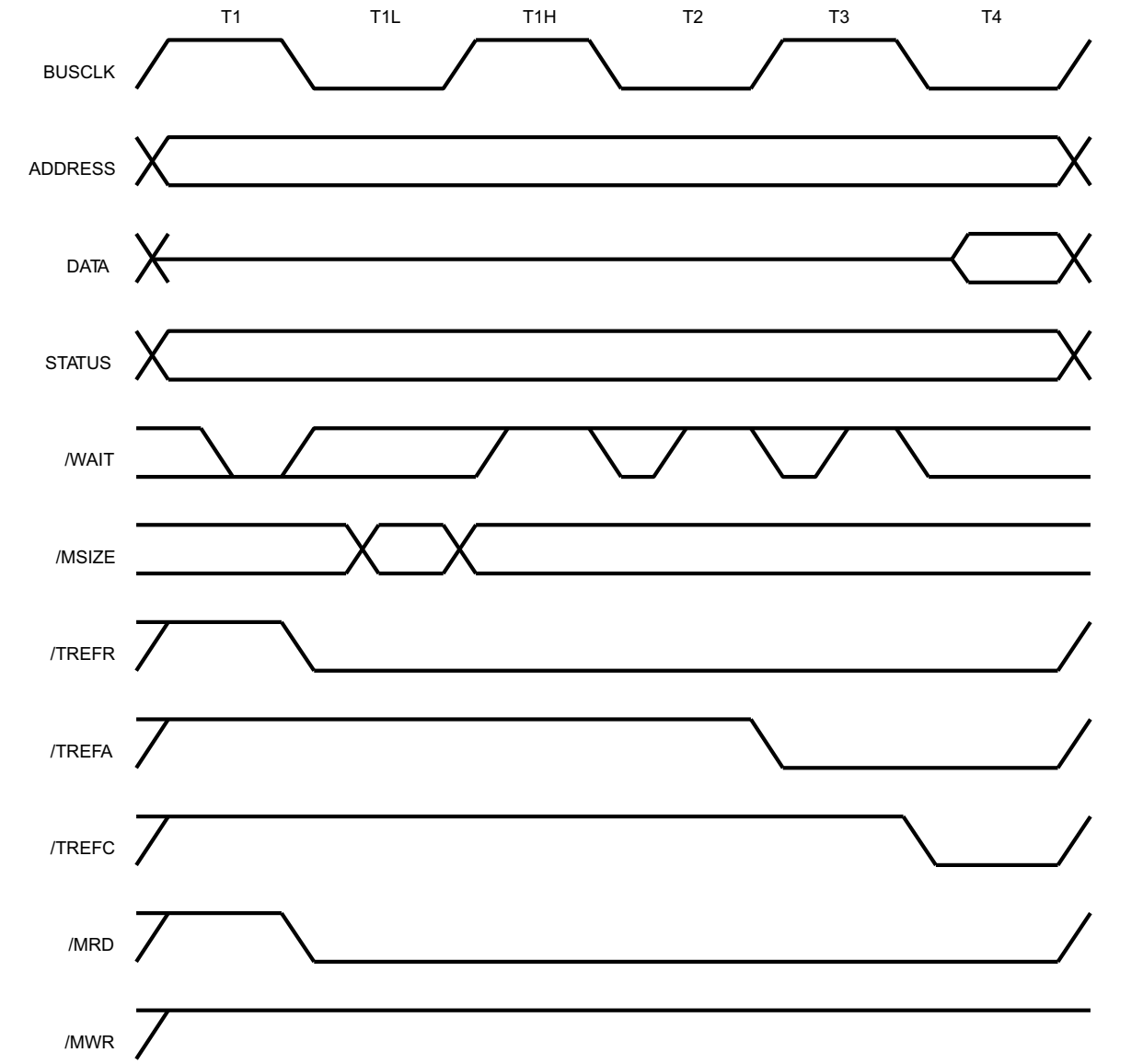

Figure 4. Read Cycle, T1 Wait

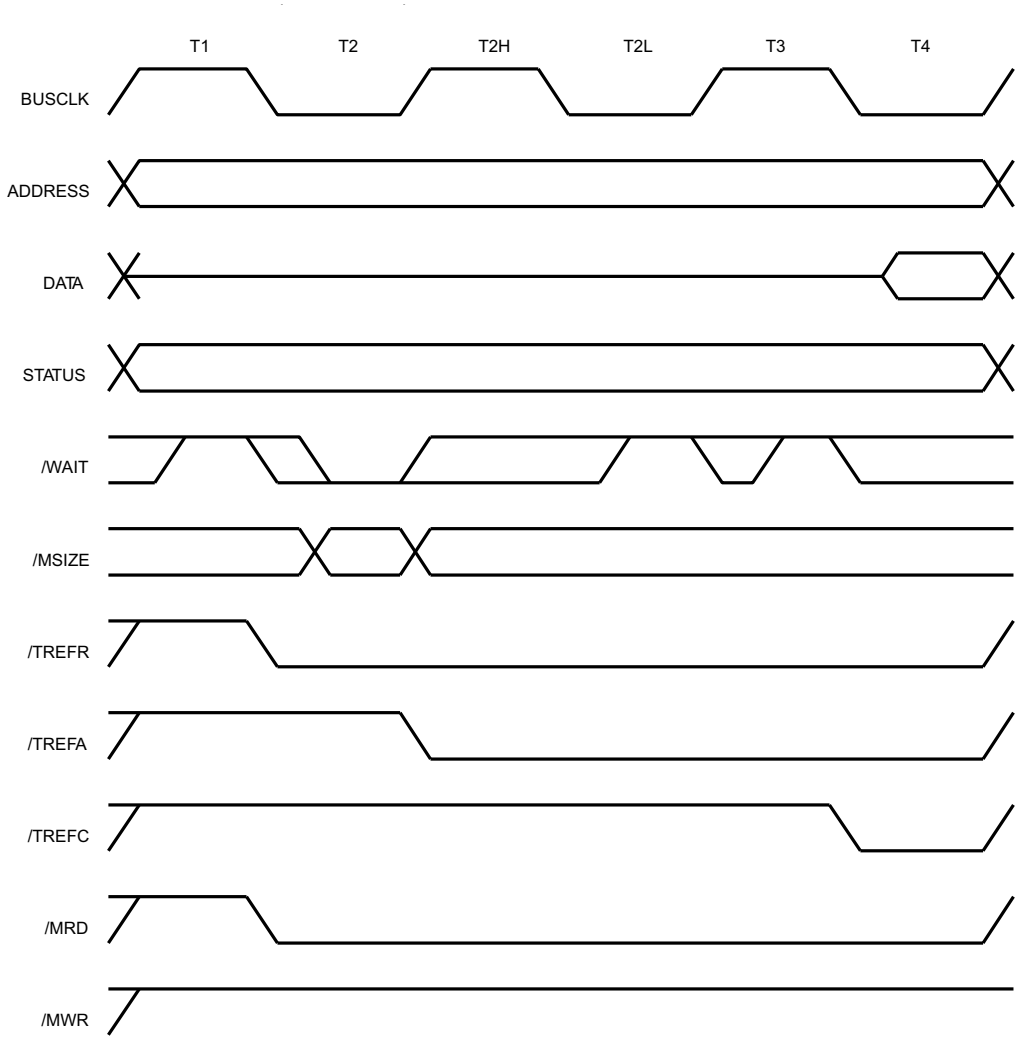

Figure 5. Read Cycle, T2 Wait

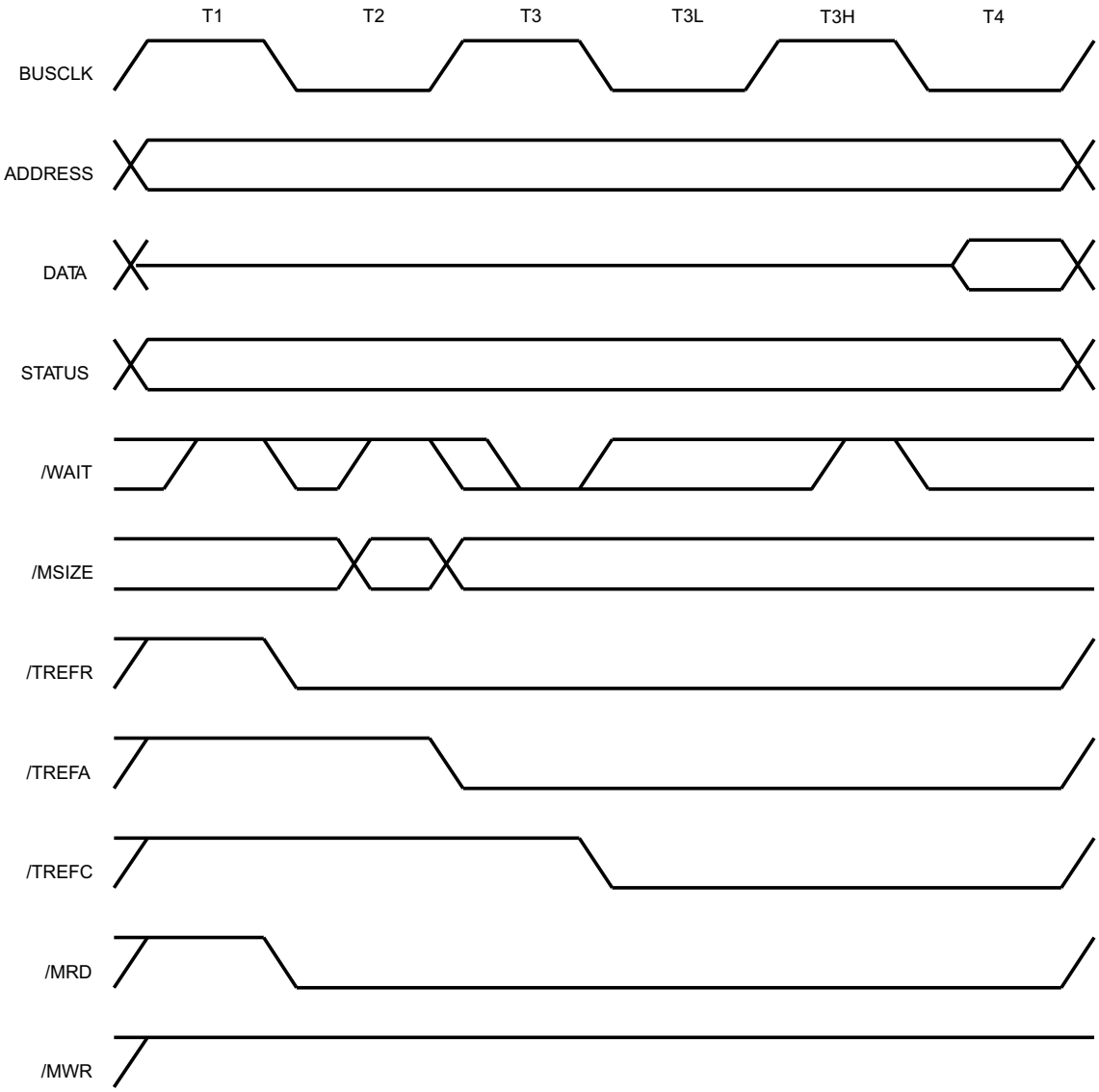

Figure 6. Read Cycle, T3 Wait

EXTERNAL INTERFACE (Continued)

Write memory transactions are shown without wait states, with wait states between T1 and T2, between T2 and T3, and between T3 and T4 (Figures 7-10). The /MWR strobe is activated at the end of T1, to allow write data setup time for the memory since the write data is driven on to the data bus at the beginning of T1.

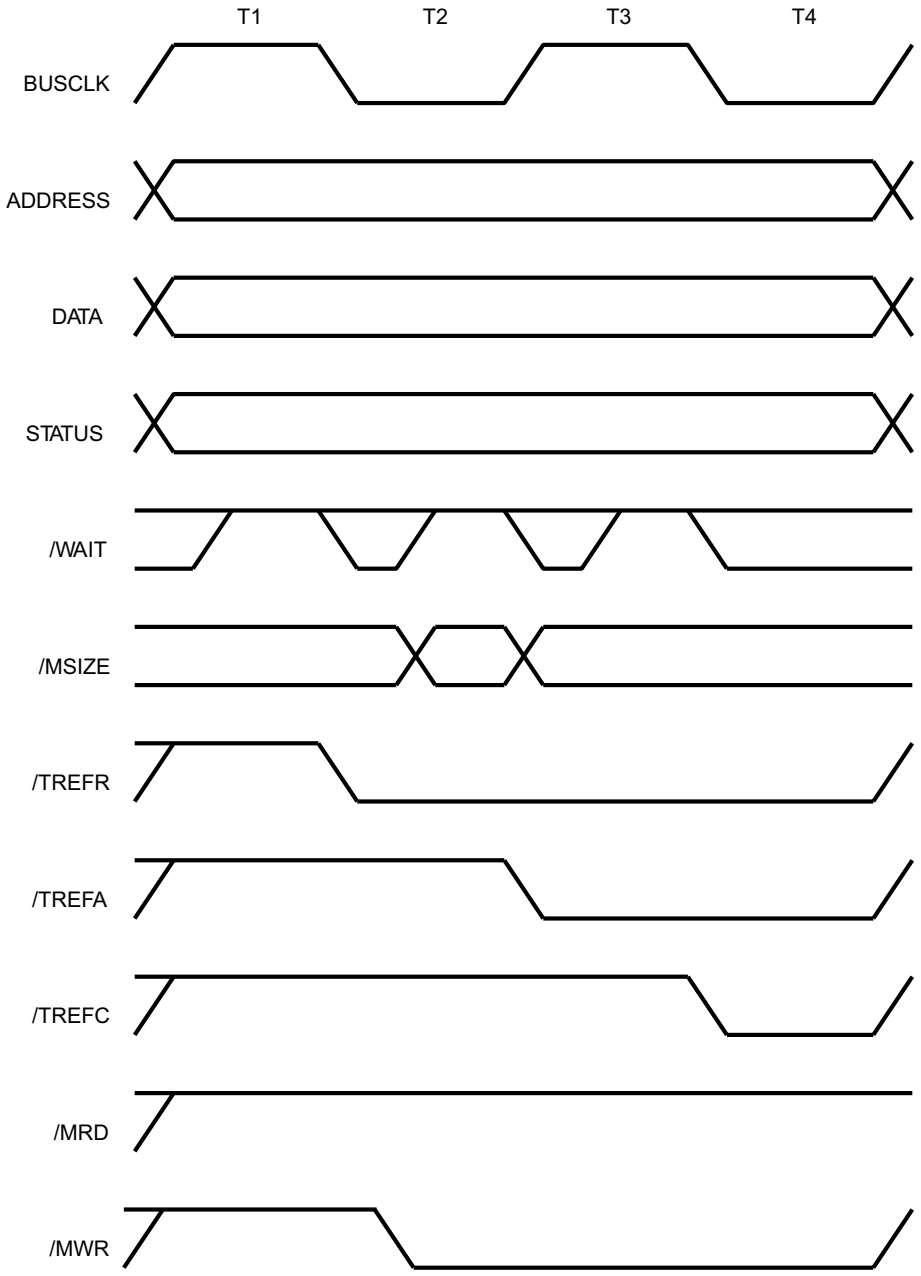

Figure 7. Write Cycle, No Waits

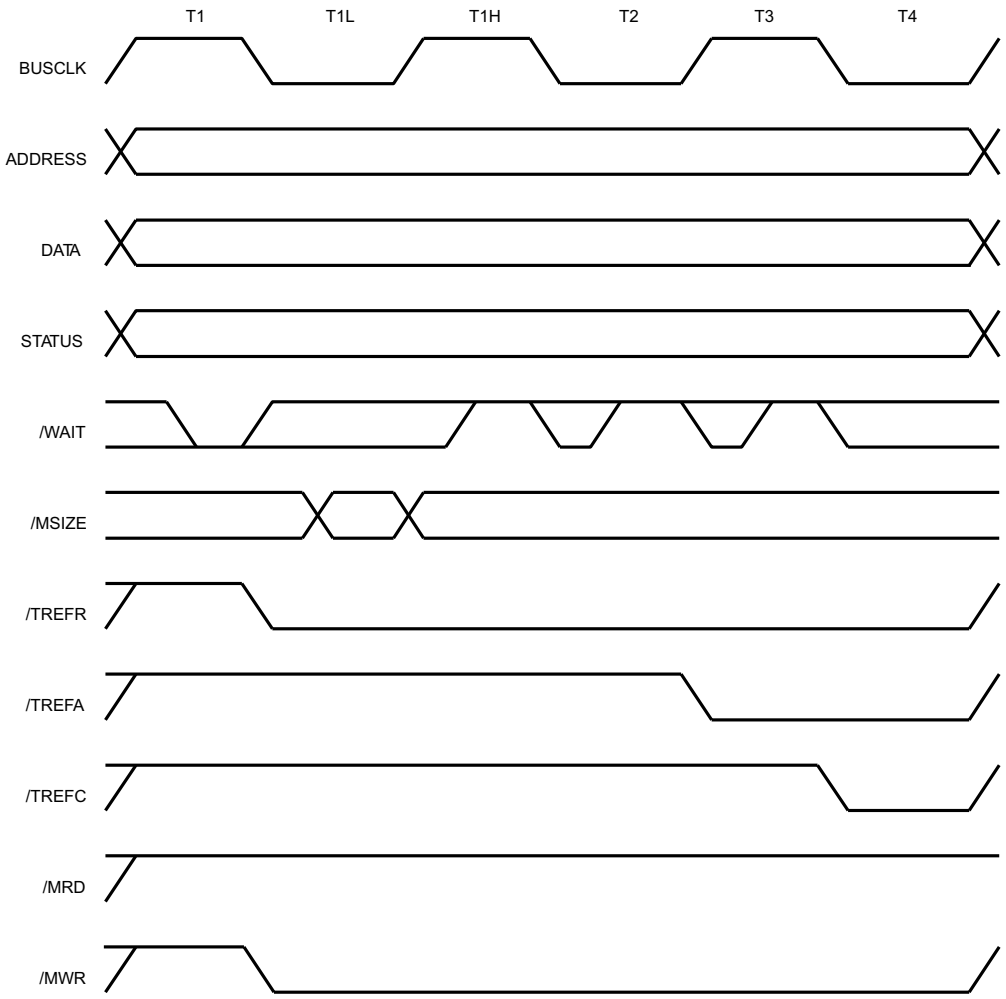

Figure 8. Write Cycle, T1 Wait

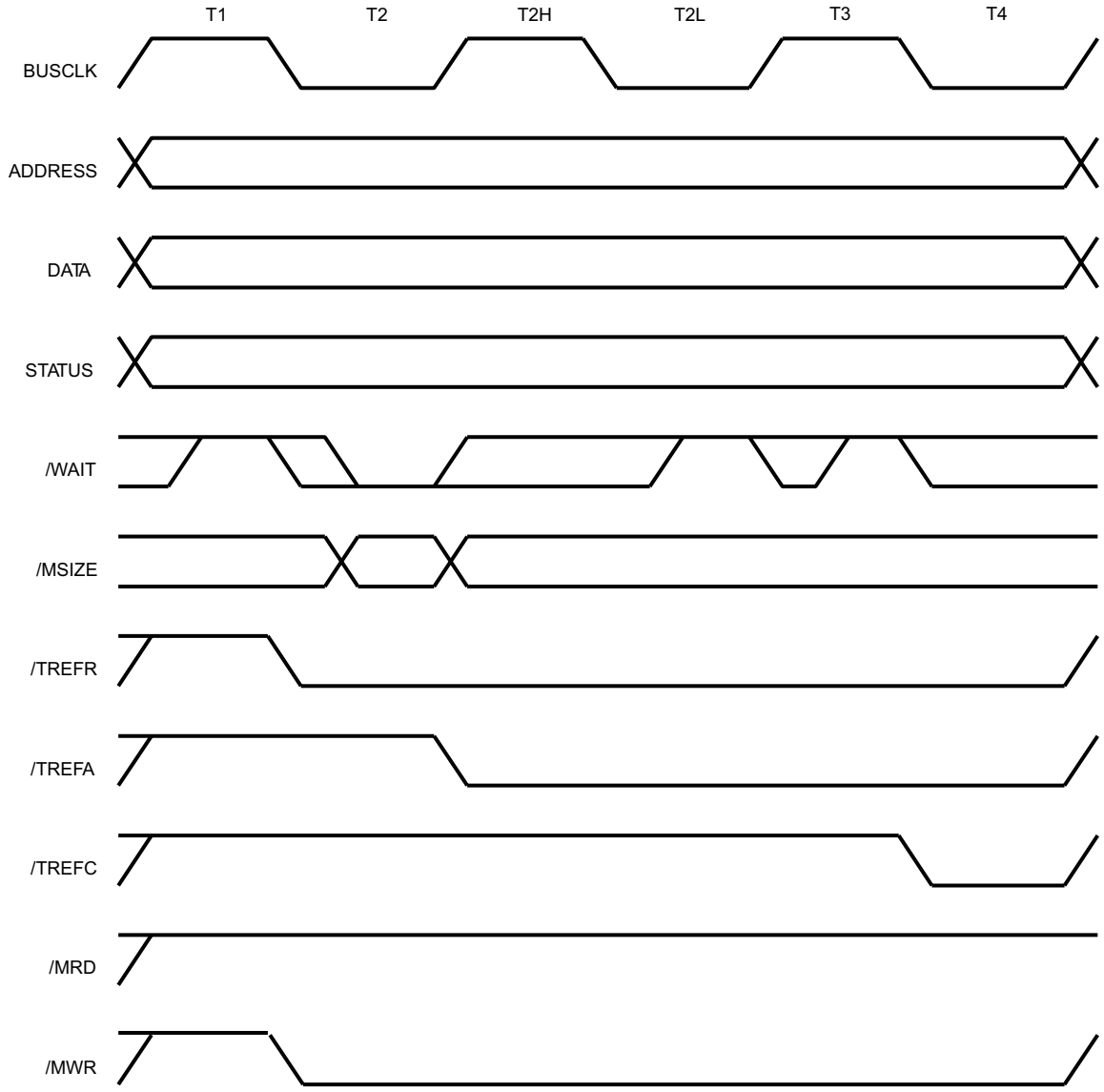

Figure 9. Write Cycle, T2 Wait

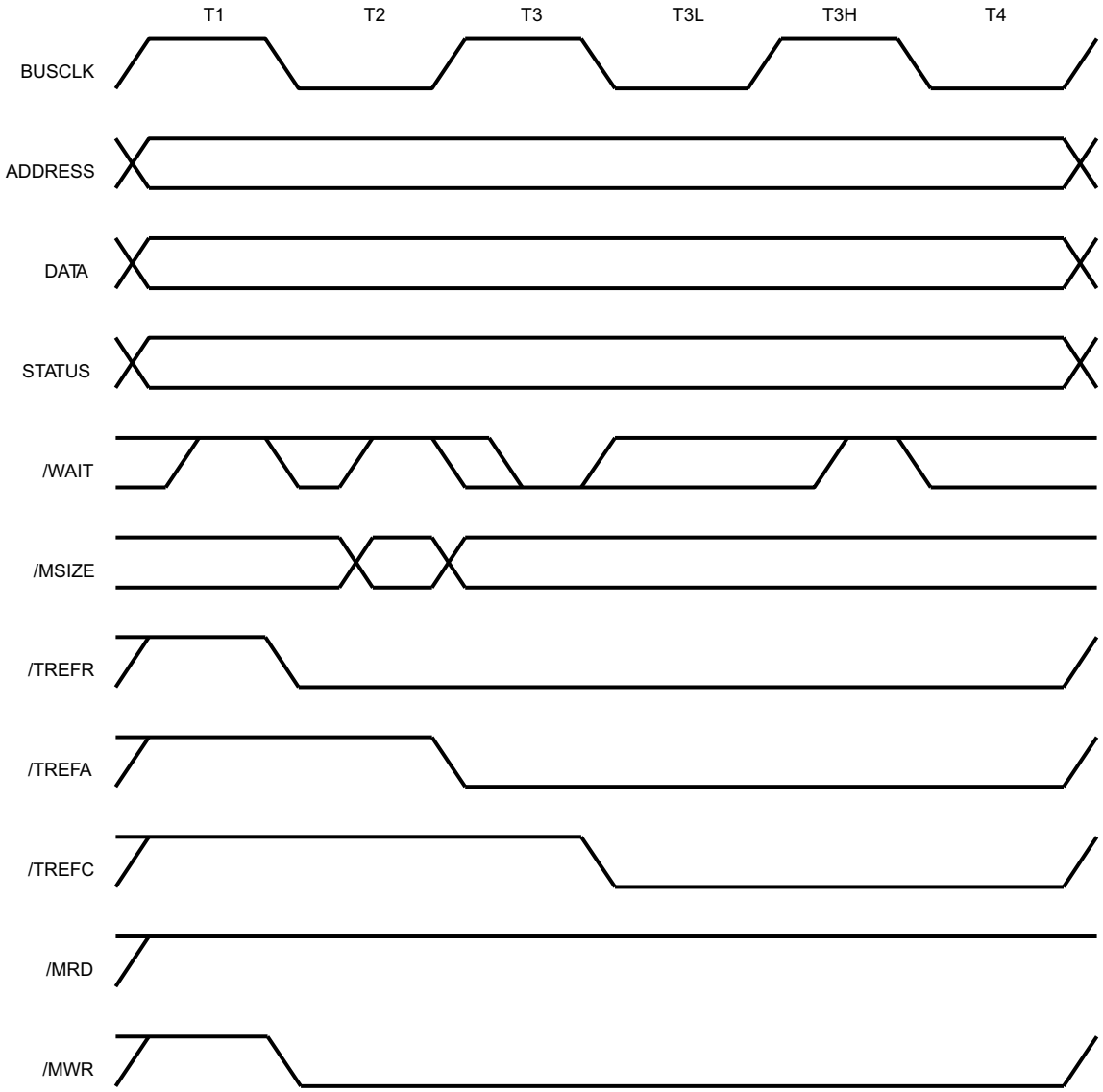

Figure 10. Write Cycle, T3 Wait

EXTERNAL INTERFACE (Continued)

Refresh Transactions

A memory refresh transaction is generated by the Z380 MPU refresh controller and can occur immediately after the final clock cycle of any other transaction. The address during the refresh transaction is not defined as the CAS-before-RASrefresh cycle is assumed, which uses the on-chip refresh address generator present on DRAMs. Prior to the first refresh transaction, a refresh setup cycle is performed to guarantee that the /CAS pre-charge time is met. This refresh setup cycle is present only prior to the first refresh transaction in a burst (Figure 11). Refresh transactions are shown without wait states, with wait states between T1 and T2, between T2 and T3, and between T3 and T4 (Figures 12-15). Note that during the refresh cycle the data bus is continuously driven, /MRD and /MWR remain inactive, /BHEN and /BLEN are active to enable all /CAS signals to the DRAMS, and those Chip Select signals enabled for DRAM refresh transactions are active.

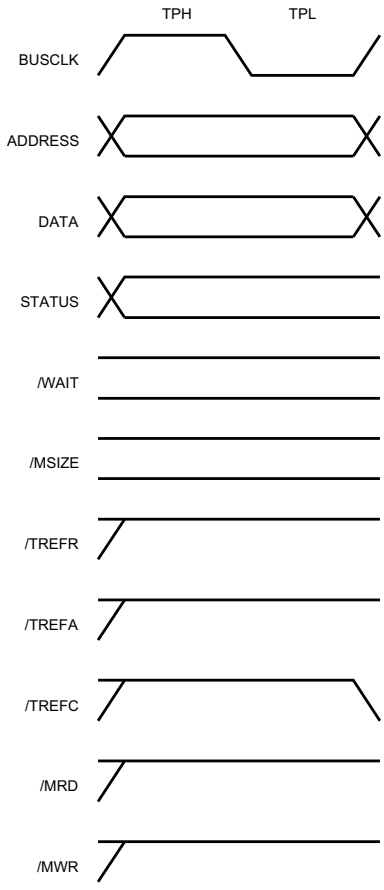

Figure 11. Refresh Setup

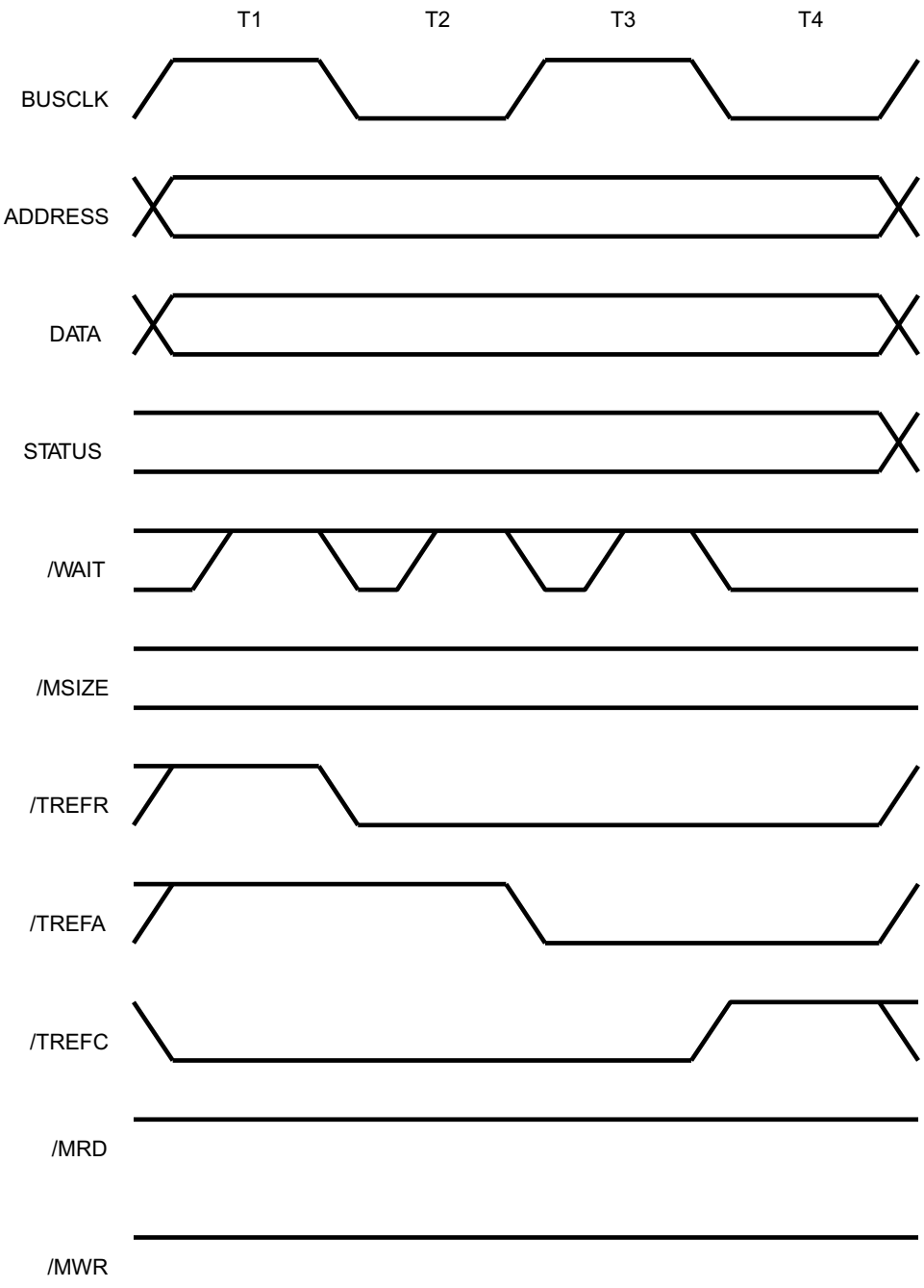

Figure 12. Refresh Cycle, No Waits

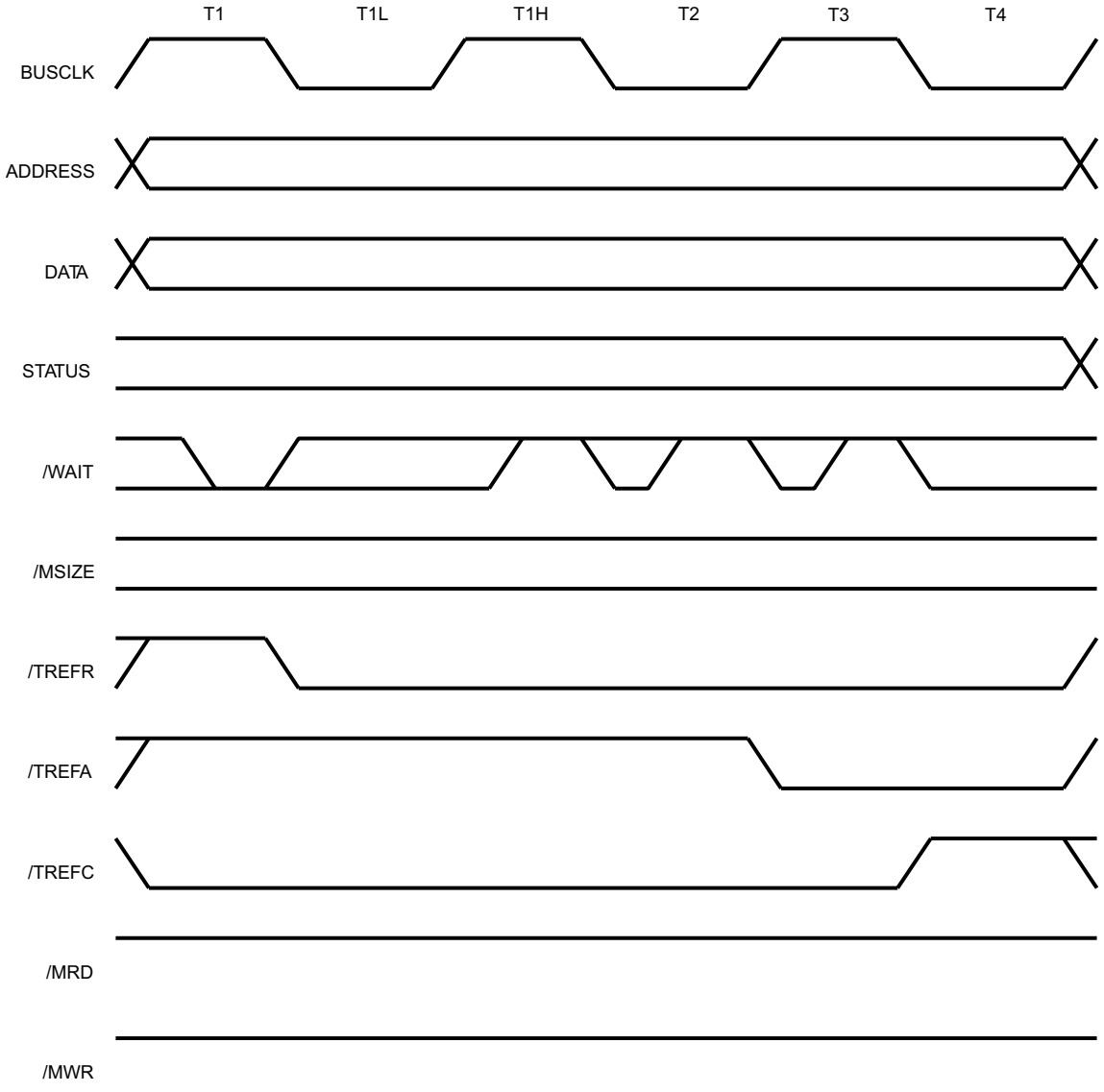

Figure 13. Refresh Cycle, T1 Wait

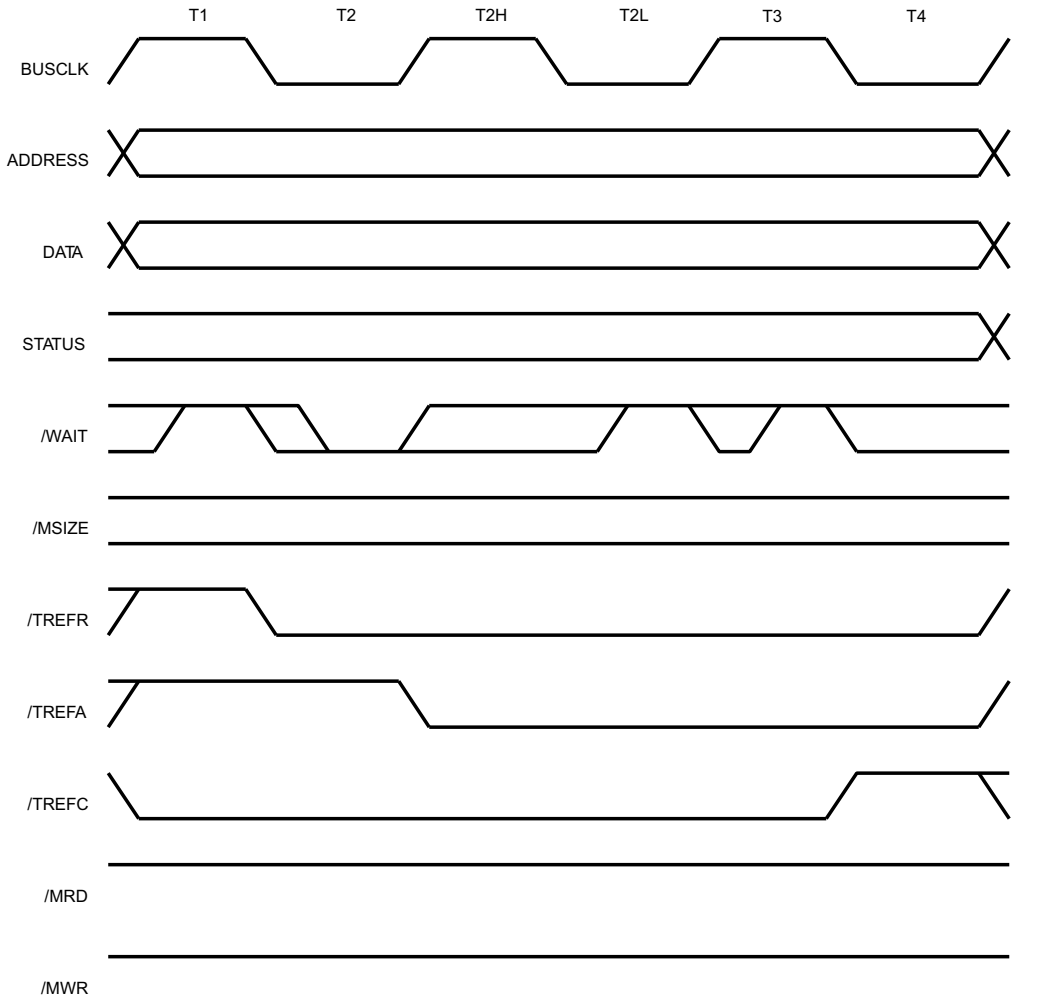

Figure 14. Refresh Cycle, T2 Wait

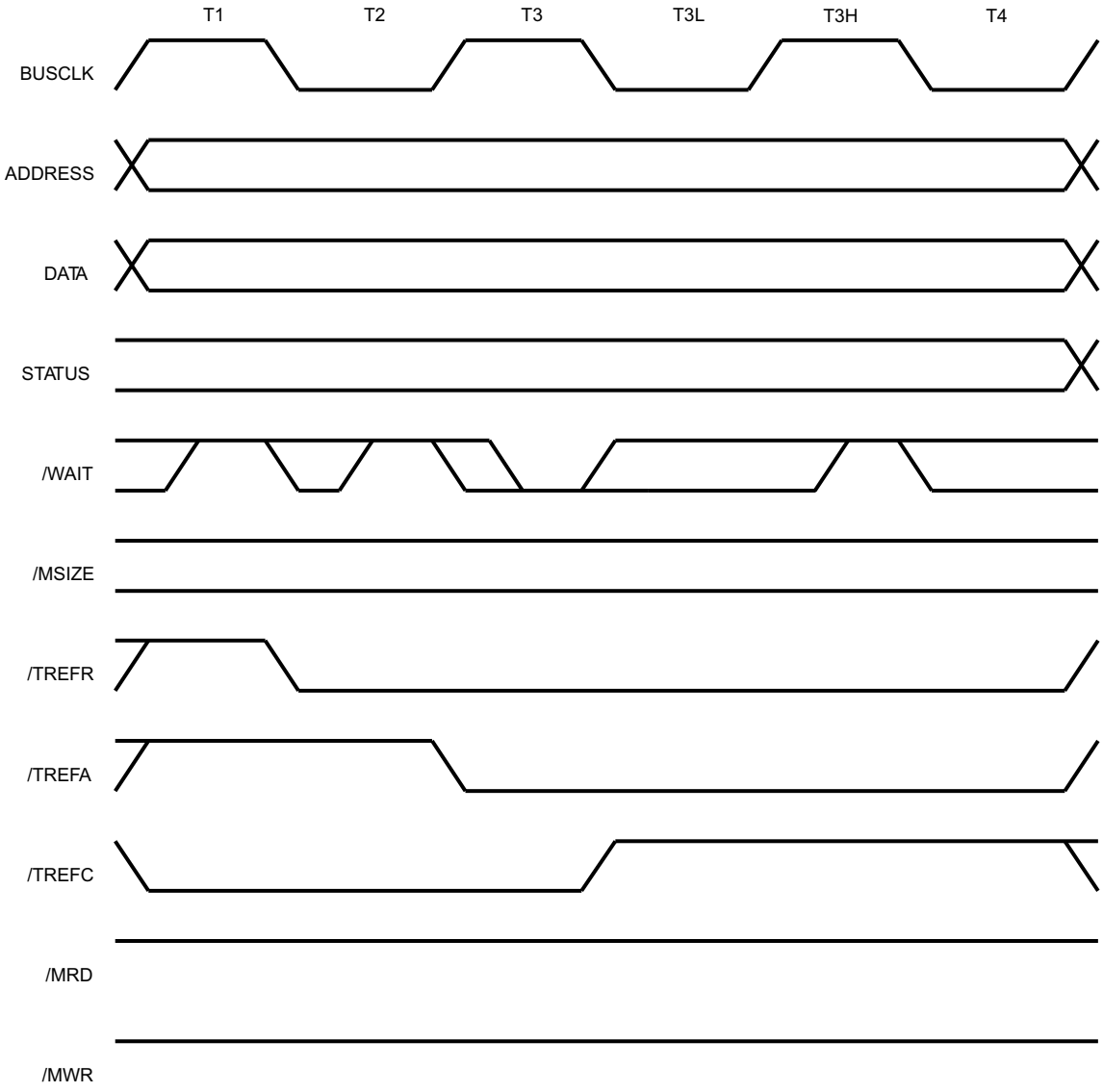

Figure 15. Refresh Cycle, T3 Wait