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Z80C30/Z85C30

CMOS SCC Serial Communications Controller

Product Specification

PS011703-0102

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Overview

- Z85C30: Optimized for Non-Multiplexed Bus Microprocessors. Z80C30: Optimized for Multiplexed Bus Microprocessors

- Pin Compatible to NMOS Versions

- Two Independent, 0 to 4.1 Mbit/Second, Full-Duplex Channels. Each channel with Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop (DPLL) for Clock Recovery.

- Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.

- Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character, Programmable Clock Factor, Break Detection and Generation; Parity, Overrun, and Framing Error Detection.

- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to either 1s or 0s.

- SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop.

- Software Interrupt Acknowledge Feature (not available with NMOS)

- Local Loopback and Auto Echo Modes

- Supports T1 Digital Trunk

- Enhanced DMA Support (not available with NMOS) 10 x 19-Bit Status FIFO 14-Bit Byte Counter

- Speeds:
    – Z85C3O-8.5, 10, 16.384 MHz
    – Z80C3O-8, 10 MHz

Other Features for Z85C30 Only

Some of the features listed below are available by default. Some of them (features with *) are disabled on default to maintain compatibility with the existing SCC design, and "program to enable through WR7".

- New programmable WR7' (write register 7 prime) to enable new features
- Improvements to support SDLC mode of synchronous communication
    – Improve functionality to ease sending back-to-back frames
    – Automatic SDLC opening Flag transmission*
    – Automatic Tx Underrun/EOM Latch reset in SDLC mode*
    – Automatic $\overline{RTS}$ deactivation*
    – TxD pin forced High in SDLC NRZI mode after closing flag*
    – Complete CRC reception*
    – Improved response to Abort sequence in status FIFO
    – Automatic Tx CRC generator preset/reset
    – Extended read for write registers*
    – Write data set-up timing improvement
- Improved AC timing
    – Three to 3.6 PCLK access recovery time.
    – Programmable $\overline{DTR}/\overline{REQ}$ timing*

- – Write data to falling edge of $\overline{\text{WR}}$ set-up time requirement is now eliminated
- – Reduced $\overline{\text{INT}}$ timing
- Other features include.
  - – Extended read function to read back the written value to the write registers.*
  - – Latching RRO during read
  - – RRO, bit D7 and RR10, bit D6 now has reset default value.

General Description

The ZiLOG Z80C30/Z85C30 Serial Communications Controller (SCC), is a pin and software compatible CMOS member of the SCC family introduced by ZiLOG in 1981. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPU's with either multiplexed or non-multiplexed address/data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. Figure 1 illustrates a block diagram of the SCC.

The many on-chip features such as Baud Rate Generators (BRG), Digital Phase Locked Loops (DPLL), and crystal oscillators reduce the need for external logic. Additional features include a 10 x 19-bit status FIFO and 14-bit byte counter to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device generates and checks CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also contains facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The daisy-chain interrupt hierarchy is also supported.
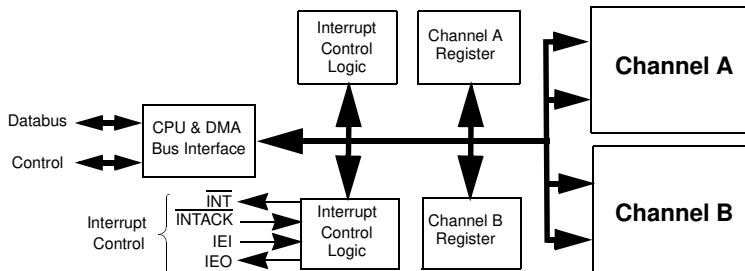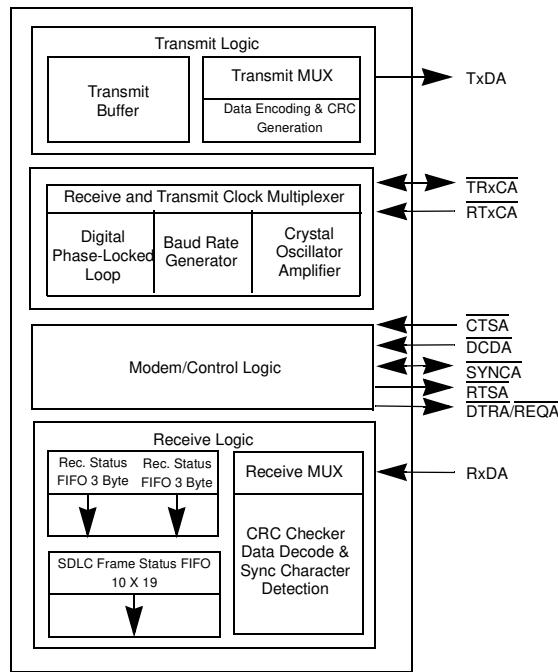
Figure 1. SCC Block Diagram

Pin Descriptions

Z85C30/Z80C30 Common Pin Functions

The following section describes the pin functions common to the Z85C30 and the Z80C30. Figures 2 and 3 detail the respective pin assignments and Figures 4 and 5 designate the pin functions.

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$

Clear To Send (inputs, active Low). If these pins are programmed for Auto Enable, a Low on the inputs enables the respective transmitters. If not programmed as Auto Enable, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs.The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$

Data Carrier Detect (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enable. Otherwise, these pins are used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

$\overline{\text{DTR}}$/$\overline{\text{REQA}}$, $\overline{\text{DTR}}$/$\overline{\text{REQB}}$

Data Terminal Ready/Request (outputs, active Low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller.

IEI

Interrupt Enable In (input, active High). IEI is used with IEO to form an interrupt daisy-chain when there is more than one interrupt driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO

Interrupt Enable Out (output, active High). IEO is High only if IEI is High and the CPU is not servicing the SCC interrupt or the SCC is not requesting an interrupt (interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{\text{INT}}$

Interrupt Request (output, open-drain, active Low). This signal activates when the SCC requests an interrupt.

$\overline{\text{INTACK}}$

Interrupt Acknowledge (input, active Low). This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{\text{RD}}$ or $\overline{\text{DS}}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). $\overline{\text{INTACK}}$ is latched by the rising edge of PCLK.

PCLK

Clock (input). This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.

RxDA, RxDB

Receive Data (inputs, active High). These signals receive serial data at standard TTL levels.

$\overline{\text{RTXCA}}$, $\overline{\text{RTXCB}}$

Receive/Transmit Clocks (inputs, active Low). These pins can be programmed in several different operating modes. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the Baud Rate Generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$

Request To Send (outputs, active Low). When the Request To Send (RTS) bit in Write Register 5 (Figure 9) sets, the IRTS signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode it strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$

Synchronization (inputs or outputs, active Low). These pins function as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 (Figure 8) but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven Low for two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized This synchronous condition is not latched. These outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

TxDA, TxDB

Transmit Data (outputs, active High). These output signals transmit serial data at standard TTL levels.

$\overline{TRXCA}$, $\overline{TRXCB}$

Transmit/Receive Clocks (inputs or outputs, active low). These pins can be programmed in several different operating modes. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-locked loop, the crystal oscillator, the Baud Rate Generator, or the transmit clock in the output mode.

$\overline{W}/\overline{REQA}$, $\overline{W}/\overline{REQB}$

Wait/Request (outputs, open-drain when programmed for a Wait function, driven High or low when programmed for a Request function). These dual-purpose outputs may be programmed as

Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

Z85C30

A/$\overline{\text{B}}$

Channel A/Channel B (input). This signal selects the channel in which the read or write operation occurs.

$\overline{\text{CE}}$

Chip Enable (input, active Low). This signal selects the SCC for a read or write operation.

D7–D0

Data Bus (bidirectional, tri-state). These lines carry data and command to and from the SCC.

D/$\overline{\text{C}}$

Data/Control Select (input). This signal defines the type of information transferred to or from the SCC. A High indicates a data transfer; a Low indicates a command.

$\overline{\text{RD}}$

Read (input, active Low). This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.

$\overline{\text{WR}}$

Write (input, active Low). When the SCC is selected, this signal indicates a write operation. The coincidence of IAD and $\overline{\text{WR}}$ is interpreted as a reset.

Z80C30

AD7–AD0

Address/Data Bus (bidirectional, active High, Tri-state). These multiplexed lines carry register addresses to the SCC as well as data or control information.

$\overline{\text{AS}}$

Address Strobe (input, active Low). Addresses on AD7–AD0 are latched by the rising edge of this signal.

$\overline{\text{CS0}}$

Chip Select 0 (input, active Low). This signal is latched concurrently with the addresses on AD7–AD0 and must be active for the intended bus transaction to occur.

CS1

Chip Select 1 (input, active High). This second select signal must also be active before the intended bus transaction can occur. CS1 must remain active throughout the transaction.

$\overline{\text{DS}}$

Data strobe (input, active Low). This signal provides timing for the transfer of data into and out of the SCC. If $\overline{\text{AS}}$ and $\overline{\text{DS}}$ coincide, this confluence is interpreted as a reset.

R/$\overline{\text{W}}$

Read/Write (input). This signal specifies whether the operation to be performed is a read or a write.

Z85C30				Z80C30			
D1	1	40	D0	AD1	1	40	AD0
D3	2	39	D2	AD3	2	39	AD2
D5	3	38	D4	AD5	3	38	AD4
D7	4	37	D6	AD7	4	37	AD6
$\overline{\text{INT}}$	5	36	$\overline{\text{RD}}$	$\overline{\text{INT}}$	5	36	$\overline{\text{DS}}$
IEO	6	35	$\overline{\text{WR}}$	IEO	6	35	$\overline{\text{AS}}$
IEI	7	34	A/$\overline{\text{B}}$	IEI	7	34	R/$\overline{\text{W}}$
$\overline{\text{INTACK}}$	8	33	$\overline{\text{CE}}$	$\overline{\text{INTACK}}$	8	33	$\overline{\text{CS0}}$
+5v	9	32	D/$\overline{\text{C}}$	+5v	9	32	CS1
$\overline{\text{W/REQA}}$	10	31	GND	$\overline{\text{W/REQA}}$	10	31	GND
$\overline{\text{SYNCA}}$	11	30	$\overline{\text{W/REQB}}$	$\overline{\text{SYNCA}}$	11	30	$\overline{\text{W/REQB}}$
$\overline{\text{RTxCA}}$	12	29	$\overline{\text{SYNCB}}$	$\overline{\text{RTxCA}}$	12	29	$\overline{\text{SYNCB}}$
RxDA	13	28	$\overline{\text{RTxCB}}$	RxDA	13	28	$\overline{\text{RTxCB}}$
$\overline{\text{TRxCA}}$	14	27	RxDB	$\overline{\text{TRxCA}}$	14	27	RxDB
TxDA	15	26	$\overline{\text{TRxCB}}$	TxDA	15	26	$\overline{\text{TRxCB}}$
$\overline{\text{DTR/REQA}}$	16	25	TxDB	$\overline{\text{DTR/REQA}}$	16	25	TxDB
$\overline{\text{RTSA}}$	17	24	$\overline{\text{DTR/REQB}}$	$\overline{\text{RTSA}}$	17	24	$\overline{\text{DTR/REQB}}$
$\overline{\text{CTSA}}$	18	23	RTSB	$\overline{\text{CTSA}}$	18	23	$\overline{\text{RTSB}}$
$\overline{\text{DCDA}}$	19	22	$\overline{\text{CTSB}}$	$\overline{\text{DCDA}}$	19	22	$\overline{\text{CTSB}}$
PCLK	20	21	$\overline{\text{DCDB}}$	PCLK	20	21	$\overline{\text{DCDB}}$

Figure 2. Z85C30 and Z80C30 DIP Pin Assignments
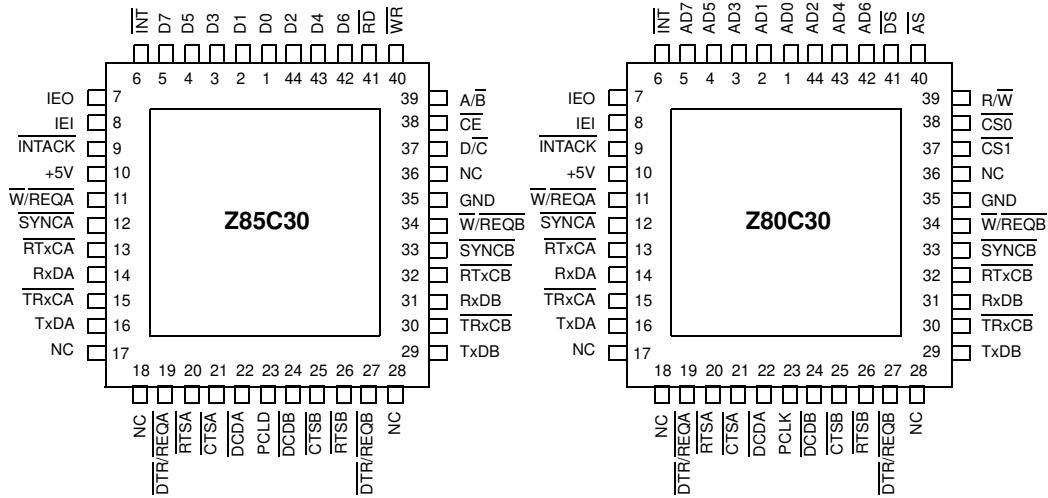
Figure 3. Z85C30 and Z80C30 PLCC Pin Assignments
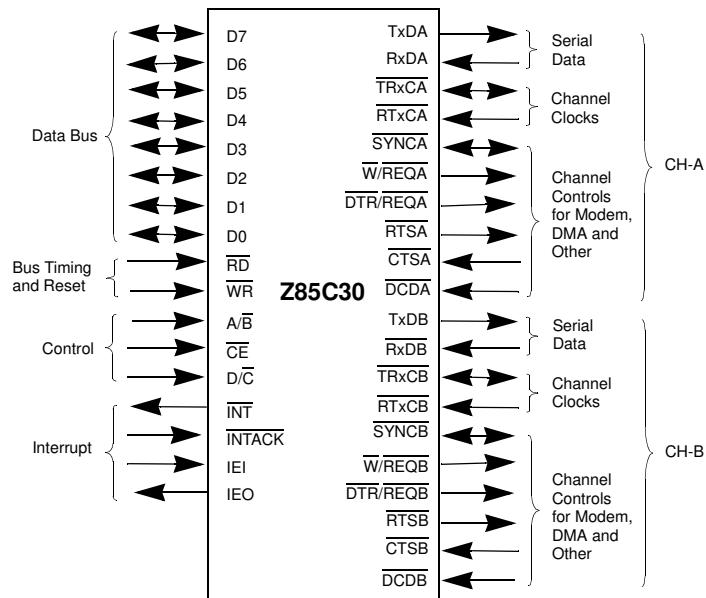
Figure 4. Z85C30 Pin Functions
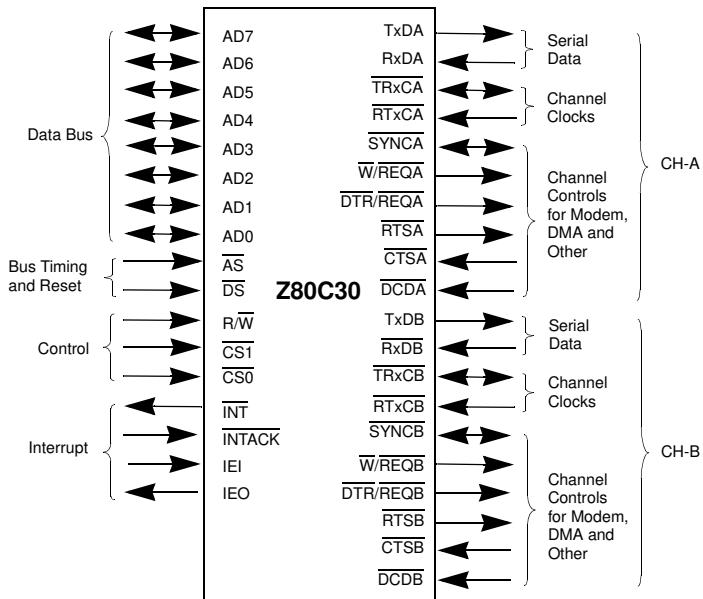
**Figure 5. Z80C30 Pin Functions**

Functional Description

The architecture of the SCC is described from two points of view:

- As a data communications device which transmits and receives data in a wide variety of protocols;

- As a microprocessor peripheral in which the SCC offers valuable features such as vectored interrupts and DMA support.

The SCC's peripheral and data communication are described in the following sections. Figure 1 on page 6 illustrates the SCC block diagram. Figures 6 and 7 show the details of the communications between the receive and transmit logic to the system bus. The features and data path for each of the SCC's A and B channels is identical.